LECTURE 410 – HIGH-SPEED COMPARATORS
(READING: AH – 483-488)

Objective

The objective of this presentation is:

1.) Show how to achieve high-speed comparators

Outline

- Concepts of high-speed comparators
- Amplifier-latch comparators
- Summary

Conceptual Illustration of a Cascaded Comparator

How does a cascaded, high-speed comparator work?

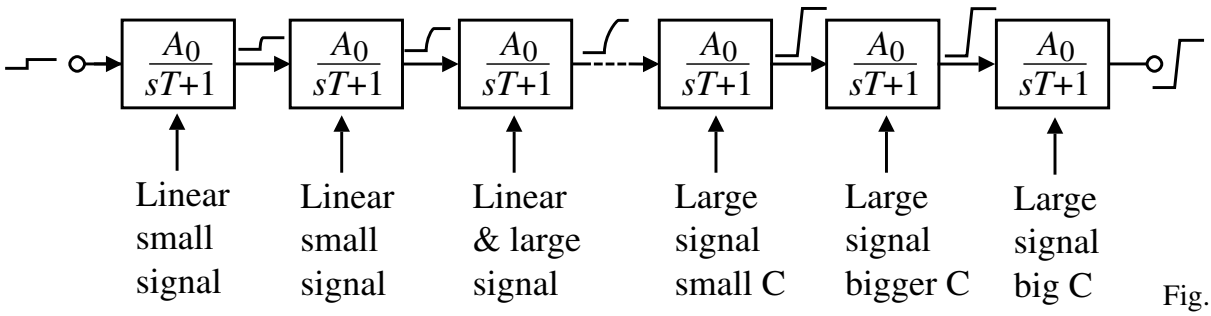


Fig. 8.6-1

Assuming a small overdrive,

1.) The initial stage build the driving capability.

2.) The latter stages swing rail-to-rail and build the ability to quickly charge and discharge capacitance.

Minimizing the Propagation Delay Time in Comparators

Fact:

- The input signal is equal to V_{in}(min) for worst case
- Amplifiers have a step response with a negative argument in the exponential
- Latches have a step response with a positive argument in the exponential

Result:

Use a cascade of linear amplifier to quickly build up the signal level and apply this amplified signal level to a latch for quick transition to the full binary output swing.

Illustration of a preamplifier and latch cascade:

Minimization of t_p:

Q. If the preamplifer consists of n stages of gain A having a single-pole response, what is the value of n and A that gives minimum propagation delay time?

A. $n = 6$ and $A = 2.62$ but this is a very broad minimum and n is usually 3 and $A \approx$ 6-7 to save area.

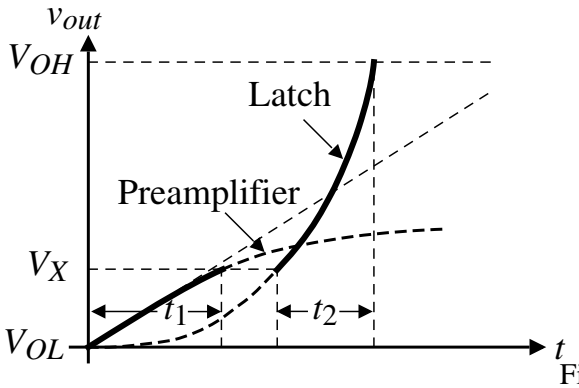


Fig. 8.6-2

Fully Differential, Three-Stage Amplifier and Latch Comparator

Circuit:

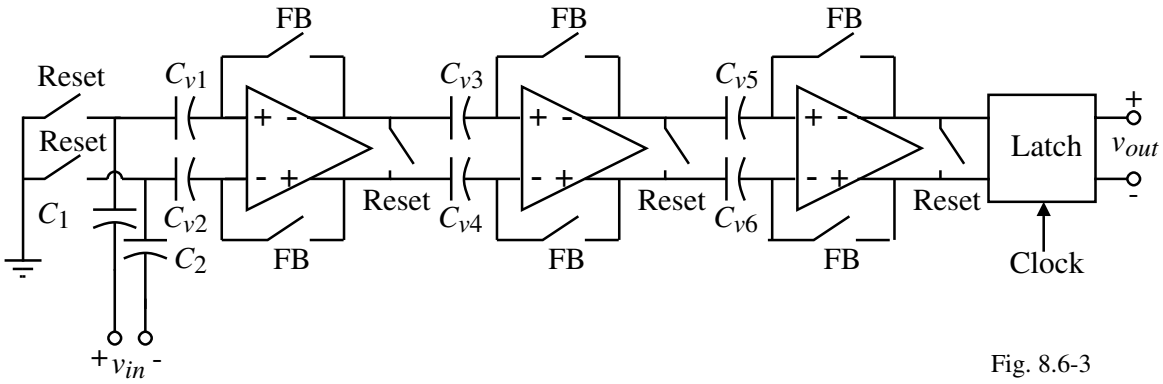


Fig. 8.6-3

Comments:

- Autozero and reset phase followed by comparison phase
- More switches are needed to accomplish the reset and autozero of all preamplifiers simultaneously
- Can run as high as 100Msps

Preamplifier and Latch Circuits

Gain:

$$A_v = -\frac{g_{m1}}{g_{m3}} = -\frac{g_{m2}}{g_{m4}} = -\sqrt{\frac{K_N'(W_1/L_1)}{K_p'(W_3/L_3)}}$$

Dominant Pole:

$$|p_{dominant}| = \frac{g_{m3}}{C} = \frac{g_{m4}}{C}$$

where C is the capacitance seen from the output nodes to ground.

If $(W_1/L_1)/(W_3/L_3) = 100$ and the bias current is 100μA, then $A = -3.85$ and the bandwidth is 15.9MHz if $C = 0.5$pF.

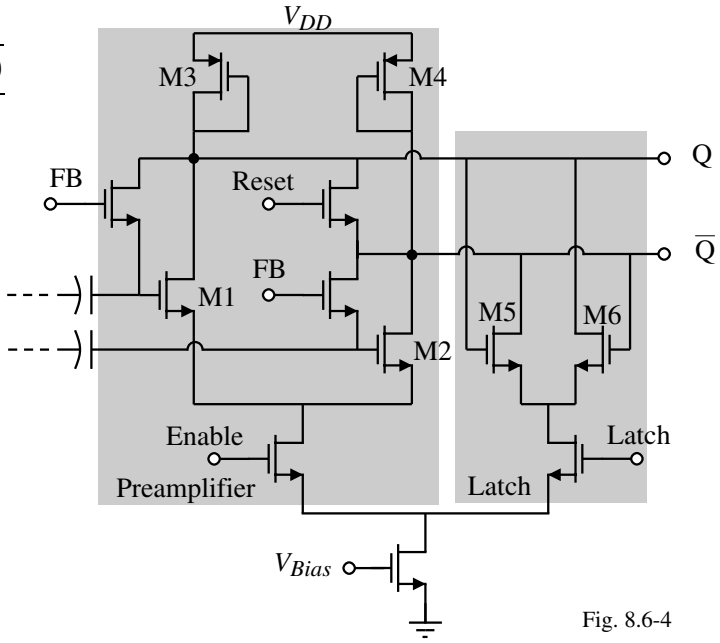


Fig. 8.6-4

Comments:

- If a buffer is used to reduce the output capacitance, one must take into account the loss of the buffer.
- The use of a preamplifier before the latch reduces the latch offset by the gain of the preamplifier so that the offset is due to the preamplifier only.

An Improved Preamplifier

Circuit:

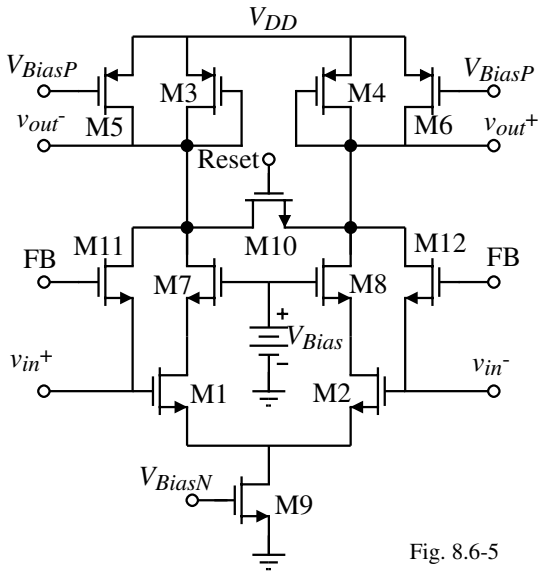


Fig. 8.6-5

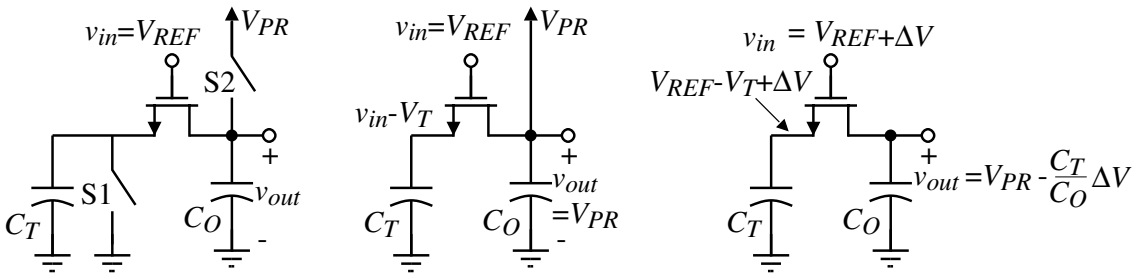
Gain:

$$A_v = -\frac{g_{m1}}{g_{m3}} = -\sqrt{\frac{K_N'(W_1/L_1)I_1}{K_P'(W_3/L_3)I_3}} = -\sqrt{\frac{K_N'(W_1/L_1)}{K_P'(W_3/L_3)}}\sqrt{1+\frac{I_5}{I_3}}$$

If $I_5 = 24I_3$, the gain is increased by a factor of 5

Charge Transfer Preamplifier

The preamplifier can be replaced by the charge transfer circuit shown.



Charge transfer amplifier. Precharge phase. Amplification phase.

Fig. 8.6-6

Comments:

- Only positive values of voltage will be amplified.
- Large offset voltages result as a function of the subthreshold current.

A CMOS Charge Transfer Preamplifier

Circuit:

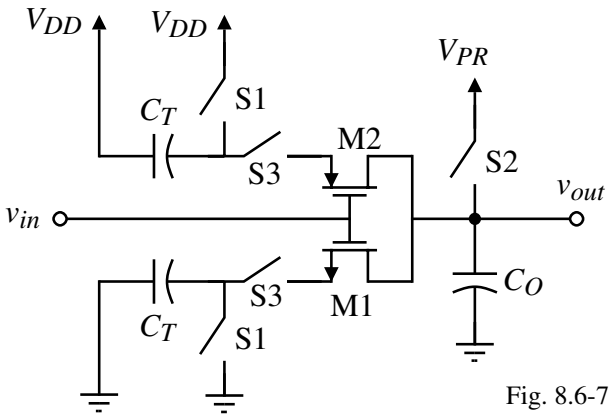


Fig. 8.6-7

Comments:

- NMOS and PMOS allow both polarities of input
- CMOS switches along with dummy switches reduce the charge injection
- Switch S3 prevents the subthreshold current influence
- Used as a preamplifier in a comparator with 8-bit resolution at 20Msps and a power dissipation of less than 5μW

A High-Speed Comparator

Circuit:

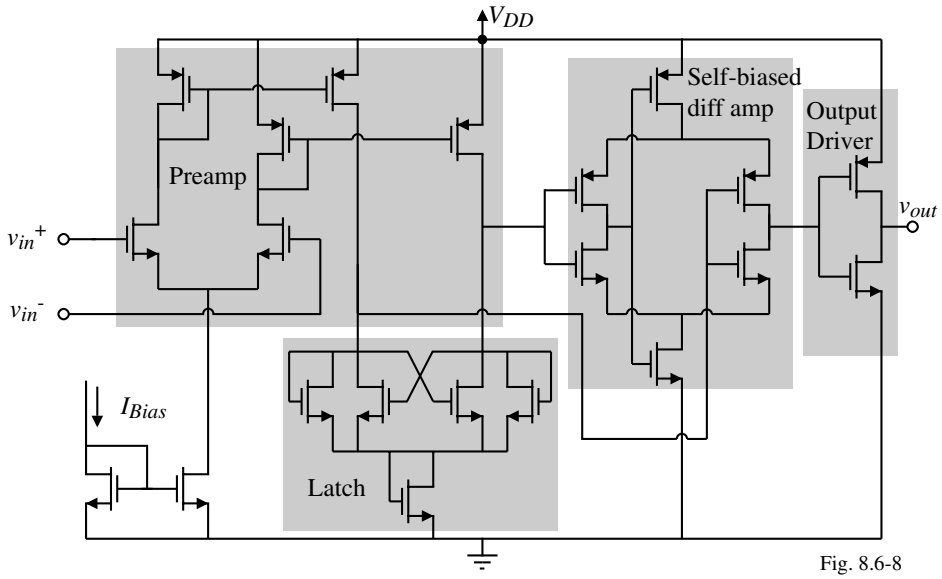


Fig. 8.6-8

Comments:

- Designed to have a t_p = 10ns with a 5pF load and a 10mV overdrive
- Not synchronous
- Comparator gain is greater than 2000V/V and the quiescent current was 100μA

SUMMARY

Types of Comparators Presented

- High-gain, open-loop
- Improved high-gain, open-loop, comparators
  - Hysteresis
  - Autozeroing
- Regenerative comparators
- Discrete-time comparators

Performance Characterization

- Propagation delay time
- Binary output swing
- Input resolution and/or gain
- Input offset voltage
- Power dissipation

Important Principles

- The speed of the comparator depends on the linear and slewing responses
- The dc input offset voltage depends on the matching and is reduced by autozeroing.
  - Charge injection is the limit of autozeroing
- The comparator gain should be large enough for a binary output when $v_{in} = V_{in}$(min)
- Cascaded comparators, the first stages should large *GB* and the last stages high *SR*

