EXAMINATION NO. 2 - SOLUTIONS
(Average score = 75/100)

Problem 1 - (25 points)

A self-compensated op amp has three higher order poles grouped closely around \(-1 \times 10^9\) radians/sec. What should be the \(GB\) of this op amp in Hz to achieve a 60° phase margin? If the low frequency gain of the op amp is 80dB, where is the location of the dominant pole, \(p_1\)? If the output resistance of this amplifier is 10MΩ, what is the value of \(C_L\) that will give this location for \(p_1\)? (Ignore any other capacitance at the output for this part of the problem).

Solution

The key to this problem is to assume that the three closely grouped poles around \(-1 \times 10^9\) radians/sec. can be approximated as three poles at \(-1 \times 10^9\) radians/sec. Therefore,

\[
\text{Phase margin} = \text{PM} = 180° - \tan^{-1}\left(\frac{GB}{|p_1|}\right) - 3 \tan^{-1}\left(\frac{GB}{|p_H|}\right) = 60°
\]

where \(p_H\) is a pole at \(-1 \times 10^9\) radians/sec. Assuming that \(GB/|p_1|\) is large then, we can write the above as,

\[
180° - 90° - 3 \tan^{-1}\left(\frac{GB}{|p_H|}\right) = 60° \rightarrow 30° = -3 \tan^{-1}\left(\frac{GB}{|p_H|}\right) \rightarrow \frac{GB}{|p_H|} = \tan(10°) = 0.1763
\]

\[
\therefore \quad GB = 0.1763|p_H| = 176.3 \text{ Mradians/sec.} \quad \rightarrow \quad GB = 28.06\text{MHz}
\]

80dB \rightarrow 10,000 which gives

\[
|p_1| = \frac{GB}{A_v} = \frac{176.3 \times 10^6}{10^4} = 17,630 \text{ radians/sec.} \quad \rightarrow \quad |p_1| = 2.806\text{kHz}
\]

The expression for \(p_1\) is

\[
|p_1| = \frac{1}{R_{out}C_L} \quad \rightarrow \quad C_L = \frac{1}{R_{out}|p_1|} = \frac{1}{1.763 \times 10^4 \times 10^7} = 5.672\text{pF}
\]
Problem 2 - (25 points)

Design the values of $W$ for each of the transistors of the op amp shown assuming that the channel lengths of all transistors are 1µm. Also design the values of the bias voltages $V_{BN}$ and $V_{BP}$. The transistor model parameters are $K_{N'} = 300\mu A/V^2$, $V_{TN} = 0.5V$, and $K_{P'} = 70\mu A/V^2$, $V_{TP} = -0.5V$. Ignore the bulk effects. Use the following constraints among the transistor widths:

$W_1 = W_2$, $W_4 = W_5$, $W_6 = 10W_4$, $W_7 = 10W_5$, $W_8 = W_9$, and $W_{10} = W_{11} = W_{12} = W_{13}$

Round the values of the transistor widths to the nearest integer that meets or exceeds the specifications. Do not use safety factors or worst case in your design. The op amp specifications assuming a load capacitance of 5pF are:

$V_{icm}^+ = 0.75V$, $V_{icm}^- = -0.25V$, $GB = 200$MHz, $V_{out}^+ = 0.5V$, $V_{out}^- = -0.5V$, $SR = 100V/\mu s$

Solution

1.) $SR = 100V/\mu s \rightarrow I_{out} = C_L \cdot SR = 5 \times 10^{-12} \cdot 10^8 = 500\mu A \rightarrow I_3 = 50\mu A$

2.) $V_{icm}^+ = 0.75V \rightarrow V_{SG4} = V_{DD} - V_{icm}^+ + V_{TN} = 1.0 - 0.75 + 0.5 = 0.75V$

$V_{ON3} = 0.75 - 0.5 = 0.25V \rightarrow \frac{W_4}{L_4} = \frac{2I_4}{K_N(V_{ON4})^2} = \frac{50}{70(0.25)^2} = 11.43 = 12$

$\therefore W_4 = W_5 = 12\mu m \rightarrow W_6 = W_7 = 120\mu m$

3.) $GB = 200$MHz or $GB = 400\pi \times 10^6$ rads/sec.

$GB = \frac{g_{m1}}{C_L} 10 \rightarrow g_{m1} = \frac{GB \cdot C_L}{10} = \frac{400\pi \times 10^6 \cdot 5 \times 10^{-12}}{10} = 628\mu S$

$\frac{W_1}{L_1} = \frac{g_{m1}^2}{2K_NI_1} = \frac{628^2}{50 \cdot 300} = 26.32 = 27 \therefore W_1 = W_2 = 27\mu m$

4.) $V_{icm}^- = -0.25V \rightarrow V_{DS3} = V_{icm}^- V_{GS1} - V_{SS}$

$V_{GS1} = \sqrt{\frac{2.25}{300 \cdot 27} + 0.5} = 0.5786V \rightarrow V_{DS3} = -0.25 - 0.5786 + 1 = 0.1714V$

$\therefore \frac{W_3}{L_3} = \frac{2I_3}{K_N(V_{ON3})^2} = \frac{2.50}{300(0.1714)^2} = 11.34 = 12 \therefore W_3 = 12\mu m$
Problem 2 – Continued

5.) \( V_{out}^+ = 0.5V \)

\[ V_{SD6} = \sqrt{\frac{2 \cdot I_6}{K_N (W_6/L_6)}} = \sqrt{\frac{2 \cdot 250}{70 \cdot 120}} = 0.243V \rightarrow V_{SD8} = 0.256V \]

\[ \therefore W_8/L_8 = \frac{2I_8}{K_P (V_{ON8})^2} = \frac{2 \cdot 250}{70 \cdot (0.256)^2} = 108.99 = 109 \quad \therefore W_8 = W_9 = 109\mu m \]

6.) \( V_{out}^- = -0.5V \) Let \( V_{DS10} = V_{DS12} = 0.25V \)

\[ \frac{W_{12}}{L_{12}} = \frac{2I_{12}}{K_N (V_{ON12})^2} = \frac{2 \cdot 250}{300 \cdot (0.25)^2} = 26.67 = 27 \]

\[ \therefore \frac{W_{10}}{L_{10}} = \frac{W_{11}}{L_{11}} = \frac{W_{12}}{L_{12}} = \frac{W_{13}}{L_{13}} = 27\mu m \]
**Problem 3 - (25 points)**

Assume the following for all transistors: $g_m = 50 \, \text{S}$, $r_{ds} = 100 \, \text{K} \Omega$, $V_{ds, sat} = 300 \, \text{mV}$, $V_{bs} = 0 \, \text{V}$, and $C_L = 25 \, \text{pF}$.

a) Determine the differential small-signal gain at very low frequencies.
b) Determine the Slew-Rate performance.
c) Determine the dominant pole of this circuit.
d) Identify the locations of the non-dominant poles of this circuit (e.g., gate of mnb2b, etc.).
Problem 4 - (25 points)

a) Identify the node that establishes the dominant pole frequency (e.g., base of Q24, etc.).
b) Identify all the nodes that introduce non-dominant poles in the circuit.
c) What is the purpose of Q15?
d) What is the purpose of Q16?
e) What is the purpose of Q17?
f) What is the purpose of Q7?
g) Is the gain from the base of Q17 to the emitter of Q23A high or low?