Problem 1 - (10 points)
For the CMOS op amp shown, find the following quantities.
1.) Slew rate (V/sec.)
2.) Positive and negative output voltage limits (all transistors remain in saturation)
3.) Positive and negative input common voltage limits (all transistors remain in saturation and use nominal parameter values)
4.) Small signal voltage gain
5.) Unity-gainbandwidth (MHz) and 6.) Power dissipation (mW).

Solution
1.) \[ SR = \frac{I_5}{C_c} = \frac{50\mu A}{5pF} = 10^7 V/\text{sec} \]
2.) \[ V_{SD7} = \sqrt{\frac{2I_7}{K_p(W/L)}} = \sqrt{\frac{500\mu A}{50-50}} = 0.447V \text{ and } V_{DS6} = \sqrt{\frac{500\mu A}{110-50}} = 0.3015V \]
   \[ V_{out}(\text{max}) = 2.5 - 0.447 = 2.053V \text{ and } V_{out}(\text{min}) = -2.5 + 0.3015 = -2.198V \]
3.) \[ ICM(\text{min}) = -2.5V + V_{GS3} - IVT^P - V_{TP} = -2.5V + \sqrt{\frac{2.25}{110-10}} = -0.7V \text{ and } V_{SG1} = \sqrt{\frac{2.25}{50-10}} + 0.7 = 1.016V \]
   \[ ICM(\text{max}) = 0.85V + 0.4472V = 1.29V \text{ and } V_{SD5(sat)} = \sqrt{\frac{50}{50-50}} = 0.4472V \text{ and } V_{SG1} = 2.5 - 0.4472 - 1.016 = 1.0366V \]
   \[ ICM(\text{max}) = 1.0366V \]
4.) \[ A_v = \frac{g_{m1}g_{m6}}{(g_{sd2}+g_{ds4})(g_{ds6}+g_{sd7})} \]
   \[ g_{m1} = \sqrt{\frac{2K_pW_1I_1}{L_1}} = \sqrt{\frac{2.5-10-25}{10-10}} = 158\mu S \]
   \[ g_{m6} = \sqrt{\frac{2K_pW_6I_6}{L_6}} = \sqrt{\frac{2.110-50-250}{10-10}} = 1658\mu S \]
   \[ G_I = 0.09-250\mu A = 22.5\mu S \]
   \[ A_v = \frac{158-1658}{2.25} = 3.489V/V \]
5.) \[ GB = \frac{g_{m1}}{C_c} = \frac{158\mu S}{5pF} = 31.6 \text{Mrads/sec} \] 
6.) \[ P_{diss} = 5 \times 350\mu A = 1.75mW \]
Problem 2 - (10 points)

Bias current calculation:

\[ V_{T8} + V_{ON8} + I_s R_s = V_{dd} - V_{ss} \quad \text{or} \quad V_{T8} + \frac{2I_s}{3K_p} = 5 - I_s R_s. \quad (1) \]

Solving for \( I_s \) quadratically would give, \( I_8 = 36 \mu A \), \( I_5 = 36 \mu A \), and \( I_7 = 60 \mu A \)

Using the formula, \( g_m = \sqrt{\frac{2K_I}{L}} \) and \( g_{ds} = \lambda I \) we get,

\[ g_{m2} = 60 \mu S, \quad g_{ds2} = 0.9 \mu S, \quad g_{ds4} = 0.72 \mu S \quad (2) \]
\[ g_{m6} = 363 \mu S, \quad g_{ds6} = 3 \mu S, \quad g_{ds7} = 2.4 \mu S \quad (3) \]

Small-signal open-loop gain:

The small-signal voltage gain can be expressed as,

\[ A_{v1} = \frac{-g_{m2}}{g_{ds2} + g_{ds4}} = -37 \quad \text{and} \quad A_{v2} = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = -67 \]

Thus, total open-loop gain is,

\[ A_v = A_{v1} \cdot A_{v2} = 2489 \text{V/V} \quad (3) \]

Output resistance:

\[ R_{out} = \frac{1}{g_{ds6} + g_{ds7}} = 185K \Omega \quad (5) \]

Power dissipation:

\[ P_{diss} = 5(36 + 36 + 60) \mu W = 660 \mu W \quad (6) \]

ICMR:

\[ V_{in,\text{max}} = 2.5 - V_{T1} - V_{ON1} - V_{ON5} = 0.51V \quad (7) \]
\[ V_{in,\text{min}} = -2.5 - V_{T1} + V_{T3} + V_{ON3} = -2.21V \quad (8) \]

Output voltage swing:

\[ V_{0,\text{max}} = 2.5 - V_{ON7} = 1.81V \quad (9) \]

Slew Rate:

Slew rate under no load condition can be given as,

\[ SR = \frac{I_5}{C_C} = 6V/\mu S \]

In presence of a load capacitor of 20 pF, slew rate would be,

\[ SR = \min \left[ \frac{I_5}{C_C}, \frac{I_7}{C_L} \right] \]
Problem 6.3-7 - Continued

CMRR:

Under perfectly balanced condition where \( I_1 = I_2 \), if a small signal common-mode variation occurs at the two input terminals, the small signal currents \( i_1 = i_2 = i_3 = i_4 \) and the differential output current at node (7) is zero. So, ideally, common-mode gain would be zero and the value for CMRR would be infinity.

GBW:

Let us design M9 and M10 first. Both these transistors would operate in triode region and will carry zero dc current. Thus, \( V_{ds9} = V_{ds10} \equiv 0 \). The equation of drain current in triode region is given as,

\[
I_D \equiv K' \frac{W}{L} (V_{GS} - V_T) V_{DS}.
\]

The on resistance of the MOS transistor in triode region of operation would be,

\[
R_{ON} = K' \frac{W}{L} (V_{GS} - V_T).
\]

It is intended to make the effective resistance of M9 and M10 equal to \( \frac{1}{g_{m6}} \).

So, \[K' \frac{W_9}{L_9} (V_{GS9} - V_{T9}) + K' \frac{W_{10}}{L_{10}} (V_{GS10} - V_{T10}) = g_{m6}\] (11)

\[
V_{D4} = V_{D3} = -2.5 + V_{T3} + V_{ON3} = -1.5V
\]

Thus, \( V_{GS9} \approx 4V \) and \( V_{GS10} \approx -1V \).

Putting the appropriate values in (11), we can solve for the aspect ratios of M9 and M10. One of the solutions could be,

\[
K' \frac{W_9}{L_9} = \frac{1}{1} \quad \text{and} \quad K' \frac{W_{10}}{L_{10}} = \text{very small} \quad (12)
\]

The dominant pole could be calculated as,

\[
p_1 = -\frac{g_{ds4} + g_{ds2}}{2\pi A_{v1} C_C} = -1.16 KHz.
\]

And the load pole would be,

\[
p_2 = -\frac{g_{m6}}{2\pi C_L} = -2.8 MHz \quad \text{for a 20 pF load.}
\]

It can be noted that in this problem, the product of the open-loop gain and the dominant pole is approximately equal to the load pole. Thus, the gain bandwidth is approximately equal to 2.8 MHz and the phase margin would be close to 45 degrees.
Problem 6.3-7 - Continued

PSRR:
If a small ripple $v_S$ is applied at the $V_{dd}$ terminal, then the gain of this ripple from this terminal to the output can be expressed as,

$$\frac{v_o}{v_S} = \frac{R_S}{g_{ds6} + g_{ds7}} = 2.8 \text{V/V}$$

Thus, PSRR due to variations in $V_{dd}$ would be, $A_v \sqrt{2.8} = 2489/2.8 = 889$.

SPICE file:

```plaintext
.model nmos nmos vto=0.7 lambda=0.04 kp=110u
.model pmos pmos vto=-0.8 lambda=0.05 kp=50u

vdd 1 0 dc 2.5 ac 0
vss 10 0 dc -2.5 ac 0
vinp 5 0 dc 0 ac 1
*vinn 4 0 dc 0 ac 0

m8 2 2 1 1 pmos w=3u l=1u
rs 2 10 100k
m5 3 2 1 1 pmos w=3u l=1u
m1 6 8 3 3 pmos w=2u l=1u
m2 7 5 3 3 pmos w=2u l=1u
m3 6 6 10 10 nmos w=4u l=1u
m4 7 6 10 10 nmos w=4u l=1u
m7 8 2 1 1 pmos w=5u l=1u
m6 8 7 10 10 nmos w=10u l=1u
c7 7 9 6p
c18 8 20p
m9 8 1 9 9 nmos w=1u l=1u
m10 8 10 9 9 pmos w=1u l=100u

.op
.ac dec 10 1 100meg
.option post
.end
```

Operating points:

```plaintext
**** mosfets
```

```plaintext

subckt element 0:m8 0:m5 0:m1 0:m2 0:m3 0:m4
model 0:pmos 0:pmos 0:pmos 0:pmos 0:nmos 0:nmos
region Cutoff Cutoff Cutoff Cutoff Saturati Saturati
id -35.3708u -34.8506u -17.4107u -17.4399u -17.4107u -17.4399u
ibs 0. 0. 0. 0. 0. 0.
```
Problem 6.3-7 - Continued

| vgs       | -1.4629 | -1.4629 | -1.3517 | -1.3527 | 975.9818m | 975.9818m |
| vds       | -1.4629 | -1.1473 | -2.8768 | -2.8331 | 975.9818m | 1.0196    |
| vbs       | 0.      | 0.      | 0.      | 0.      | 0.        | 0.        |
| vth       | -800.0000m | -800.0000m | -800.0000m | -800.0000m | 700.0000m | 700.0000m |
| vdsat     | -662.9217m | -662.9217m | -551.7476m | -552.7377m | 275.9818m | 275.9818m |
| beta      | 160.9719u | 158.6045u | 114.3838u | 114.1657u | 457.1773u | 457.9449u |
| gamma     | 527.6252m | 527.6252m | 527.6252m | 527.6252m | 527.6252m | 527.6252m |
| gm        | 106.7118u | 105.1423u | 63.1110u  | 63.1037u  | 126.1726u | 126.3844u |
| gds       | 1.6480u  | 1.6480u  | 761.0636n | 763.7975n | 670.2604n | 670.2604n |
| gmb       | 36.9704u | 36.4266u | 21.8648u  | 21.8623u  | 43.7126u  | 43.7860u  |
| cdot      | 2.021e-18 | 1.585e-18 | 2.649e-18 | 2.609e-18 | 1.797e-18 | 1.878e-18 |
| cgtot     | 7.005e-16 | 7.000e-16 | 4.693e-16 | 4.692e-16 | 9.467e-16 | 9.467e-16 |
| cbtst     | 7.806e-18 | 7.806e-18 | 6.216e-18 | 6.205e-18 | 2.402e-17 | 2.402e-17 |
| cdg       | 2.021e-18 | 1.585e-18 | 2.649e-18 | 2.609e-18 | 1.797e-18 | 1.878e-18 |

Results from SPICE simulation:

i. Unloaded output (load capacitor = 0)

   GBW = 1.5 MHz., Phase Margin = 90 deg, 1% settling time = 0.39 us.

ii. Loaded output (load capacitor = 20 pF)

   GBW = 1.5 MHz., Phase Margin = 65 deg, 1% settling time = 0.48 us.
Problem 6.3-7 - Continued

CL = 0 pF

1% settling time = 0.39 us.

CL = 20 pF

1% settling time = 0.48 us.
Problem 3 - (10 points)
Small signal differential voltage gain:

By intuitive analysis methods,
\[
\frac{v_{o1}}{v_{in}} = -0.5g_{m1} \frac{g_{ds1}}{g_{ds1} + g_{ds3}}
\]
and
\[
\frac{v_{out}}{v_{o1}} = -g_{m4} \frac{g_{ds4}}{g_{ds4} + g_{ds5}}
\]
∴ \[
\frac{v_{out}}{v_{in}} = \frac{0.5g_{m1}g_{m4}}{(g_{ds1}+g_{ds3})(g_{ds4}+g_{ds5})}
\]
\[g_{m1} = \sqrt{\frac{2K_N W_1 I_{D1}}{L_1}} = \sqrt{24\cdot2\cdot4\cdot10^{-6}} \times 10^{-6} = 43.82 \mu S\]
\[g_{ds1} = \lambda N I_{D1} = 0.01\cdot10 \mu A = 0.1 \mu S, \quad g_{ds3} = \lambda p I_{D3} = 0.02\cdot10 \mu A = 0.2 \mu S\]

\[g_{m4} = \sqrt{\frac{2K_P W_4 I_{D4}}{L_4}} = \sqrt{2\cdot8\cdot10^{-6} \cdot 100} \times 10^{-6} = 126.5 \mu S\]
\[g_{ds4} = \lambda p I_{D4} = 0.02\cdot100 \mu A = 2 \mu S, \quad g_{ds5} = \lambda N I_{D5} = 0.01\cdot100 \mu A = 1 \mu S\]
∴ \[
\frac{v_{out}}{v_{in}} = \frac{0.5\cdot43.82\cdot126.5}{(0.1+0.2)(1+2)} = 3.079 \text{V/V}
\]

Output resistance:
\[R_{out} = \frac{1}{g_{ds4} + g_{ds5}} = \frac{10^6}{1+2} = 333 \text{k} \Omega\]
Dominant pole, \(p_1\):
\[|p_1| = \frac{1}{R_1C_1} \text{ where } R_1 = \frac{1}{g_{ds1}+g_{ds3}} = \frac{10^6}{0.1+0.2} = 3.33 \text{M} \Omega\]
and
\[C_1 = C_c(1+|A_v2|) = 5 \text{pF} \left(1 + \frac{g_{m4}}{g_{ds4}+g_{ds5}}\right) = 5\left(1+\frac{126.5}{3}\right) = 215.8 \text{pF}\]
\[|p_1| = \frac{10^6}{3.33\cdot2\cdot15.8} = 1.391 \text{ rads/sec} \rightarrow |p_1| = 1.391 \text{ rads/sec} = 221 \text{Hz}\]
\[G_B = \frac{0.5g_{m1}}{C_c} = \frac{0.5\cdot43.82\times10^{-6}}{5\times10^{-12}} = 4.382 \text{ Mrads/sec} \]
\[G_B = 4.382 \text{ Mrads/sec} = 0.697 \text{MHz}\]
\[\text{SR} = \frac{I_{D6}}{C_c} = \frac{10 \mu A}{5 \text{pF}} = 2 \text{V/\mu s}\]
\[P_{diss} = 10 \text{V}(140 \mu A) = 1.4 \text{mW}\]
Problem 4 - Design Problem 2 (50 points)
**NMOS Characteristics**

\[ V_{th} = 0.662 \text{ V} \]

\[ g_{ds} = \lambda_n I_D \Rightarrow 29.8824 \mu = \lambda n \times 1.1465 \text{ m} \]

\[ \Rightarrow \lambda n = 0.026 \]

\[ g_m^2 = 2 k'_n \frac{W}{L} I_D \Rightarrow \left[ 5.8228 \times 10^{-3} \right]^2 = 2 k'_n \times 100 \times 1.1465 \times 10^{-3} \]

\[ \Rightarrow k'_n = 147.86 \text{ mA/V}^2 \]

Therefore, \( \begin{cases} V_{th} = 0.662 \text{ V} \\ k'_n = 147.86 \text{ mA/V}^2 \\ \lambda n = 0.026 \end{cases} \) forms the foundation to do

the initial design by hand calculation.
\[ V_{th} = -0.864 \text{ V} \]

\[ g_{ds} = \lambda_p I_D \Rightarrow 9.14 \approx \mu = \lambda_p \times 87.3301 \mu A \]

\[ \Rightarrow \lambda_p = 0.105 \]

\[ g_m = 2k' \frac{W}{L} I_D \Rightarrow [1.009 \times 10^{-3}] = 2k' \frac{100 \times 87.3301 \times 10^{-6}} \]

\[ \Rightarrow k' = 58.3 \text{ mA/V}^2 \]

Therefore, \[ \begin{cases} V_{th} = -0.864 \text{ V} \\ k' = 58.3 \text{ mA/V}^2 \\ \lambda_p = 0.105 \end{cases} \]

Forms the basis to do the initial design by trial calculation.
**Structure**

---

**Explanation:**

1. M10, M4 set up the bias voltage at gate of M9. Then M9, M5, M7 are current mirrors to set up the bias currents for differential pair and M7 is a constant current sink load with respect to M6.

2. M1, M2 differential pair with current mirror load consisting of M3 and M4. This is the first stage of the amplifier and the gain is \( G_m = R_x \). \( G_m = G_{m1} = G_{m2} = G_m \) and \( R_x = Y_m || Y_m || Y_m \).

3. M6 is a common source amplifier with a constant sink load to get a high gain hopefully.

4. M8 acts as a resistor AC wise to create nulling zeros with M8.
1. Power consumption consideration:

\[ [2.5 - (-2.5)] I_{total} \leq 1 \text{ mW} \]

\[ \Rightarrow I_{total} \leq 200 \mu A \]

2. Phase range > 60° \( \Rightarrow \) \( C_C > 0.22 C_L \)

Now \( C_L = 10 \text{ pF} \) \( \Rightarrow \) \( C_C > 2 \text{ pF} \)

let's use \( C_C = 3 \text{ pF} \)

3. Slew Rate Consideration:

\[ SR = \frac{I_S}{C_c} = \frac{I_S}{3 \text{ pF}} \geq 10 \text{ V/\mu s} \]

\[ \Rightarrow I_S \geq 30 \mu A \]

let's use \( I_S = 30 \mu A \)

then the output stage current \( I_{Q6} \) to \( I_{Q7} \)

are choose to be \( 5 I_S = 150 \mu A \)

then we have use \( 150 \mu A \) now.
Output stage

\[ V_{o,max} = 2.5 - V_{506, (sat)} \]

\[ i_0 = \frac{58.3}{2} \times 100 (\delta V)^2 \]

\[ \delta V = 0.92 \eta \]

\[ i_e V_{o,max} = 2.273 \]

\[ V_{o,min} = -2.5 + V_{507, (sat)} \]

\[ i_0 = \frac{149.86}{2} \times 100 (\delta V)^2 \]

\[ \delta V = 0.142 \]

\[ V_{o,min} = -2.5 + 0.142 = -2.358 \]

Therefore, \[ OVSR = 2.273 + 2.358 = 4.631 > 4.5 \] (OK)

For \[ V_o = 0 \] normal bias operation.

\[ M6: i_0 = \frac{58.3}{2} \times 100 \left[ V_{506} - 0.864 \right]^2 (1 + 0.105 \times 2.5) \]

\[ \beta = \frac{58.3 \times f (V_{506} - 0.864)^2}{1.26} \Rightarrow V_{506} = 1.066 \]

\[ i_e V_{506} = 0.5 - 1.066 = 1.434 \ V \]

\[ M7: i_0 = \frac{149.86}{2} \times 100 \left[ V_{507} - 0.662 \right]^2 (1 + 0.026 \times 2.5) \]

\[ \beta = 149.86 \times f (V_{507} - 0.662)^2 \times 1.065 \Rightarrow V_{507} = 0.8 \]

\[ i_e V_{507} = -2.5 + 0.8 = -1.7 \ V \]
\[ V_{c(min)} = -2.5 + V_{DS3(COD)} + V_{BE1} \]

\[ 30 = \frac{146.86}{2} \times 20 \times V_{CE}^2 \Rightarrow V_{CE} = 0.742 \]

\[ I_S = \frac{5.83}{2} \times 1 \times V_{CE}^2 \Rightarrow V_{CE} = 0.717 \]

\[ V_{c(max)} = 2.5 - V_{DS4(COD)} + V_{TN} \]

\[ V_{c(max)} = 2.5 - 0.717 + 0.642 \]

\[ \therefore |CMR| = 3.445 + 1.64 = 4.096 > 3 \text{ (ok)} \]
(6) GB checking:

\[ GB = \frac{g_m}{C_C} \quad g_m = \sqrt{2(1478)(100)} = 0.666 \text{ mS} \]

\[ GB = \frac{0.666 \text{ mS}}{3 \text{ pF}} = 2.22 \times 10^8 \text{ pF} = 35.3 \text{ MHz} > 25 \text{ MHz} \]

(7) Avr(u) checking:

\[ g_m_1 = g_m_2 = 0.666 \text{ mS} \]

\[ R_i = R_{sc4} \parallel R_{sc2} = \frac{508.8 \text{ k} \Omega}{508.8 \text{ k} \Omega} = 508.8 \text{ k} \Omega \]

\[ g_m_3 = \sqrt{2 \times 508.8 \times 100 \times 150} = 1.32 \text{ mS} \quad \text{and} \quad R_0 = R_{sc6} \parallel R_{sc7} = 5.08 \text{ k} \Omega \]

\[ \therefore \text{Avr(u)} = \frac{g_m_1 R_2 R_3}{1.666 \times 508.8 \times 1.32} = 0.8 \]

\[ = 2.5 \times 10^4 \text{ pF} = 2.27 \times 10^4 > 10^4 \]
\( \phi = 180^\circ - \tan^{-1} \left[ \frac{6B}{|P_1|} \right] - \tan^{-1} \left[ \frac{6B}{|P_3|} \right] \)

\[ = 180^\circ - \tan^{-1} \left[ \frac{2.22 \times 10^8}{686.2} \right] - \tan^{-1} \left[ \frac{6B}{|P_3|} \right] \]

\[ = 180^\circ - 89.9^\circ - \tan^{-1} \left[ \frac{6B}{|P_3|} \right] \]

\[ \left\{ \begin{array}{c}
A_{B4} = 100 \times 10 \ \text{mm}^2, \quad A_{P3} = 100 \times 10 \ \text{mm}^2 \\
C_2 = C_{6ba} + C_{6da} + C_{6ds} + C_{7es} + C_{9ss} \approx 0.482 \ \text{pF}
\end{array} \right. \]

\[ P_{P3} = \frac{1}{2\pi R_{ce} C_e} = \frac{1}{3.14 \times 3.2 \times 10^{-3} \times 0.052 \ \text{pF}} = 100.6 \ \text{MHz} \]

\[ \phi = 180^\circ - 89.9^\circ - \tan^{-1} \left[ \frac{31.3 \ \text{MHz}}{100.6 \ \text{MHz}} \right] \]

\[ = 70.76^\circ \]
\[ \text{pole #1 (dominant pole)} = p_1 = -\frac{g_{m1}}{A/C_c} = -\frac{0.666 \times 10^{-2}}{3.32 \times 10^3 \times 3 \times 10^{12}} = -\frac{0.666 \times 5}{3.3 \times 10^5} \text{ rps} \]

\[ p_1 = 668.6 \text{ rps} \approx 1.06 \text{ kHz} \]

\[ \text{pole #2} = p_2 = -\frac{g_{m2}}{C_c} = -\frac{2 \times 10^{-3}}{10^{-11}} = -1.3 \times 10^8 \text{ rps} \]

Note: \( GB = 2.15 \times 10^8 \text{ rps} \Rightarrow |p_2| < |GB| \] Need zero-nulling to earn phase margin.

\subsection*{Zero-nulling}

Zero-pole cancelation \(\Rightarrow\) zero \(\Rightarrow\) \[ \frac{-1}{R_2 C_c - C_c/g_{m6}} \]

\[ \Rightarrow \frac{-1}{R_2 C_c - \frac{g_{m6}}{C_c}} \Rightarrow \frac{g_{m6}}{C_c} R_2 C_c = C_c + C_L \]

\[ R_2 = \frac{C_c + C_L}{g_{m6} C_c} = \frac{1.3 \times 10^{12}}{3.32 \times 10^3 \times 3 \times 10^{12}} = 3.28 \text{ k\Omega} \]

\[ V_s (\text{high}) = +1.9 \]

\[ V_s (\text{low}) = \frac{1}{0.87} \]

\[ V_L = \frac{1}{4.4} \]

\[ V_s = 3.55 \]
All bulk for NMOS → -2.5V
All bulk for PMOS → +2.5V

M3, M4, M6, M7, M13 are trimmed so that the input offset voltage is not needed. It doesn’t affect the circuit performance as long as @ \( V_i = 0, V_o = 0 \).

A) B) C) “2” points are biased at the correct operating points.
All bulk for NMOS $\rightarrow -2.5\,V$

All bulk for PMOS $\rightarrow +2.5\,V$