Problem 1 - (10 points)

This problem deals with the op amp shown in Fig. P6.5-15. All device lengths are 1µm, the slew rate is ±10V/µs, the GB is 10MHz, the maximum output voltage is +2V, the minimum output voltage is -2V, and the input common mode range is from -1V to +2V. Design all W values of all transistors in this op amp. Your design must meet or exceed the specifications. When calculating the maximum or minimum output voltages, divide the voltage drop across series transistors equally. Ignore bulk effects in this problem. When you have completed your design, find the value of the small signal differential voltage gain, $A_{vd} = \frac{v_{out}}{v_{id}}$, where $v_{id} = v_1 - v_2$ and the small signal output resistance, $R_{out}$.

Solution

1.) The slew rate will specify $I$. \[ I = C \cdot SR = 10^{-11} \cdot 10^7 = 10^{-4} = 100\mu A. \]

2.) Use $GB$ to define $W_1$ and $W_2$.

\[ GB = \frac{g_{m1}}{C} \rightarrow g_{m1} = GB \cdot C = 2\pi \cdot 10^7 \cdot 10^{-11} = 628\mu S \]

\[ \therefore W_1 = \frac{g_{m1}^2}{2K_N(0.5I)} = \frac{(628)^2}{2 \cdot 110 \cdot 50} = 35.85 \quad \Rightarrow \quad W_1 = W_2 = 36\mu m \]

3.) Design $W_{15}$ to give $V_T + 2V_{ON}$ bias for M6 and M7. $V_{ON} = 0.5V$ will meet the desired maximum output voltage specification. Therefore,

\[ v_{SG15} = V_{ON15} + |V_T| = 2(0.5V) + |V_T| \rightarrow V_{ON15} = 1V = \sqrt{\frac{2I}{K_P W_{15}}} \]

\[ \therefore W_{15} = \frac{2I}{K_P V_{ON15}^2} = \frac{2 \cdot 100}{50 \cdot 1^2} = 4\mu m \quad \Rightarrow \quad W_{15} = 4\mu m \]

4.) Design $W_3$, $W_4$, $W_6$ and $W_7$ to have a saturation voltage of 0.5V with 1.5I current.

\[ W_3 = W_4 = W_6 = W_7 = \frac{2(1.5I)}{K_P V_{ON}^2} = \frac{2 \cdot 150}{50 \cdot 0.5^2} = 24\mu m \quad \Rightarrow \quad W_3 = W_4 = W_6 = W_7 = 24\mu m \]
Problem 6.5-15 – Continued

5.) Next design $W_8$, $W_9$, $W_{10}$ and $W_{11}$ to meet the minimum output voltage specification. Note that we have not taken advantage of smallest minimum output voltage because a normal cascode current mirror is used which has a minimum voltage across it of $V_T + 2V_{ON}$. Therefore, setting $V_T + 2V_{ON} = 1V$ gives $V_{ON} = 0.15V$. Using worst case current, we choose $1.5I$. Therefore,

$$W_8 = W_9 = W_{10} = W_{11} = \frac{2(1.5I)}{K_NV_{ON}^2} = \frac{2 \cdot 1.5 \cdot 10^{-11}}{0.15^2} = 121\mu m \Rightarrow W_8 = W_9 = W_{10} = W_{11} = 121\mu m$$

6.) Check the maximum ICM voltage.

$$V_{ic}(\text{max}) = V_{DD} + V_{SD3}(\text{sat}) + V_{TN} = 3V - 0.5 + 0.7 = 3.2V \text{ which exceeds spec.}$$

7.) Use the minimum ICM voltage to design $W_5$.

$$V_{ic}(\text{min}) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1} = -3 + V_{DS5}(\text{sat}) + \left(\frac{2.5V}{\sqrt{110\cdot 0.36}} + 0.7\right) = -1V$$

$$\therefore \quad V_{DS5}(\text{sat}) = 1.141 \quad \rightarrow \quad W_5 = \frac{2I}{K_NV_{DS5}(\text{sat})^2} = 1.39\mu m = 1.4\mu m$$

Also, let $W_{12} = W_{13} = W_5 \quad \Rightarrow \quad W_{12} = W_{13} = W_5 = 1.4\mu m$

8.) $W_{14}$ is designed as

$$W_{14} = W_3 = \frac{I_{14}}{I_3} = \frac{24\mu m}{1.5I} = 16\mu m \quad \Rightarrow \quad W_{14} = 16\mu m$$

Now, calculate the op amp small-signal performance.

$$R_{out} \approx r_{ds11}g_{m9}r_{ds9}g_{m7}r_{ds7}(r_{ds2}||r_{ds4})$$

$$g_{m9} = \sqrt{2}K_N I_W = 1632\mu S, \quad r_{ds9} = r_{ds11} = \frac{25V}{100\mu A} = 0.25\Omega,$$

$$g_{m7} = \sqrt{2}K_P I_W = 490\mu S, \quad r_{ds7} = \frac{20V}{100\mu A} = 0.2\Omega, \quad r_{d2} = \frac{25V}{50\mu A} = 0.5\Omega$$

$$r_{ds4} = \frac{150\mu A}{0.1333\Omega} = 0.25\Omega \Rightarrow R_{out} \approx 102\Omega || 10.31\Omega = 9.3682\Omega$$

$$A_{vd} = (2+k) g_{m1}R_{out}, \quad k = \frac{102\Omega}{(r_{ds2}||r_{ds4})g_{m7}r_{ds7}'} = 9.888, \quad g_{m1} = \sqrt{K_N I_W} = 629\mu S$$

$$\therefore \quad A_{vd} = (0.5459)(629\mu S)(9.3682\Omega) = 3.217V/V \quad \Rightarrow \quad A_{vd} = 3.217V/V$$
6.28

If the bias current level of 741 input stage is doubled, then from (6.134), \( G_m = \frac{1}{2.7 \times 10^3} \)

From (6.138),

\[
R_{o1} = R_{out} \mid_{Q_4} \parallel \left[ R_{out} \mid_{Q_6} \right] = 2 \frac{R_{o4}}{R_{o6}} \parallel (1 + g_m \parallel (1 \times 10^3))
\]

Using \( \eta_{npn} = 2 \times 10^{-4} \), \( \eta_{pnp} = 5 \times 10^4 \) and \( |I_C| = 19.4 A \), we have

\[
\frac{R_{o4}}{R_{o6}} = \frac{1}{\eta g_m} = \frac{10^4}{2 \times 26} = 2.74 \text{ M}\Omega
\]

\[
R_{o6} = \frac{10^4}{2} \times \frac{26}{19 \times 10^{-3}} = 6.84 \text{ M}\Omega
\]

\( g_m \parallel 1 \times 10^3 = 0.73 \)

\( R_{o1} = (5.48) \parallel (6.84 \times 1.73) \text{ M}\Omega = 3.75 \text{ M}\Omega \)

741 equivalent

\[
\begin{align*}
1.35 \text{ M}\Omega & \quad 3.75 \text{ M}\Omega \quad 5.7 \text{ M}\Omega \quad 83 \text{ k}\Omega \quad 9.1 \text{ M}\Omega \\
\frac{V_{id}}{2.7} & \quad \frac{V_{i_2}}{14.7}
\end{align*}
\]

\[
3.75 \parallel 5.7 \quad 2.26 \text{ M}\Omega \quad 83 \text{ k}\Omega \parallel 9.1 \text{ M} = 82 \text{ k}\Omega
\]

\[
A_v = \frac{2260}{2.7} \cdot \frac{0.147}{836 \times 558} = 4.68,000
\]
If the 100 kΩ emitter resistor of Q₁₇ is removed, then in

\[ R_{eq1} = r_{π17} + \frac{B}{g_m} \times 250 \times 26 = 11.8 \, kΩ \times 0.55 \]

\[ R_{i2} = r_{π16} + (1 + B_0) \left( r_{π17} / 50 \, kΩ \right) \]

\[ = 406 \, kΩ + 251 \times 9.55 \, kΩ \]

\[ = 2.8 \, MΩ \]

From (6.146)

\[ g_{m2} = g_{m17} = \frac{0.55}{26} = \frac{1}{47.3} \, Ω \]

From (6.147)

\[ R_{02} = \frac{r_{013b} \parallel r_{017}}{g_{m}} \]

\[ r_{013b} = \frac{1}{\frac{1}{g_{m}} \times 5} = \frac{10^4}{26} = 94.5 \, kΩ \]

\[ r_{017} = \frac{1}{\frac{1}{g_{m}} \times 2} = \frac{10^4}{26} = 236 \, kΩ \]

\[ \therefore R_{02} = 67.5 \, kΩ \]

\[ A_v = \frac{1980 \times 67}{5.4 \times 0.047} \]

\[ = 523,000 \]

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Minimum CM input voltage:

The circuit ceases to function correctly when Q₃ and Q₄ saturate.

Q₁₇ and Q₄ operate in the F.A.R. when,

\[ V_{EC₃} > V_{CE(sat)} \]

\[ V_{E₃} = V_{IC} - V_{BE₁} \]

\[ V_{C₃} = -V_{EE} + V_{BE₅} + V_{BE₁} + I_{C₄} \, (1k) \]

\[ V_{EC₃} = V_{IC} - V_{BE₁} - (-V_{EE}) - V_{BE₅} - V_{BE₁} > V_{CE(sat)} \]

\[ V_{IC} > -V_{EE} + V_{BE₁} + V_{BE₅} + V_{BE₁} + V_{CE(sat)} \]

Maximum CM input voltage:

Q₁ and Q₂ operate in the F.A.R. when

\[ V_{CE₁} > V_{CE(sat)} \]

\[ V_{C₁} = V_{CC} - |V_{BE₈}| \]

\[ V_{E₁} = V_{IC} - V_{BE₁} \]

\[ V_{CE₁} = V_{CC} - |V_{BE₈}| - V_{IC} + V_{BE₁} > V_{CE(sat)} \]

Assume \( V_{BE₁} = |V_{BE₈}| \)

Then \( V_{IC} < V_{CC} - V_{CE(sat)} \)
### DC Transfer Curves

<table>
<thead>
<tr>
<th>VOLT (V)</th>
<th>27.000X Temp 27.000X</th>
<th>27.000X Temp 27.000X</th>
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</tr>
<tr>
<td>-A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>+B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-B</td>
<td></td>
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### Operating Point Information

<table>
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<tr>
<th>Mode</th>
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<th>+Voltage Node</th>
<th>+Voltage Node</th>
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<tbody>
<tr>
<td>+3</td>
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<td>+1.433V+01</td>
<td>-1.490V+01</td>
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<tr>
<td>+6</td>
<td>+1.107V+00</td>
<td>+1.441V+01</td>
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<td>-2.361V-03</td>
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<tr>
<td>+25</td>
<td>+3.509V+03</td>
<td>+1.500V+01</td>
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</tr>
</tbody>
</table>

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**POWER SUPPLIES**

VCC: 100 V
VSS: 200 V

**INPUT STAGE**

Q1: 7 V, 8.10, NPN
Q2: 7.9, 11, NPN
Q3: 12 V, 6, 10, PNP
Q4: 16 V, 6, 11, PNP
Q5: 12 V, 13, 14, NPN
Q6: 16 V, 13, 15, NPN
Q7: 100 V, 12, 13, NPN
Q8: 7 V, 7, 100, PNP
Q9: 6 V, 7, 100, PNP
Q10: 6 V, 4, 5, NPN
Q11: 4 V, 4, 200, NPN
Q12: 3 V, 3, 100, PNP
R1: 14, 200, 1X
R2: 15, 200, 1X
R3: 13, 200, 50K
R5: 3, 4, 39K
R4: 5, 200, 5K

**BIPOLAR GAIN STAGE**

Q13B: 19, 3, 100, PNP
Q16: 100 V, 16, 17, NPN
Q17: 19 V, 17, 18, NPN
R8: 18, 200, 100
R9: 17, 200, 50K

**OUTPUT STAGE**

Q14A: 20 V, 3, 100, PNP
Q14: 100 V, 20, 25, NPN, 3
Q18: 20 V, 21, 22, NPN
Q19: 20 V, 20, 21, NPN
Q20: 200 V, 22, 23, PNP, 3
Q23: 200 V, 19, 22, PNP
R6: 25 V, 9, 27
R7: 23 V, 9, 22
R10: 21 V, 22, 40K

**VI1**

V0: 0
.MODEL NPN NPN BP=250 IS=5E-15 VAF=130
.MODEL PNP PNP BP=50 IS=2E-15 VAF=50
.MODEL PNP PNP BP=50 IS=0.5E-15 VAF=50
.MODEL PNP PNP BP=50 IS=1.5E-15 VAF=50
.OPTIONS MFCOMP NONC
.WIDTH OUT=50
.GP
.DC VI1 -15 15 0.5

* ASSUMING VCC(HAP) = 0.2 V AND VSS(NCH) = 8.7 V.
* THE HAMCALCULATIONS PREDICT A COMMON-MODE RANGE OF
* +13.7 V < VCC < 14.8 V
* IN THE VOLTAGE-FOLLOWER CONFIGURATION, VO = VI = VCC
* AS LONG AS THE AMPLIFIER IS WORKING CORRECTLY.
* THE RESULTS OF THIS SIMULATION SHOW THAT
* VO = VI FOR THE FOLLOWING RANGE:
* +13 V < VO < +14.5 V
* THEREFORE, THIS SIMULATION SHOWS THAT THE
* COMMON MODE INPUT RANGE IS:
* +13 V < (VO = VI = VCC) < 14.5 V
* WHICH IS CLOSE TO THEResult
* PREDICTED BY HAMCALCULATIONS.

**PLOT DC V(9)**

**END**
Problem 5 – (10 points)

A two-stage, BiCMOS op amp is shown. For the PMOS transistors, the model parameters are \( K_F' = 50 \mu A/V^2 \), \( V_{TP} = -0.7 \) V and \( \lambda_P = 0.05 V^{-1} \). For the NPN BJTs, the model parameters are \( \beta_F = 100 \), \( V_{CE}(sat) = 0.2 \) V, \( V_A = 25 \) V, \( V_I = 26 mV \), \( I_s = 10 fA \) and \( n=1 \). (a.) Identify which input is positive and which input is negative. (b.) Find the numerical values of differential voltage gain magnitude, \( |A_v(0)| \), \( GB \) (in Hertz), the slew rate, \( SR \), and the location of the RHP zero. (c.) Find the numerical value of the maximum and minimum input common mode voltages.

Solution

(a.) The plus and minus signs on the schematic show which input is positive and negative.

(b.) The differential voltage gain, \( A_v(0) \), is given as

\[
A_v(0) = \frac{g_{m1}}{g_{ds2} + g_{o4} + g_{\pi6}} \quad \frac{g_{m6}}{g_{ds7} + g_{o6}} \quad g_{m1} = g_{m2} = \sqrt{2 \cdot 50 \cdot 25 \cdot 10} = 158.1 \mu S
\]

\[
r_{ds2} = \frac{20}{25 \mu A} = 0.8 M\Omega, \quad r_{o4} = \frac{V_A}{I_C} = \frac{25}{25 \mu A} = 1 M\Omega, \quad g_{m6} = \frac{I_C}{V_I} = \frac{100 \mu A}{26 mV} = 3846 \mu S
\]

\[
r_{\pi6} = \frac{\beta_F}{g_{m6}} = 26 k\Omega, \quad r_{ds7} = \frac{1}{\lambda p I_D} = \frac{20}{100 \mu A} = 0.2 M\Omega \quad \text{and} \quad r_{o6} = \frac{1}{\lambda p I_D} = \frac{20}{100 \mu A} = 0.25 M\Omega
\]

\[|A_v(0)| = [158.1(0.81||1||0.026)][3846(0.2||0.25)] = 3.888 \cdot 427.36 = 1659.6 V/V \]

\[GB = \frac{g_{m1} C_c}{5 pF} = 31.62 \times 10^6 \text{ rads/sec} \rightarrow GB = 5.0325 \text{MHz} \]

\[SR = \frac{50 \mu A}{5 pF} = 10 V/\mu s\]

\[\text{RHP zero} = \frac{g_{m6} C_c}{5 pF} = \frac{3.846 mS}{5 pF} = 769.24 \times 10^6 \text{ rads/sec} \cdot (122 \text{MHz})\]

(c.) The maximum input common mode voltage is given as

\[v_{icm^+} = V_{CC} - V_{DS5(sat)} - V_{SG1} = 1.5 - \sqrt{\frac{2.50}{50 \cdot 10}} - 0.7 - \sqrt{\frac{2.25}{50 \cdot 10}} = 0.8 - 0.447 - 0.316 = 0.0367 V\]

\[v_{icm^-} = -1.5 + V_{BE3} - V_{T1} = -1.5 + V_t \ln\left(\frac{25 \mu A}{10 fA}\right) - 0.7 = -2.2 + 0.5626 = -1.6374 V\]