LECTURE 130 – COMPENSATION OF OP AMPS-II
(READING: GHLM – 638-652, AH – 260-269)

INTRODUCTION

The objective of this presentation is to continue the ideas of the last lecture on compensation of op amps.

Outline

- Compensation of Op Amps
  - General principles
  - Miller, Nulling Miller
  - Self-compensation
  - Feedforward
- Summary

Conditions for Stability of the Two-Stage Op Amp (Assuming $p_3 \geq GB$)

- Unity-gainbandwith is given as:

$$GB = A_v(0)\cdot|p_1| = \left(\frac{g_{mI}g_{mII}R_IR_{II}}{g_{mII}R_IR_{II}C_c}\right) = \frac{g_{mI}}{C_c} = \left(\frac{g_{m1}g_{m2}R_1R_2}{g_{m2}R_1R_2C_c}\right) = \frac{g_{m1}}{C_c}$$

- The requirement for 45° phase margin is:

$$\pm 180° - \mathrm{Arg}[AF] = \pm 180° - \tan^{-1}\left(\frac{\omega}{|p_1|}\right) - \tan^{-1}\left(\frac{\omega}{|p_2|}\right) - \tan^{-1}\left(\frac{\omega}{z}\right) = 45°$$

Let $\omega = GB$ and assume that $z \geq 10GB$, therefore we get,

$$\pm 180° - \tan^{-1}\left(\frac{GB}{|p_1|}\right) - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}\left(\frac{GB}{z}\right) = 45°$$

$$135° \approx \tan^{-1}(A_v(0)) + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + \tan^{-1}(0.1) = 90° + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + 5.7°$$

$$39.3° \approx \tan^{-1}\left(\frac{GB}{|p_2|}\right) \Rightarrow \frac{GB}{|p_2|} = 0.818 \Rightarrow \boxed{|p_2| \geq 1.22GB}$$

- The requirement for 60° phase margin:

$$\boxed{|p_2| \geq 2.2GB \text{ if } z \geq 10GB}$$

- If 60° phase margin is required, then the following relationships apply:

$$\frac{g_{m6}}{C_c} > \frac{10g_{m1}}{C_c} \quad \Rightarrow \quad \boxed{g_{m6} > 10g_{m1}} \qquad \text{and} \quad \frac{g_{m6}}{C_2} > \frac{2.2g_{m1}}{C_c} \quad \Rightarrow \quad \boxed{C_c > 0.22C_2}$$

Controlling the Right-Half Plane Zero

Why is the RHP zero a problem?

Because it boosts the magnitude but lags the phase - the worst possible combination for stability.

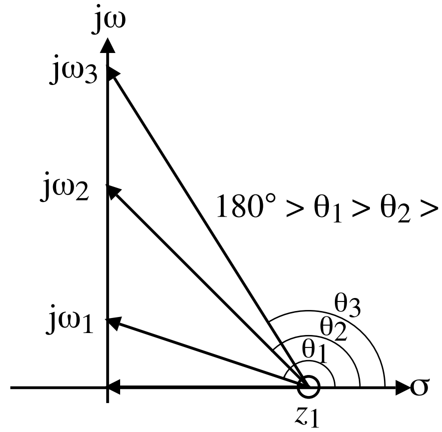


Fig. 430-01

Solution of the problem:

If zeros are caused by two paths to the output, then eliminate one of the paths.

Use of Buffer to Eliminate the Feedforward Path through the Miller Capacitor

Model:

The transfer function is given by the following equation,

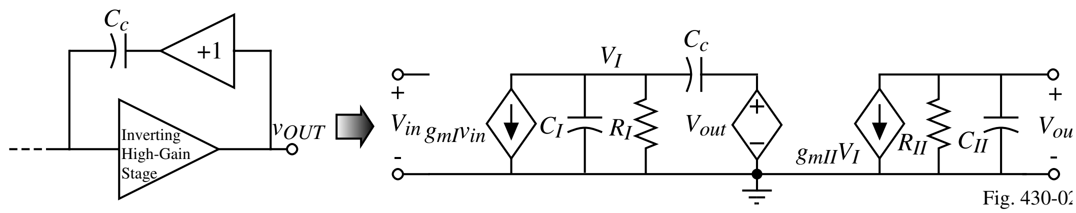


Fig. 430-02

$$\frac{V_o(s)}{V_{in}(s)} = \frac{(g_{mI})(g_{mII})(R_I)(R_{II})}{1 + s[R_IC_I + R_{II}C_{II} + R_IC_c + g_{mII}R_IR_{II}C_c] + s^2[R_IR_{II}C_{II}(C_I + C_c)]}$$

Using the technique as before to approximate p_1 and p_2 results in the following

$$p_1 \cong \frac{-1}{R_IC_I + R_{II}C_{II} + R_IC_c + g_{mII}R_IR_{II}C_c} \cong \frac{-1}{g_{mII}R_IR_{II}C_c}$$

and

$$p_2 \cong \frac{-g_{mII}C_c}{C_{II}(C_I + C_c)}$$

Comments:

Poles are approximately what they were before with the zero removed.

For 45° phase margin, $|p_2|$ must be greater than GB

For 60° phase margin, $|p_2|$ must be greater than $1.73GB$

Use of Buffer with Finite Output Resistance to Eliminate the RHP Zero

Assume that the unity-gain buffer has an output resistance of R_o.

Model:

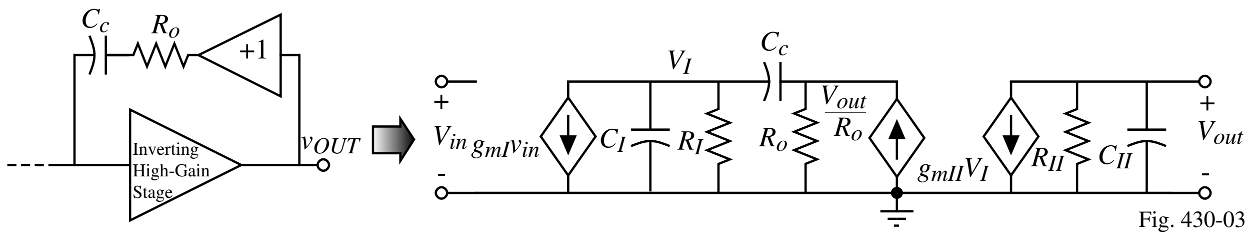


Fig. 430-03

It can be shown that if the output resistance of the buffer amplifier, R_o, is not neglected that another pole occurs at,

$$p_4 \cong \frac{-1}{R_o[C_IC_c/(C_I + C_c)]}$$

and a LHP zero at

$$z_2 \cong \frac{-1}{R_oC_c}$$

Closer examination shows that if a resistor, called a *nulling resistor*, is placed in series with C_c that the RHP zero can be eliminated or moved to the LHP.

Use of Nulling Resistor to Eliminate the RHP Zero (or turn it into a LHP zero)†

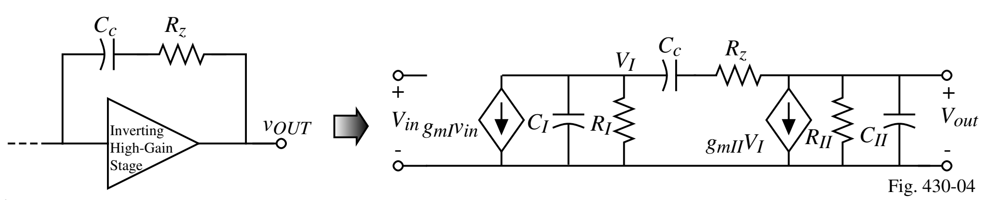


Fig. 430-04

Nodal equations:

$$g_{mI}V_{in} + \frac{V_I}{R_I} + sC_IV_I + \left(\frac{sC_c}{1 + sC_cR_z}\right)(V_I - V_{out}) = 0$$

$$g_{mII}V_I + \frac{V_o}{R_{II}} + sC_{II}V_{out} + \left(\frac{sC_c}{1 + sC_cR_z}\right)(V_{out} - V_I) = 0$$

Solution:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a\{1 - s[(C_c/g_{mII}) - R_zC_c]\}}{1 + bs + cs^2 + ds^3}$$

where

$a = g_{mI}g_{mII}R_IR_{II}$

$b = (C_{II} + C_c)R_{II} + (C_I + C_c)R_I + g_{mII}R_IR_{II}C_c + R_zC_c$

$c = [R_IR_{II}(C_IC_{II} + C_cC_I + C_cC_{II}) + R_zC_c(R_IC_I + R_{II}C_{II})]$

$d = R_IR_{II}R_zC_IC_{II}C_c$

† W.J. Parrish, "An Ion Implanted CMOS Amplifier for High Performance Active Filters", Ph.D. Dissertation, 1976, Univ. of CA., Santa Barbara.

Use of Nulling Resistor to Eliminate the RHP - Continued

If R_z is assumed to be less than R_I or R_{II} and the poles widely spaced, then the roots of the above transfer function can be approximated as

$$p_1 \cong \frac{-1}{(1+g_{mII}R_{II})R_IC_c} \cong \frac{-1}{g_{mII}R_{II}R_IC_c}$$

$$p_2 \cong \frac{-g_{mII}C_c}{C_IC_{II}+C_cC_I+C_cC_{II}} \cong \frac{-g_{mII}}{C_{II}}$$

$$p_4 = \frac{-1}{R_zC_I}$$

(p_3 has been used previously for the mirror pole so we choose p_4 for the nulling resistor pole)

and

$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)}$$

Note that the zero can be placed anywhere on the real axis.

Conceptual Illustration of the Nulling Resistor Approach

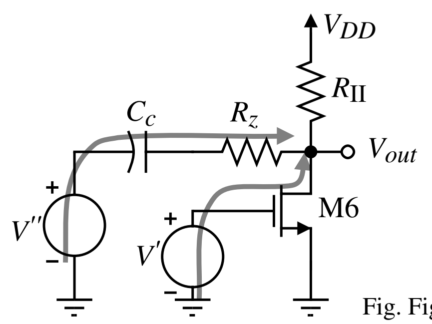


Fig. Fig. 430-05

The output voltage, V_{out}, can be written as

$$V_{out} = \frac{-g_{m6}R_{II}\left(R_z+\frac{1}{sC_c}\right)}{R_{II}+R_z+\frac{1}{sC_c}}V' + \frac{R_{II}}{R_{II}+R_z+\frac{1}{sC_c}}V'' = \frac{-R_{II}\left[g_{m6}R_z+\frac{g_{m6}}{sC_c}-1\right]}{R_{II}+R_z+\frac{1}{sC_c}}V$$

when $V = V' = V''$.

Setting the numerator equal to zero and assuming $g_{m6} = g_{mII}$ gives,

$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)}$$

A Design Procedure that Allows the RHP Zero to Cancel the Output Pole, p_2

We desire that $z_1 = p_2$ in terms of the previous notation.

Therefore,

$$\frac{1}{C_c(1/g_{mII} - R_z)} = \frac{-g_{mII}}{C_{II}}$$

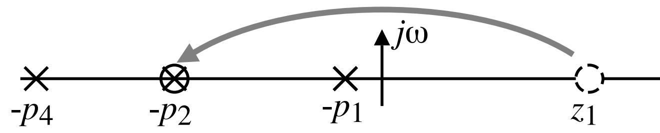


Fig. 430-06

The value of R_z can be found as

$$R_z = \left(\frac{C_c + C_{II}}{C_c}\right)(1/g_{mII})$$

With p_2 canceled, the remaining roots are p_1 and p_4(the pole due to R_z) . For unity-gain stability, all that is required is that

$$|p_4| > A_v(0)|p_1| = \frac{A_v(0)}{g_{mII}R_{II}R_IC_c} = \frac{g_{mI}}{C_c}$$

and

$$(1/R_zC_I) > (g_{mI}/C_c) = GB$$

Substituting R_z into the above inequality and assuming $C_{II} >> C_c$ results in

$$C_c > \sqrt{\frac{g_{mI}}{g_{mII}}C_IC_{II}}$$

This procedure gives excellent stability for a fixed value of C_{II} ($\approx C_L$).

Unfortunately, as C_L changes, p_2 changes and the zero must be readjusted to cancel p_2.

Increasing the Magnitude of the Output Pole[†]

The magnitude of the output pole , p_2, can be increased by introducing gain in the Miller capacitor feedback path. For example,

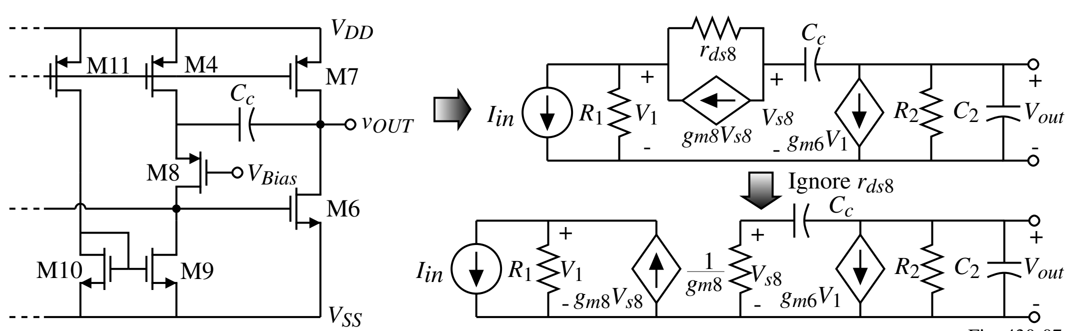


Fig. 430-07

The resistors R_1 and R_2 are defined as

$$R_1 = \frac{1}{g_{ds2} + g_{ds4} + g_{ds9}} \qquad \text{and } R_2 = \frac{1}{g_{ds6} + g_{ds7}}$$

where transistors M2 and M4 are the output transistors of the first stage.

Nodal equations:

$$I_{in} = G_1V_1 - g_{m8}V_{s8} = G_1V_1 - \left(\frac{g_{m8}sC_c}{g_{m8} + sC_c}\right)V_{out} \quad \text{and} \quad 0 = g_{m6}V_1 + \left[G_2 + sC_2 + \frac{g_{m8}sC_c}{g_{m8} + sC_c}\right]V_{out}$$

† B.K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," *IEEE J. of Solid-State Circuits*, Vol. SC-18, No. 6 (Dec. 1983) pp. 629-633.

Increasing the Magnitude of the Output Pole - Continued

Solving for the transfer function V_{out}/I_{in} gives,

$$\frac{V_{out}}{I_{in}} = \left(\frac{-g_{m6}}{G_1G_2}\right)\left[\frac{\left(1+\frac{sC_c}{g_{m8}}\right)}{1+s\left[\frac{C_c}{g_{m8}}+\frac{C_2}{G_2}+\frac{C_c}{G_2}+\frac{g_{m6}C_c}{G_1G_2}\right]+s^2\left(\frac{C_cC_2}{g_{m8}G_2}\right)}\right]$$

Using the approximate method of solving for the roots of the denominator gives

$$p_1 = \frac{-1}{\frac{C_c}{g_{m8}}+\frac{C_c}{G_2}+\frac{C_2}{G_2}+\frac{g_{m6}C_c}{G_1G_2}} \approx \frac{-6}{g_{m6}r_{ds}{}^2C_c}$$

and

$$p_2 \approx \frac{-\frac{g_{m6}r_{ds}{}^2C_c}{6}}{\frac{C_cC_2}{g_{m8}G_2}} = \frac{g_{m8}r_{ds}{}^2G_2}{6}\left(\frac{g_{m6}}{C_2}\right) = \left(\frac{g_{m8}r_{ds}}{3}\right)|p_2'|$$

where all the various channel resistance have been assumed to equal r_{ds} and p_2’ is the output pole for normal Miller compensation.

Result:

Dominant pole is approximately the same and the output pole is increased by $\approx g_mr_{ds}$.

Concept Behind the Increasing of the Magnitude of the Output Pole

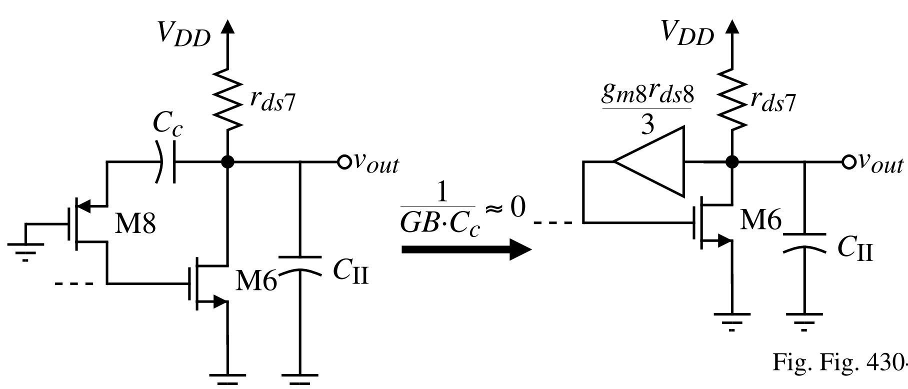


Fig. Fig. 430-08

$$R_{out} = r_{ds7}||\left(\frac{3}{g_{m6}g_{m8}r_{ds8}}\right) \approx \frac{3}{g_{m6}g_{m8}r_{ds8}}$$

Therefore, the output pole is approximately,

$$|p_2| \approx \frac{g_{m6}g_{m8}r_{ds8}}{3C_{II}}$$

Besides, the common gate amplifier stops the feedforward path preventing the RHP zero.

FEEDFORWARD COMPENSATION

Use two parallel paths to achieve a LHP zero for lead compensation purposes.

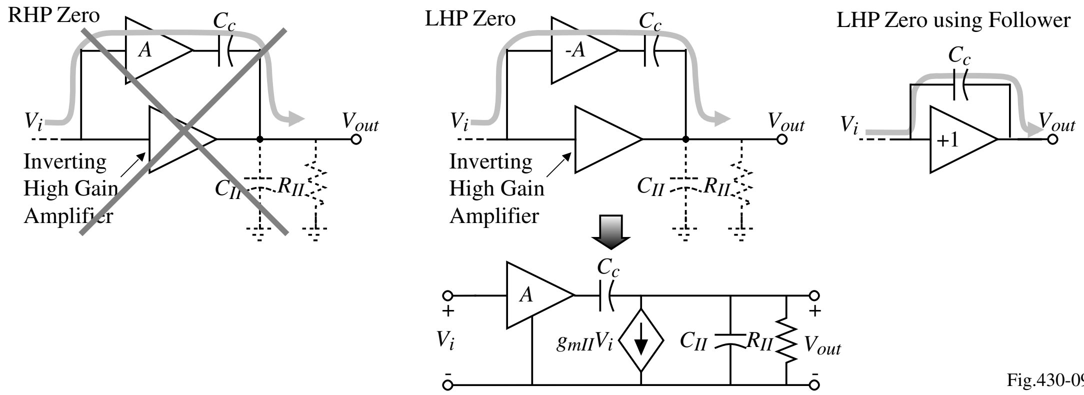


Fig.430-09

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{AC_c}{C_c + C_{II}}\left(\frac{s + g_{mII}/AC_c}{s + 1/[R_{II}(C_c + C_{II})]}\right)$$

To use the LHP zero for compensation, a compromise must be observed.

- Placing the zero below GB will lead to boosting of the loop gain that could deteriorate the phase margin.
- Placing the zero above GB will have less influence on the leading phase caused by the zero.

Note that a source follower is a good candidate for the use of feedforward compensation.

SELF-COMPENSATED OP AMPS

Self compensation occurs when the load capacitor is the compensation capacitor (can never be unstable for resistive feedback)

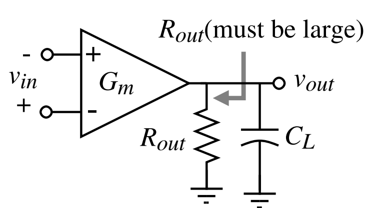
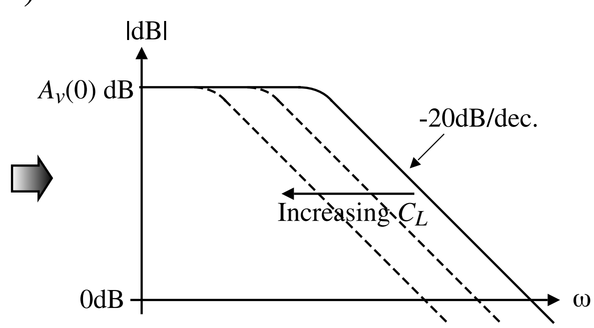


Fig. 430-10



Voltage gain:

$$\frac{v_{out}}{v_{in}} = A_v(0) = G_m R_{out}$$

Dominant pole:

$$p_1 = \frac{-1}{R_{out}C_L}$$

Unity-gainbandwidth:

$$GB = A_v(0)\cdot|p_1| = \frac{G_m}{C_L}$$

Stability:

Large load capacitors simply reduce GB but the phase is still 90° at GB.

SUMMARY

Compensation

- Designed so that the op amp with unity gain feedback (buffer) is stable
- Types
  - Miller
  - Miller with nulling resistors
  - Self Compensating
  - Feedforward

