LECTURE 140 – SIMPLE CMOS OP AMPS
(READING: Text-GHLM – 425-434, 453-454, AH – 249-253)

INTRODUCTION

The objective of this presentation is:

1.) Illustrate the analysis of CMOS op amps

2.) Prepare for the design of CMOS op amps

Outline

- Simple CMOS Op Amps
  - Two-stage
  - Folded-cascode
- Summary

SIMPLE TWO-STAGE CMOS OP AMPS

Two-Stage CMOS Op Amp

Circuit:

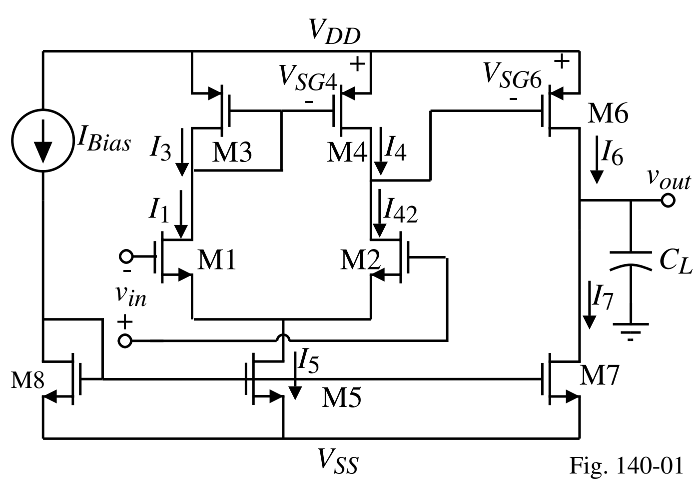


Fig. 140-01

DC Conditions:

$I_5 = I_{bias}$, $I_1 = I_2 = 0.5I_5 = 0.5I_{bias}$,

$I_7 = I_6 = nI_{Bias}$

$V_{icm}(\max) = V_{DD} - V_{SG3} + V_{T1}$

$V_{icm}(\min) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1}$

$V_{out}(\max) = V_{DD} - V_{SD6}(\text{sat})$

$V_{out}(\min) = V_{SS} + V_{DS7}(\text{sat})$

Notice that the output stage is class A

$$\therefore\ I_{sink} = I_7 \text{ and } I_{source} = \frac{K_N' W_6}{2L_6}(V_{DD}-V_{SS}-V_T)^2 - I_7$$

DC Balance Conditions for the Two-Stage Op Amp

For best performance, keep all transistors in saturation.

M4 is the only transistor that cannot be forced into saturation by internal connections or external voltages.

Therefore, we develop conditions to force M4 to be in saturation.

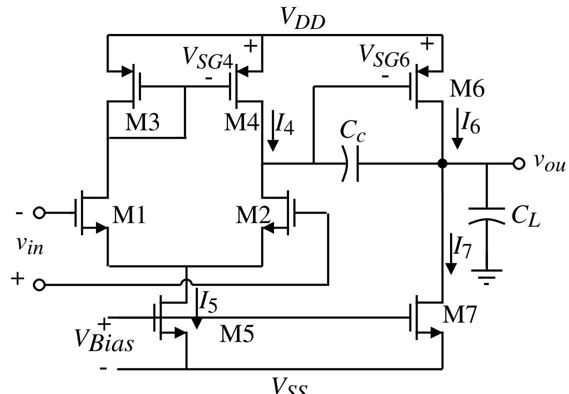


Fig. 140-02

1.) First *assume* that $V_{SG4} = V_{SG6}$. This will cause "proper mirroring" in the M3-M4 mirror. Also, the gate and drain of M4 are at the same potential so that M4 is "guaranteed" to be in saturation.

2.) Let $S_i \equiv \frac{W_i}{L_i}$, *if* $V_{SG4} = V_{SG6}$, then $I_6 = \left(\frac{S_6}{S_4}\right) I_4$

3.) However, $I_7 = \left(\frac{S_7}{S_5}\right) I_5 = \left(\frac{S_7}{S_5}\right)(2I_4)$

4.) For balance, I_6 must equal I_7 $\Rightarrow$ $\boxed{\frac{S_6}{S_4} = \frac{2S_7}{S_5}}$ which is called the "balance conditions"

5.) So if the balance conditions are satisfied, then $V_{DG4} = 0$ and M4 is saturated.

Small-Signal Performance of the Two-Stage CMOS Op Amp

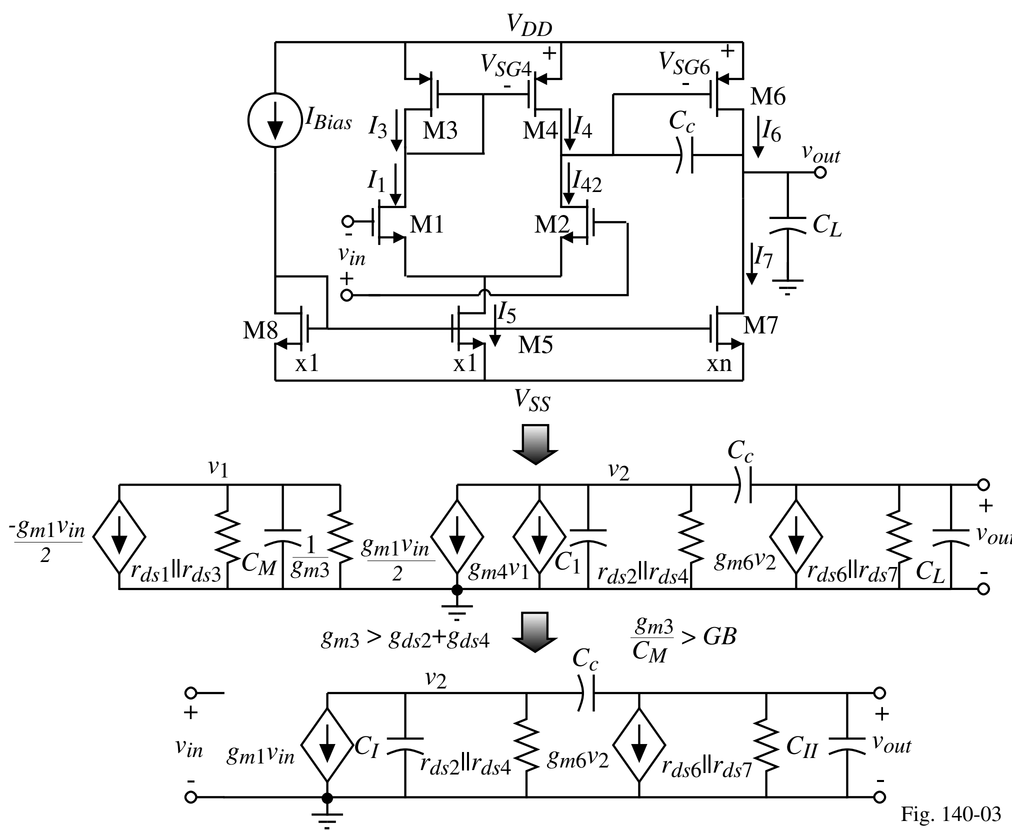


Fig. 140-03

Small-Signal Performance of the Two-Stage CMOS Op Amp

Summary of the small signal performance:

Midband performance-

$$A_o = g_{mI}g_{mII}R_IR_{II} \approx g_{m1}g_{m6}(r_{ds2}||r_{ds4})(r_{ds6}||r_{ds7}), \quad R_{out} = r_{ds6}||r_{ds7}, \quad R_{in} = \infty$$

Roots-

$$\text{Zero} = \frac{g_{mII}}{C_c} = \frac{g_{m6}}{C_c}$$

$$\text{Poles at} \quad p_1 \approx \frac{-1}{g_{mII}R_IR_{II}C_c} = \frac{-(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m6}C_c} \quad \text{and} \quad p_2 \approx \frac{-g_{mII}}{C_{II}} \approx \frac{-g_{m6}}{C_L}$$

Assume that $g_{m1} = 100\mu S$, $g_{m6} = 1mS$, $r_{ds2} = r_{ds4} = 2M\Omega$ $r_{ds6} = r_{ds7} = 0.5M\Omega$, $C_c = 5pF$ and $C_L = 10pF$:

$$A_o = (100\mu S)(1M\Omega)(1000\mu S)(0.25M\Omega) = 25{,}000V/V, \quad R_{in} = \infty, \; R_{out} = 250k\Omega$$

Zero = 1000μS/5pF = $2\text{x}10^8$ rads/sec or 31.83MHz,

$$p_1 = \frac{-1}{(1mS)(1M\Omega)(0.25M\Omega)(5pF)}$$

= -800 rads/sec or 127.3Hz,

GB = 3.178MHz

and p_2 = (-1000μS/10pF) = 10^8 rads/sec or 15.915MHz

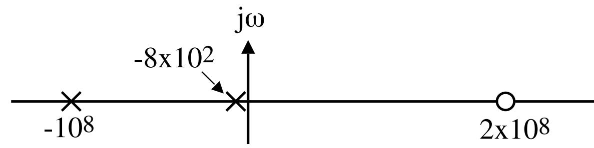
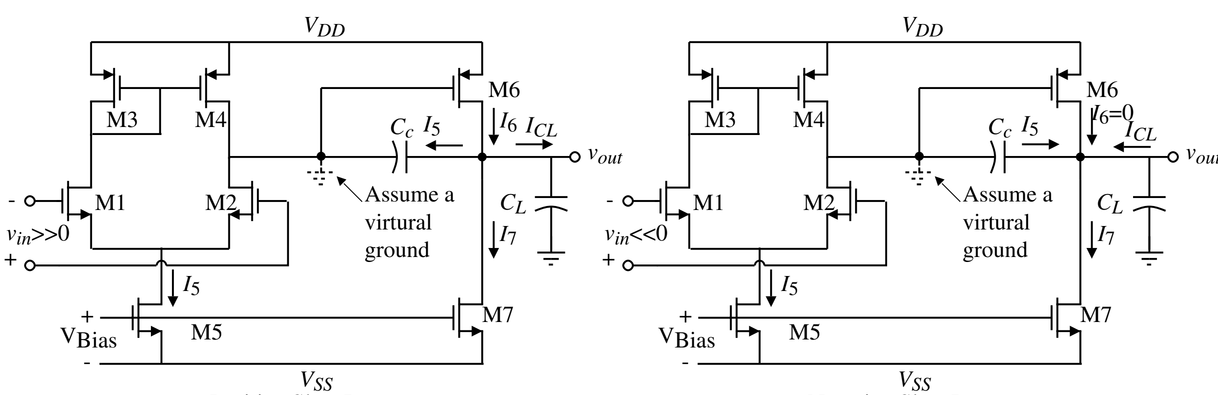


Fig. 140-04

Slew Rate of a Two-Stage CMOS Op Amp

Remember that slew rate occurs when currents flowing in a capacitor become limited and is given as

$$I_{lim} = C\frac{dv_C}{dt} \quad \text{where } v_C \text{ is the voltage across the capacitor } C.$$



Positive Slew Rate   Negative Slew Rate   Fig. 140-05

$$SR^+ = \min\left[\frac{I_5}{C_c}, \frac{I_6-I_5-I_7}{C_L}\right] = \frac{I_5}{C_c} \text{ because } I_6>>I_5 \qquad SR^- = \min\left[\frac{I_5}{C_c}, \frac{I_7-I_5}{C_L}\right] = \frac{I_5}{C_c} \text{ if } I_7>>I_5.$$

Therefore, if C_L is not too large and if I_7 is significantly greater than I_5, then the slew rate of the two-stage op amp should be,

$$SR = \frac{I_5}{C_c}$$

Folded Cascode, CMOS Op Amp

Circuit:

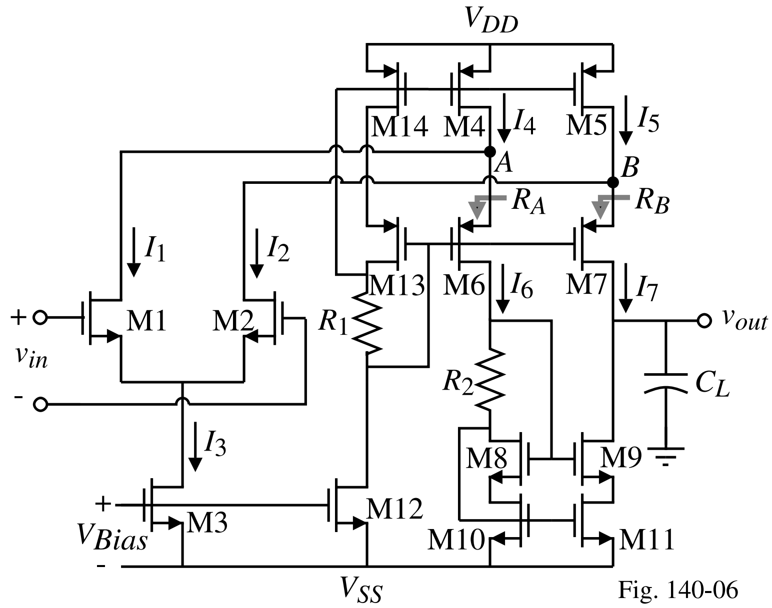


Fig. 140-06

Comments:

- The bias currents, I_4 and I_5, should be designed so that I_6 and I_7 never become zero (i.e. I_4=I_5=1.5I_3)
- This amplifier is nearly balanced (would be exactly if R_A was equal to R_B)
- Self compensating
- Poor noise performance, the gain occurs at the output so all intermediate transistors contribute to the noise along with the input transistors. (Some first stage gain can be achieved if R_A and R_B are greater than g_{m1} or g_{m2}.

Small-Signal Analysis of the Folded Cascode Op Amp

Model:

Recalling what we learned about the resistance looking into the source of the cascode transistor;

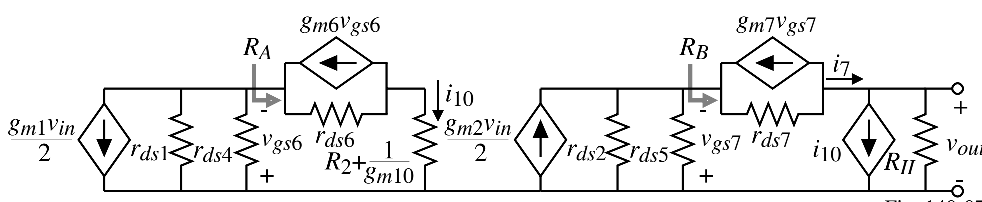


Fig. 140-07

$$R_A = \frac{r_{ds6}+R_2+(1/g_{m10})}{1+g_{m6}r_{ds6}} \approx \frac{1}{g_{m6}} \quad \text{and} \quad R_B = \frac{r_{ds7}+R_{II}}{1+g_{m7}r_{ds7}} \approx \frac{R_{II}}{g_{m7}r_{ds7}} \quad \text{where} \quad R_{II} \approx g_{m9}r_{ds9}r_{ds11}$$

The small-signal voltage transfer function can be found as follows. The current i_{10} is written as

$$i_{10} = \frac{-g_{m1}(r_{ds1}||r_{ds4})v_{in}}{2[R_A + (r_{ds1}||r_{ds4})]} \approx \frac{-g_{m1}v_{in}}{2}$$

and the current i_7 can be expressed as

$$i_7 = \frac{g_{m2}(r_{ds2}||r_{ds5})v_{in}}{2\left[\frac{R_{II}}{g_{m7}r_{ds7}} + (r_{ds2}||r_{ds5})\right]} = \frac{g_{m2}v_{in}}{2\left(1+\frac{R_{II}(g_{ds2}+g_{ds5})}{g_{m7}r_{ds7}}\right)} = \frac{g_{m2}v_{in}}{2(1+k)} \quad \text{where} \quad k = \frac{R_{II}(g_{ds2}+g_{ds4})}{g_{m7}r_{ds7}}$$

The output voltage, v_{out}, is equal to the sum of i_7 and i_{10} flowing through R_{out}. Thus,

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2(1+k)}\right)R_{out} = \left(\frac{2+k}{2+2k}\right) g_{mI}R_{out}$$

Frequency Response of the Folded Cascode Op Amp

The frequency response of the folded cascode op amp is determined primarily by the output pole which is given as

$$p_{out} = \frac{-1}{R_{out}C_{out}}$$

where C_{out} is all the capacitance connected from the output of the op amp to ground.

All other poles must be greater than $GB = g_{m1}/C_{out}$. The approximate expressions for each pole is

1.) Pole at node A: $p_A \approx -1/R_A C_A$

2.) Pole at node B: $p_B \approx -1/R_B C_B$

3.) Pole at drain of M6: $p_6 \approx \dfrac{-1}{(R_2+1/g_{m10})C_6}$

4.) Pole at source of M8: $p_8 \approx -g_{m8}/C_8$

5.) Pole at source of M9: $p_9 \approx -g_{m9}/C_9$

6.) Pole at gate of M10: $p_{10} \approx -g_{m10}/C_{10}$

where the approximate expressions are found by the reciprocal product of the resistance and parasitic capacitance seen to ground from a given node. One might feel that because R_B is approximately r_{ds} that this pole might be too small. However, at frequencies where this pole has influence, C_{out}, causes R_{out} to be much smaller making p_B also non-dominant.

Example 1 - Folded Cascode, CMOS Op Amp

Assume that all $g_{mN} = g_{mP} = 100\mu S$, $r_{dsN} = 2M\Omega$, $r_{dsP} = 1M\Omega$, and $C_L = 10pF$. Find all of the small-signal performance values for the folded-cascode op amp.

$$R_{II} = 0.4G\Omega,\ R_A = 10k\Omega,\text{ and } R_B = 4M\Omega \quad \therefore\ k = \frac{0.4\text{x}10^9(0.3\text{x}10^{-6})}{100} = 1.2$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{2+1.2}{2+2.4}\right)(100)(57.143) = (0.729)(5714.3) = 4{,}156\text{V/V}$$

$$R_{out} = R_{II}\,||[g_{m7}r_{ds7}(r_{ds5}||r_{ds2})] = 400M\Omega||[(100)(0.667M\Omega)] = 57.143M\Omega$$

$$|p_{out}| = \frac{1}{R_{out}C_{out}} = \frac{1}{57.143M\Omega\cdot 10pF} = 1{,}750\text{ rads/sec.} \Rightarrow 278\text{Hz} \Rightarrow GB = 1.21\text{MHz}$$

Comments on the Folded Cascode, CMOS Op Amp:

- Good PSRR
- Good ICMR
- Self compensated
- Can cascade an output stage to get extremely high gain with lower output resistance (use Miller compensation in this case)
- Need first stage gain for good noise performance
- Widely used in telecommunication circuits where large dynamic range is required

SUMMARY

- Two stage op amp gives reasonably robust performance as an "on-chip" op amp
- DC balance conditions insure proper mirroring and all transistors in saturation
- Slew rate of the two-stage op amp is I_5/C_c
- Folded cascode op amp offers wider input common voltage range
- Folded cascode op amp is a self-compensated op amp because the dominant pole at the output and proportional to the load capacitor

