LECTURE 160 – MOSFET OP AMP DESIGN
(READING: GHLM – 472-480, AH – 269-286)

INTRODUCTION

Objective

The objective of this presentation is:

1.) Develop the design equations for a two-stage CMOS op amp

2.) Illustrate the design of a two-stage CMOS op amp

Outline

- Design relationships
- Design of Two Stage CMOS Op Amp
- Summary

OP AMP DESIGN

Unbuffered, Two-Stage CMOS Op Amp

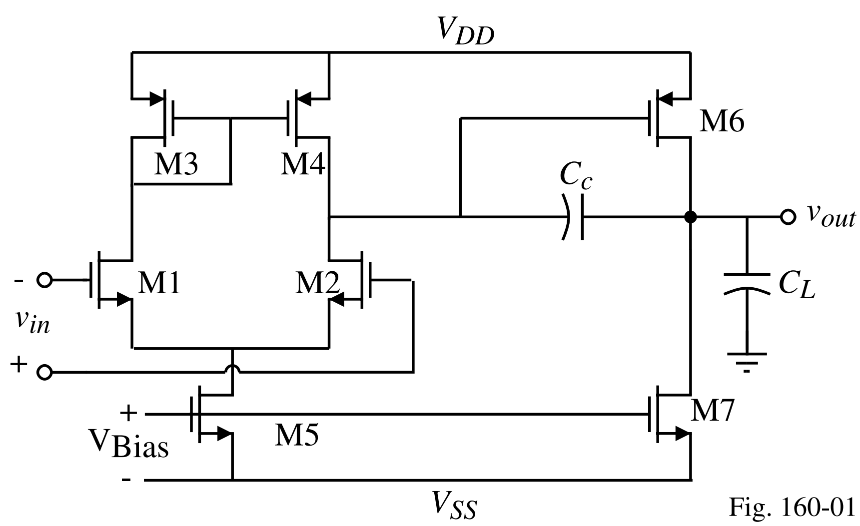

Fig. 160-01

Notation:

$$S_i = \frac{W_i}{L_i} = W/L \text{ of the ith transistor}$$

Design Relationships for the Two-Stage Op Amp

Slew rate $SR = \dfrac{I_5}{C_c}$ (Assuming $I_7 >> I_5$ and $C_L > C_c$)

First-stage gain $A_{v1} = \dfrac{g_{m1}}{g_{ds2} + g_{ds4}} = \dfrac{2g_{m1}}{I_5(\lambda_2 + \lambda_4)}$

Second-stage gain $A_{v2} = \dfrac{g_{m6}}{g_{ds6} + g_{ds7}} = \dfrac{g_{m6}}{I_6(\lambda_6 + \lambda_7)}$

Gain-bandwidth $GB = \dfrac{g_{m1}}{C_c}$

Output pole $p_2 = \dfrac{-g_{m6}}{C_L}$

RHP zero $z_1 = \dfrac{g_{m6}}{C_c}$

60° phase margin requires that $g_{m6} = 2.2g_{m2}(C_L/C_c)$ if all other roots are $\geq 10GB$.

Positive ICMR $V_{in(max)} = V_{DD} - \sqrt{\dfrac{I_5}{\beta_3}} - |V_{T03}|_{(max)} + V_{T1(min)})$

Negative ICMR $V_{in(min)} = V_{SS} + \sqrt{\dfrac{I_5}{\beta_1}} + V_{T1(max)} + V_{DS5}(sat)$

Saturation voltage $V_{DS}(sat) = \sqrt{\dfrac{2I_{DS}}{\beta}}$ (all transistors are saturated)

Op Amp Specifications

The following design procedure assumes that specifications for the following parameters are given.

1. Gain at dc, $A_v(0)$
2. Gain-bandwidth, GB
3. Phase margin (or settling time)
4. Input common-mode range, ICMR
5. Load Capacitance, C_L
6. Slew-rate, SR
7. Output voltage swing
8. Power dissipation, P_{diss}

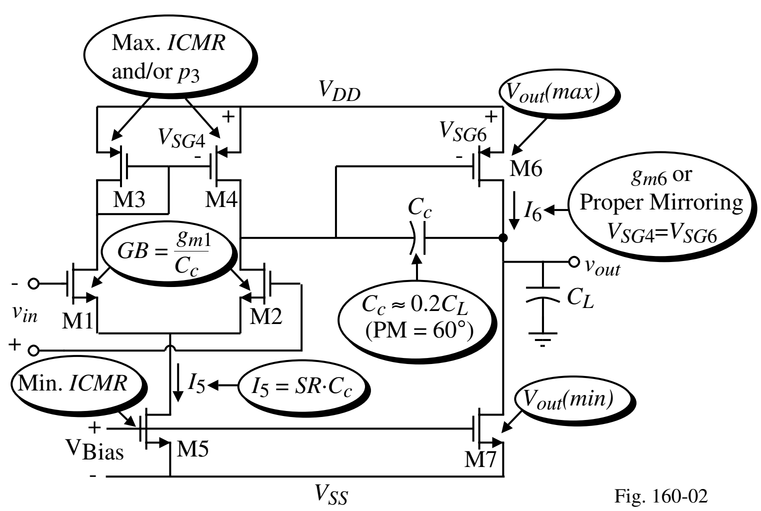

Fig. 160-02

Unbuffered Op Amp Design Procedure

This design procedure assumes that the gain at dc (A_v), unity gain bandwidth (GB), input common mode range (V_{in}(min) and V_{in}(max)), load capacitance (C_L), slew rate (SR), settling time (T_s), output voltage swing (V_{out}(max) and V_{out}(min)), and power dissipation (P_{diss}) are given. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.

1. From the desired phase margin, choose the minimum value for C_c, i.e. for a 60° phase margin we use the following relationship. This assumes that $z \geq 10GB$.

$$C_c > 0.22C_L$$

2. Determine the minimum value for the "tail current" (I_5) from the largest of the two values.

$$I_5 = SR \cdot C_c \qquad \text{or} \qquad I_5 \cong 10\left(\frac{V_{DD} + |V_{SS}|}{2 \cdot T_s}\right)$$

3. Design for S_3 from the maximum input voltage specification.

$$S_3 = \frac{I_5}{K'_3[V_{DD} - V_{in}(\text{max}) - |V_{T03}|(\text{max}) + V_{T1}(\text{min})]^2}$$

4. Verify that the pole of M3 due to C_{gs3} and C_{gs4} (= $0.67W_3L_3C_{ox}$) will not be dominant by assuming it to be greater than 10 GB

$$\frac{g_{m3}}{2C_{gs3}} > 10GB.$$

Unbuffered Op Amp Design Procedure - Continued

5. Design for S_1 (S_2) to achieve the desired GB.

$$g_{m1} = GB \cdot C_c \rightarrow S_2 = \frac{g_{m2}^2}{K'_2 I_5}$$

6. Design for S_5 from the minimum input voltage. First calculate V_{DS5}(sat) then find S_5.

$$V_{DS5}(\text{sat}) = V_{in}(\text{min}) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\text{max}) \geq 100 \text{ mV} \quad \rightarrow \quad S_5 = \frac{2I_5}{K'_5[V_{DS5}(\text{sat})]^2}$$

7. Find S_6 by letting the second pole (p_2) be equal to 2.2 times GB and assuming that $V_{SG4} = V_{SG6}$.

$$g_{m6} = 2.2g_{m2}(C_L/C_c) \quad \rightarrow \quad S_6 = S_4 \frac{g_{m6}}{g_{m4}}$$

8. Calculate I_6 from

$$I_6 = \frac{g_{m6}^2}{2K'_6 S_6}$$

Check to make sure that S_6 satisfies the V_{out}(max) requirement and adjust as necessary.

9. Design S_7 to achieve the desired current ratios between I_5 and I_6.

$$S_7 = (I_6/I_5)S_5 \qquad \text{(Check the minimum output voltage requirements)}$$

Unbuffered Op Amp Design Procedure - Continued

10. Check gain and power dissipation specifications.

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)} \qquad P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

11. If the gain specification is not met, then the currents, I_5 and I_6, can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they are satisfied. If the power dissipation is too high, then one can only reduce the currents I_5 and I_6. Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.

12. Simulate the circuit to check to see that all specifications are met.

Example 1 - Design of a Two-Stage Op Amp

Using the material and device parameters given in Tables 3.1-1 and 3.1-2, design an amplifier similar to that shown in Fig. 6.3-1 that meets the following specifications. Assume the channel length is to be 1µm.

$A_v > 3000$V/V	$V_{DD} = 2.5$V	$V_{SS} = -2.5$V	60° phase margin
$GB = 5$MHz	$C_L = 10$pF	$SR > 10$V/µs	
V_{out} range = ±2V	$ICMR = -1$ to 2V	$P_{diss} \leq 2$mW	

Solution

1.) The first step is to calculate the minimum value of the compensation capacitor C_c,

$$C_c > (2.2/10)(10\text{ pF}) = 2.2\text{ pF}$$

2.) Choose C_c as 3pF. Using the slew-rate specification and C_c calculate I_5.

$$I_5 = (3\text{x}10^{-12})(10\text{x}10^6) = 30\ \mu\text{A}$$

3.) Next calculate $(W/L)_3$ using ICMR requirements.

$$(W/L)_3 = \frac{30\text{x}10^{-6}}{(50\text{x}10^{-6})[2.5 - 2 - .85 + 0.55]^2} = 15 \quad \rightarrow \quad \boxed{(W/L)_3 = (W/L)_4 = 15}$$

Example 1 - Continued

4.) Now we can check the value of the mirror pole, p_3, to make sure that it is in fact greater than $10GB$. Assume the $C_{ox} = 0.4\text{fF}/\mu\text{m}^2$. The mirror pole can be found as

$$p_3 \approx \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K'_pS_3I_3}}{2(0.667)W_3L_3C_{ox}} = 2.81\text{x}10^9\text{(rads/sec)}$$

or 448 MHz. Thus, p_3, is not of concern in this design because $p_3 >> 10GB$.

5.) The next step in the design is to calculate g_{m1} to get

$$g_{m1} = (5\text{x}10^6)(2\pi)(3\text{x}10^{-12}) = 94.25\mu\text{S}$$

Therefore, $(W/L)_1$ is

$$(W/L)_1 = (W/L)_2 = \frac{g_{m1}^2}{2K'_NI_1} = \frac{(94.25)^2}{2\cdot 110\cdot 15} = 2.79 \approx 3.0 \quad \Rightarrow \quad \boxed{(W/L)_1 = (W/L)_2 = 3}$$

6.) Next calculate V_{DS5},

$$V_{DS5} = (-1) - (-2.5) - \sqrt{\frac{30\text{x}10^{-6}}{110\text{x}10^{-6}\cdot 3}} - .85 = 0.35\text{V}$$

Using V_{DS5} calculate $(W/L)_5$ from the saturation relationship.

$$(W/L)_5 = \frac{2(30\text{x}10^{-6})}{(110\text{x}10^{-6})(0.35)^2} = 4.49 \approx 4.5 \quad \rightarrow \quad \boxed{(W/L)_5 = 4.5}$$

Example 1 - Continued

7.) For 60° phase margin, we know that

$$g_{m6} \geq 10g_{m1} \geq 942.5\mu\text{S}$$

Assuming that $g_{m6} = 942.5\mu\text{S}$ and knowing that $g_{m4} = 150\mu\text{S}$, we calculate $(W/L)_6$ as

$$(W/L)_6 = 15\,\frac{942.5\text{x}10^{-6}}{(150\text{x}10^{-6})} = 94.25 \approx 94$$

8.) Calculate I_6 using the small-signal g_m expression:

$$I_6 = \frac{(942.5\text{x}10^{-6})^2}{(2)(50\text{x}10^{-6})(94.25)} = 94.5\mu\text{A} \approx 95\mu\text{A}$$

If we calculate $(W/L)_6$ based on V_{out}(max), the value is approximately 15. Since 94 exceeds the specification and maintains better phase margin, we will stay with $(W/L)_6 =$ 94 and $I_6 = 95\mu\text{A}$.

With $I_6 = 95\mu\text{A}$ the power dissipation is

$$P_{diss} = 5\text{V}\cdot(30\mu\text{A}+95\mu\text{A}) = 0.625\text{mW}.$$

Example 1 - Continued

9.) Finally, calculate $(W/L)_7$

$$(W/L)_7 = 4.5\left(\frac{95\text{x}10^{-6}}{30\text{x}10^{-6}}\right) = 14.25 \approx 14 \quad \rightarrow \quad \boxed{(W/L)_7 = 14}$$

Let us check the V_{out}(min) specification although the W/L of M7 is so large that this is probably not necessary. The value of V_{out}(min) is

$$V_{out}(\text{min}) = V_{DS7}(\text{sat}) = \sqrt{\frac{2\cdot 95}{110\cdot 35}} = 0.351\text{V}$$

which is less than required. At this point, the first-cut design is complete.

10.) Now check to see that the gain specification has been met

$$A_v = \frac{(92.45\text{x}10^{-6})(942.5\text{x}10^{-6})}{15\text{x}10^{-6}\,(.04 + .05)95\text{x}10^{-6}\,(.04 + .05)} = 7{,}697\text{V/V}$$

which exceeds the specifications by a factor of two. .An easy way to achieve more gain would be to increase the W and L values by a factor of two which because of the decreased value of λ would multiply the above gain by a factor of 20.

Incorporating the Nulling Resistor into the Miller Compensated Two-Stage Op Amp

Circuit:

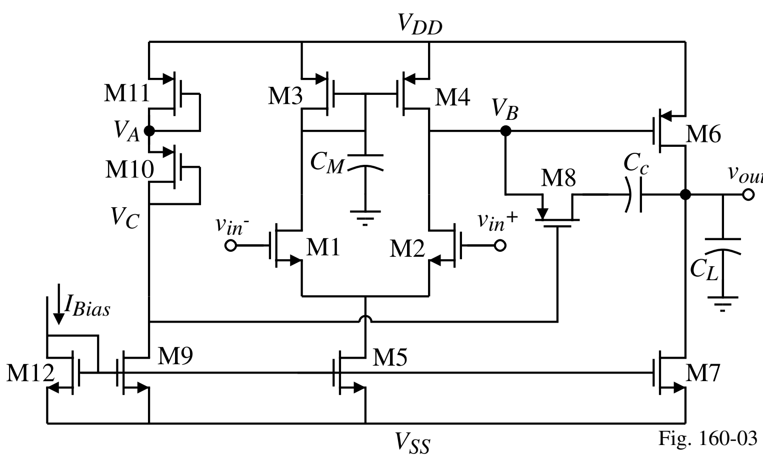

Fig. 160-03

We saw earlier that the roots were:

$$p_1 = -\frac{g_{m2}}{A_vC_c} = -\frac{g_{m1}}{A_vC_c} \qquad p_2 = -\frac{g_{m6}}{C_L}$$

$$p_4 = -\frac{1}{R_zC_I} \qquad z_1 = \frac{-1}{R_zC_c - C_c/g_{m6}}$$

where $A_v = g_{m1}g_{m6}R_IR_{II}$.

(Note that p_4 is the pole resulting from the nulling resistor compensation technique.)

Design of the Nulling Resistor (M8)

In order to place the zero on top of the second pole (p_2), the following relationship must hold

$$R_z = \frac{1}{g_{m6}}\left(\frac{C_L + C_c}{C_c}\right) = \left(\frac{C_c+C_L}{C_c}\right)\frac{1}{\sqrt{2K'_P S_6 I_6}}$$

The resistor, R_z, is realized by the transistor M8 which is operating in the active region because the dc current through it is zero. Therefore, R_z, can be written as

$$R_z = \frac{\partial v_{DS8}}{\partial i_{D8}}\Big|_{V_{DS8}=0} = \frac{1}{K'_P S_8 (V_{SG8}-|V_{TP}|)}$$

The bias circuit is designed so that voltage V_A is equal to V_B.

$$\therefore \quad |V_{GS10}| - |V_T| = |V_{GS8}| - |V_T| \Rightarrow \quad V_{SG11} = V_{SG6} \quad \Rightarrow \quad \left(\frac{W_{11}}{L_{11}}\right) = \left(\frac{I_{10}}{I_6}\right)\left(\frac{W_6}{L_6}\right)$$

In the saturation region

$$|V_{GS10}| - |V_T| = \sqrt{\frac{2(I_{10})}{K'_P(W_{10}/L_{10})}} = |V_{GS8}| - |V_T|$$

$$\therefore \quad R_z = \frac{1}{K'_P S_8}\sqrt{\frac{K'_P S_{10}}{2I_{10}}} = \frac{1}{S_8}\sqrt{\frac{S_{10}}{2K'_P I_{10}}}$$

Equating the two expressions for R_z gives $\left(\frac{W_8}{L_8}\right) = \left(\frac{C_c}{C_L + C_c}\right)\sqrt{\frac{S_{10}S_6 I_6}{I_{10}}}$

Example 2 - RHP Zero Compensation

Use results of Ex. 1 and design compensation circuitry so that the RHP zero is moved from the RHP to the LHP and placed on top of the output pole p_2. Use device data given in Ex. 1.

Solution

The task at hand is the design of transistors M8, M9, M10, M11, and bias current I_{10}. The first step in this design is to establish the bias components. In order to set V_A equal to V_B, then V_{SG11} must equal V_{SG6}. Therefore,

$$S_{11} = (I_{11}/I_6)S_6$$

Choose $I_{11} = I_{10} = I_9 = 15\mu A$ which gives $S_{11} = (15\mu A/95\mu A)94 = 14.8 \approx 15$.

The aspect ratio of M10 is essentially a free parameter, and will be set equal to 1. There must be sufficient supply voltage to support the sum of V_{SG11}, V_{SG10}, and V_{DS9}. The ratio of I_{10}/I_5 determines the (W/L) of M9. This ratio is

$$(W/L)_9 = (I_{10}/I_5)(W/L)_5 = (15/30)(4.5) = 2.25 \approx 2$$

Now $(W/L)_8$ is determined to be

$$(W/L)_8 = \left(\frac{3\text{pF}}{3\text{pF}+10\text{pF}}\right)\sqrt{\frac{1\cdot 94\cdot 95\mu A}{15\mu A}} = 5.63 \approx 6$$

Example 2 - Continued

It is worthwhile to check that the RHP zero has been moved on top of p_2. To do this, first calculate the value of R_z. V_{SG8} must first be determined. It is equal to V_{SG10}, which is

$$V_{SG10} = \sqrt{\frac{2I_{10}}{K'_P S_{10}}} + |V_{TP}| = \sqrt{\frac{2\cdot 15}{50\cdot 1}} + 0.7 = 1.474\text{V}$$

Next determine R_z.

$$R_z = \frac{1}{K'_P S_8(V_{SG10}-|V_{TP}|)} = \frac{10^6}{50\cdot 5.63(1.474-.7)} = 4.590\text{k}\Omega$$

The location of z_1 is calculated as

$$z_1 = \frac{-1}{(4.590 \text{ x } 10^3)(3\text{x}10^{-12}) - \frac{3\text{x}10^{-12}}{942.5\text{x}10^{-6}}} = -94.46\text{x}10^6 \text{ rads/sec}$$

The output pole, p_2, is

$$p_2 = \frac{942.5\text{x}10^{-6}}{10\text{x}10^{-12}} = -94.25\text{x}10^6 \text{ rads/sec}$$

Thus, we see that for all practical purposes, the output pole is canceled by the zero that has been moved from the RHP to the LHP.

The results of this design are summarized below.

W_8 = 6 µm W_9 = 2 µm W_{10} = 1 µm W_{11} = 15 µm

SUMMARY

Programmability of the Two-Stage Op Amp

The following relationships depend on the bias current, I_{bias}, in the following manner and allow for programmability after fabrication.

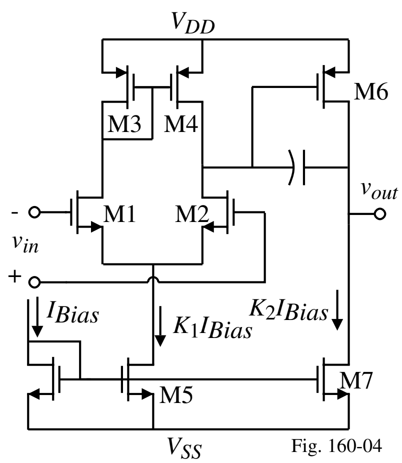

Fig. 160-04

$$A_v(0) = g_{mI}g_{mII}R_IR_{II} \propto \frac{1}{I_{Bias}}$$

$$GB = \frac{g_{mI}}{C_c} \propto \sqrt{I_{Bias}}$$

$$P_{diss} = (V_{DD}+|V_{SS}|)(1+K_1+K_2)I_{Bias} \propto I_{bias}$$

$$SR = \frac{K_1I_{Bias}}{C_c} \propto I_{Bias}$$

$$R_{out} = \frac{1}{2\lambda K_2I_{Bias}} \propto \frac{1}{I_{Bias}}$$

$$|p_1| = \frac{1}{g_{mII}R_IR_{II}C_c} \propto \frac{I_{Bias}{}^2}{\sqrt{I_{Bias}}} \propto I_{Bias}{}^{1.5}$$

$$|z| = \frac{g_{mII}}{C_c} \propto \sqrt{I_{Bias}}$$

Illustration of the I_{bias} dependence →

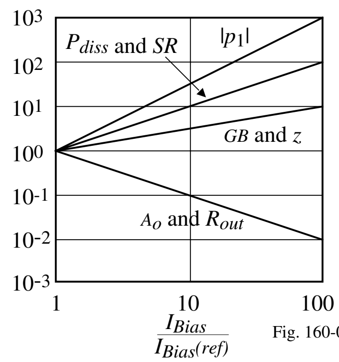

Fig. 160-05

