LECTURE 310 – HIGH SPEED/FREQUENCY OP AMPS
(READING: AH – 368-384)

Objective

The objective of this presentation is:

1.) Explore op amps having high frequency response and/or high slew rate

2.) Give examples

Outline

- Extending the GB of conventional op amps
- Switched op amps
- Current feedback op amps
- Programmable gain amplifiers
- Parallel path op amps
- Summary

What is the Influence of *GB* on the Frequency Response?

The op amp is primarily designed to be used with negative feedback. When the product of the op amp gain and feedback gain (loss) is not greater than unity, negative feedback does not work satisfactorily.

Example of a gain of -10 voltage amplifier:

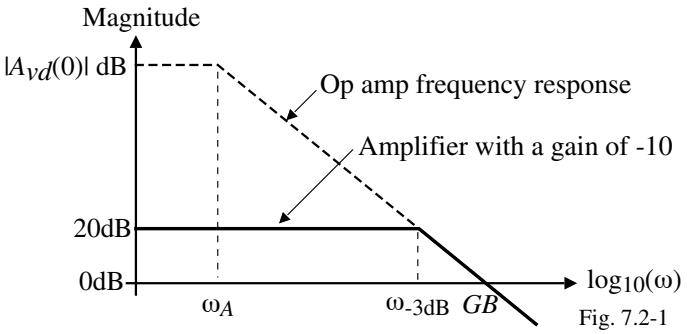


Fig. 7.2-1

What causes the *GB*?

We know that

$$GB = \frac{g_m}{C}$$

where g_m is the transconductance that converts the input voltage to current and C is the capacitor that causes the dominant pole.

This relationship assumes that all higher-order poles are greater than *GB*.

What is the Limit of *GB*?

The following illustrates what happens when the next higher pole is not greater than *GB*:

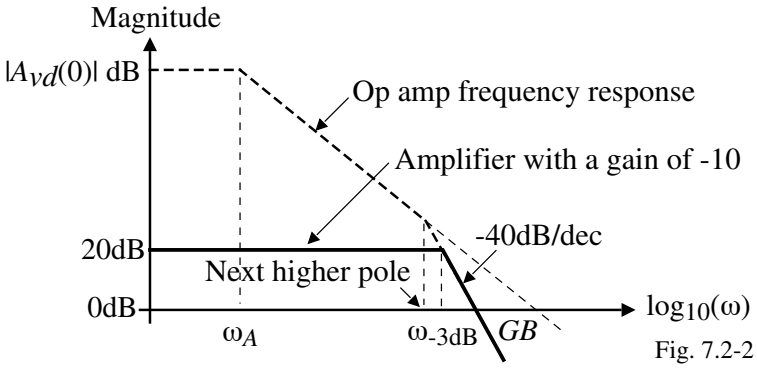


Fig. 7.2-2

For a two-stage op amp, the poles and zeros are:

1.) Dominant pole $p_1 = \dfrac{-g_{m1}}{A_v(0)C_c}$

2.) Output pole $p_2 = \dfrac{-g_{m6}}{C_L}$

3.) Mirror pole $p_3 = \dfrac{-g_{m3}}{C_{gs3}+C_{gs4}}$

4.) Nulling pole $p_4 = \dfrac{-1}{R_z C_I}$

5.) Nulling zero $z_1 = \dfrac{-1}{R_z C_c-(C_c/g_{m6})}$

A Procedure to Increase the *GB* of a Two-Stage Op Amp

1.) Use the nulling zero to cancel the closest pole beyond the dominant pole.

2.) The maximum *GB* would be equal to the magnitude of the second closest pole beyond the dominant pole.

3.) Adjust the dominant pole so that $GB \approx 2.2$x(second closest pole beyond the dominant pole)

Illustration which assumes that p_2 is the next closest pole beyond the dominant pole:

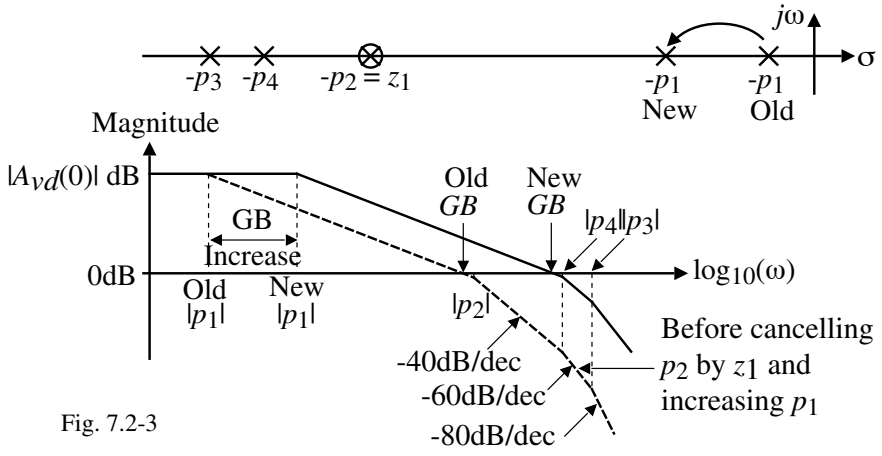


Fig. 7.2-3

Example 7.2-1 - Increasing the *GB* of the Op Amp Designed in Ex. 6.3-1

Use the two-stage op amp designed in Example 6.3-1 and apply the above approach to increase the gainbandwidth as much as possible.

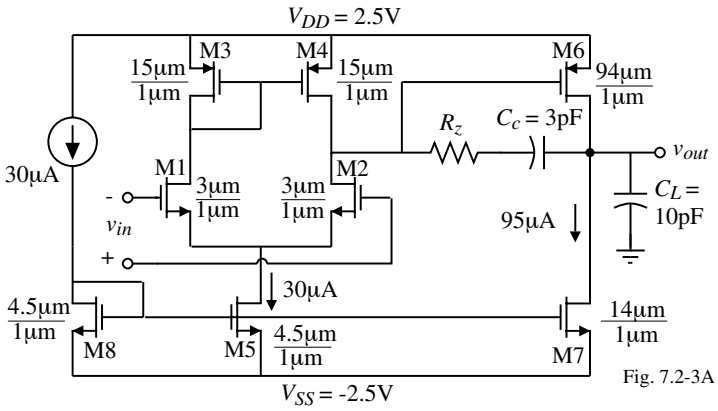


Fig. 7.2-3A

Solution

1.) First find the values of p_2, p_3, and p_4.

(a.) From Ex. 6.3-2, we see that

$$p_2 = -94.25\text{x}10^6 \text{ rads/sec.}$$

(b.) p_3 was found in Ex. 6.3-1 as

$$p_3 = -2.81\text{x}10^9 \text{ rads/sec.}$$

(c.) To find p_4, we must find C_I which is the output capacitance of the first stage of the op amp. C_I consists of the following capacitors,

$$C_I = C_{bd2} + C_{bd4} + C_{gs6} + C_{gd2} + C_{gd4}$$

For C_{bd2} the width is 3µm ⇒ L1+L2+L3 = 3µm ⇒ AS/AD=9µm^2 and PS/PD = 12µm.

For C_{bd4} the width is 15µm ⇒ L1+L2+L3 = 3µm ⇒ AS/AD=45µm^2 and PS/PD = 36µm.

From Table 3.2-1:

$$C_{bd2} = (9\mu\text{m}^2)(770\text{x}10^{-6}\text{F/m}^2) + (12\mu\text{m})(380\text{x}10^{-12}\text{F/m}) = 6.93\text{fF}+4.56\text{fF} = 11.5\text{fF}$$

$$C_{bd4} = (45\mu\text{m}^2)(560\text{x}10^{-6}\text{F/m}^2) + (36\mu\text{m})(350\text{x}10^{-12}\text{F/m}) = 25.2\text{fF}+12.6\text{F} \approx 37.8\text{fF}$$

Example 7.2-1 - Continued

C_{gs6} is given by Eq. (10b) of Sec. 3.2 and is

$$C_{gs6} = CGDO\cdot W_6 + 0.67(C_{ox}W_6L_6) = (220\text{x}10^{-12})(94\text{x}10^{-6}) + (0.67)(24.7\text{x}10^{-4})(94\text{x}10^{-12})$$
$$= 20.7\text{fF} + 154.8\text{fF} = 175.5\text{fF}$$

$$C_{gd2} = 220\text{x}10^{-12}\text{x}3\mu\text{m} = 0.66\text{fF} \quad \text{and} \quad C_{gd4} = 220\text{x}10^{-12}\text{x}15\mu\text{m} = 3.3\text{fF}$$

Therefore, C_I = 11.5fF + 37.8fF + 175.5fF + 0.66fF + 3.3fF = 228.8fF. Although C_{bd2} and C_{bd4} will be reduced with a reverse bias, let us use these values to provide a margin. In fact, we probably ought to double the whole capacitance to make sure that other layout parasitics are included. Thus let C_I be 300fF.

In Ex. 6.3-2, R_z was 4.591kΩ which gives p_4 = - 0.726x10^9 rads/sec.

2.) Using the nulling zero, z_1, to cancel p_2, gives p_4 as the next smallest pole.

For 60° phase margin $GB = |p_4|/2.2$ if the next smallest pole is more than 10*GB*.

$$\therefore \quad GB = 0.726\text{x}10^9/2.2 = 0.330\text{x}10^9 \text{ rads/sec. or } 52.5\text{MHz.}$$

This value of *GB* is designed from the relationship that $GB = g_{m1}/C_c$. Assuming g_{m1} is constant, then $C_c = g_{m1}/GB = (94.25\text{x}10^{-6})/(0.330\text{x}10^9) = 286\text{fF}$. It might be useful to increase g_{m1} in order to keep C_c above the surrounding parasitic capacitors (C_{gd6} = 20.7fF). The success of this method assumes that there are no other roots with a magnitude smaller than 10*GB*.

Example 7.2-2 - Increasing the *GB* of the Folded Cascode Op Amp of Ex. 6.5-3

Use the folded-cascode op amp designed in Example 6.5-3 and apply the above approach to increase the gainbandwidth as much as possible. Assume that the drain/source areas are equal to 2μm times the width of the transistor and that all voltage dependent capacitors are at zero voltage.

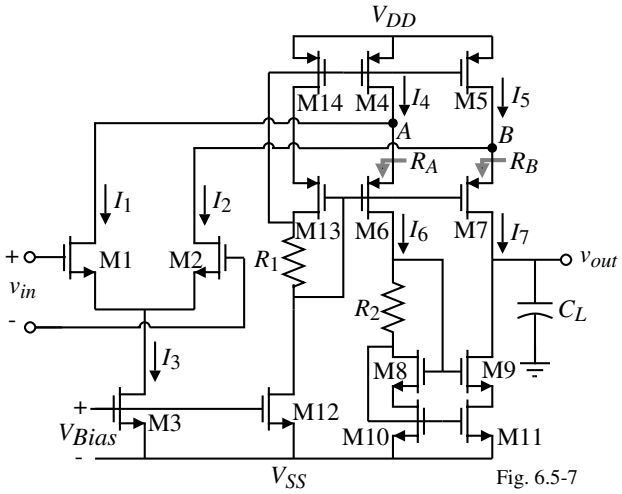


Fig. 6.5-7

Solution

The poles of the folded cascode op amp are:

$p_A \approx \dfrac{-1}{R_A C_A}$ (the pole at the source of M6)

$p_B \approx \dfrac{-1}{R_B C_B}$ (the pole at the source of M7)

$p_6 \approx \dfrac{-1}{(R_2+1/g_{m10})C_6}$ (the pole at the drain of M6)

$p_8 \approx \dfrac{-g_{m8}}{C_8}$ (the pole at the source of M8) $p_9 \approx \dfrac{-g_{m9}}{C_9}$ (the pole at the source of M9)

and $p_{10} \approx \dfrac{-g_{m10}}{C_{10}}$ (the pole at the gates of M10 and M11)

Example 7.2-2 - Continued

Let us evaluate each of these poles.

1,) For p_A, the resistance R_A is approximately equal to g_{m6} and C_A is given as

$$C_A = C_{gs6} + C_{bd1} + C_{gd1} + C_{bd4} + C_{bs6} + C_{gd4}$$

From Ex. 6.5-3, $g_{m6} = 744.6\mu S$ and capacitors giving C_A are found using the parameters of Table 3.2-1 as,

$$C_{gs6} = (220\text{x}10^{-12}\cdot 80\text{x}10^{-6}) + (0.67)(80\text{x}10^{-6}\cdot 10^{-6}\cdot 24.7\text{x}10^{-4}) = 149\text{fF}$$

$$C_{bd1} = (770\text{x}10^{-6})(35.9\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (380\text{x}10^{-12})(2\cdot 37.9\text{x}10^{-6}) = 84\text{fF}$$

$$C_{gd1} = (220\text{x}10^{-12}\cdot 35.9\text{x}10^{-6}) = 8\text{fF}$$

$$C_{bd4} = C_{bs6} = (560\text{x}10^{-6})(80\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (350\text{x}10^{-12})(2\cdot 82\text{x}10^{-6}) = 147\text{fF}$$

and

$$C_{gd4} = (220\text{x}10^{-12})(80\text{x}10^{-6}) = 17.6\text{fF}$$

Therefore,

$$C_A = 149\text{fF} + 84\text{fF} + 8\text{fF} + 147\text{fF} + 17.6\text{fF} + 147\text{fF} = 0.553\text{pF}$$

Thus,

$$p_A = \frac{-744.6\text{x}10^{-6}}{0.553\text{x}10^{-12}} = -1.346\text{x}10^{9} \text{ rads/sec.}$$

2.) For the pole, p_B, the capacitance connected to this node is

$$C_B = C_{gd2} + C_{bd2} + C_{gs7} + C_{gd5} + C_{bd5} + C_{bs7}$$

Example 7.2-2 - Continued

The various capacitors above are found as

$$C_{gd2} = (220\text{x}10^{-12}\cdot 35.9\text{x}10^{-6}) = 8\text{fF}$$
$$C_{bd2} = (770\text{x}10^{-6})(35.9\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (380\text{x}10^{-12})(2\cdot 37.9\text{x}10^{-6}) = 84\text{fF}$$
$$C_{gs7} = (220\text{x}10^{-12}\cdot 80\text{x}10^{-6}) + (0.67)(80\text{x}10^{-6}\cdot 10^{-6}\cdot 24.7\text{x}10^{-4}) = 149\text{fF}$$
$$C_{gd5} = (220\text{x}10^{-12})(80\text{x}10^{-6}) = 17.6\text{fF}$$

and

$$C_{bd5} = C_{bs7} = (560\text{x}10^{-6})(80\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (350\text{x}10^{-12})(2\cdot 82\text{x}10^{-6}) = 147\text{fF}$$

The value of C_B is the same as C_A and g_{m6} is assumed to be the same as g_{m7} giving $p_B = p_A = -1.346\text{x}10^9$ rads/sec.

3.) For the pole, p_6, the capacitance connected to this node is

$$C_6 = C_{bd6} + C_{gd6} + C_{gs8} + C_{gs9}$$

The various capacitors above are found as

$$C_{bd6} = (560\text{x}10^{-6})(80\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (350\text{x}10^{-12})(2\cdot 82\text{x}10^{-6}) = 147\text{fF}$$
$$C_{gs8} = (220\text{x}10^{-12}\cdot 36.4\text{x}10^{-6}) + (0.67)(36.4\text{x}10^{-6}\cdot 10^{-6}\cdot 24.7\text{x}10^{-4}) = 67.9\text{fF}$$

and

$$C_{gs9} = C_{gs8} = 67.9\text{fF} \qquad C_{gd6} = C_{gd5} = 17.6\text{fF}$$

Therefore,

$$C_6 = 147\text{fF} + 17.6\text{fF} + 67.9\text{fF} + 67.9\text{fF} = 0.300\text{pF}$$

Example 7.2-2 - Continued

From Ex. 6.5-3, $R_2 = 2\text{k}\Omega$ and $g_{m6} = 744.6\text{x}10^{-6}$. Therefore, p_6, can be expressed as

$$-p_6 = \frac{1}{(2\text{x}10^3 + (10^6/744.6))0.300\text{x}10^{-12}} = 0.966\text{x}10^9 \text{ rads/sec.}$$

4.) Next, we consider the pole, p_8. The capacitance connected to this node is

$$C_8 = C_{bd10} + C_{gd10} + C_{gs8} + C_{bs8}$$

These capacitors are given as,

$$C_{bs8} = C_{bd10} = (770\text{x}10^{-6})(36.4\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (380\text{x}10^{-12})(2\cdot 38.4\text{x}10^{-6}) = 85.2\text{fF}$$
$$C_{gs8} = (220\text{x}10^{-12}\cdot 36.4\text{x}10^{-6}) + (0.67)(36.4\text{x}10^{-6}\cdot 10^{-6}\cdot 24.7\text{x}10^{-4}) = 67.9\text{fF}$$

and

$$C_{gd10} = (220\text{x}10^{-12})(36.4\text{x}10^{-6}) = 8\text{fF}$$

The capacitance C_8 is equal to

$$C_8 = 67.9\text{fF} + 8\text{fF} + 85.2\text{fF} + 85.2\text{fF} = 0.246\text{pF}$$

Using the g_{m8} of Ex. 6.5-3 of 774.6μS, the pole p_8 is found as, $-p_8 = 3.149\text{x}10^9$ rads/sec.

5.) The capacitance for the pole at p_9 is identical with C_8. Therefore, since g_{m9} is also 774.6μS, the pole p_9 is equal to p_8 and found to be $-p_9 = 3.149\text{x}10^9$ rads/sec.

6.) Finally, the capacitance associated with p_{10} is given as

$$C_{10} = C_{gs10} + C_{gs11} + C_{bd8}$$

These capacitors are given as

Example 7.2-2 - Continued

$$C_{gs10} = C_{gs11} = (220\text{x}10^{-12}\cdot 36.4\text{x}10^{-6}) + (0.67)(36.4\text{x}10^{-6}\cdot 10^{-6}\cdot 24.7\text{x}10^{-4}) = 67.9\text{fF}$$

and

$$C_{bd8} = (770\text{x}10^{-6})(36.4\text{x}10^{-6}\cdot 2\text{x}10^{-6}) + (380\text{x}10^{-12})(2\cdot 38.4\text{x}10^{-6}) = 85.2\text{fF}$$

Therefore,

$$C_{10} = 67.9\text{fF} + 67.9\text{fF} + 85.2\text{fF} = 0.221\text{pF}$$

which gives the pole p_{10} as $-744.6\text{x}10^{-6}/0.246\text{x}10^{-12} = -3.505\text{x}10^{9}$ rads/sec.

The poles are summarized below:

$p_A = -1.346\text{x}10^9$ rads/sec $p_B = -1.346\text{x}10^9$ rads/sec $p_6 = -0.966\text{x}10^9$ rads/sec

$p_8 = -3.149\text{x}10^9$ rads/sec $p_9 = -3.149\text{x}10^9$ rads/sec $p_{10} = -3.505\text{x}10^9$ rads/sec

The smallest of these poles is p_6. Since p_A and p_B are not much larger than p_6, we will find the new *GB* by dividing p_6 by 5 (rather than 2.2) to get $200\text{x}10^6$ rads/sec. Thus the new *GB* will be $200/2\pi$ or 32MHz. The magnitude of the dominant pole is given as

$$p_{dominant} = \frac{GB}{A_{vd}(0)} = \frac{200\text{x}10^6}{7{,}464} = 26{,}795 \text{ rads/sec.}$$

The value of load capacitor that will give this pole is

$$C_L = \frac{1}{p_{dominant}\cdot R_{out}} = \frac{1}{26.795\text{x}10^3\cdot 19.4\text{M}\Omega} \approx 1.9\text{pF}$$

Therefore, the new *GB* = 32MHz compared with the old *GB* = 10MHz.

Conclusion for Increasing the *GB* of Op Amps

Maximum GB depends on the input transconductance and the capacitance that causes the dominant pole.

Quantity	MOSFET Op Amp	BJT Op Amp
g_m dependence	$\sqrt{2K'\left(\frac{W}{L}\right)I_D}$	$\frac{I_C}{kT/q} = \frac{I_C}{V_t}$
Maximum g_m	≈ 1 mA/V	≈ 20 mA/V
GB for 10pF	15 MHz	300 MHz
GB for 1pF	150 MHz	3 GHz

Note that the power dissipation will be large for large *GB* because current is needed for large g_m.

Assumption:

All higher-order roots are above *GB*.

The larger *GB*, the more difficult this becomes.

Conclusion:

- The best CMOS op amps have a *GB* of 10-50MHz
- The best BJT op amps have a *GB* of 100-200MHz

Switched Amplifiers

Switched amplifiers are time varying circuits that yield circuits with smaller parasitic capacitors and therefore higher frequency response. Such circuits are called *dynamically biased*.

- Switched amplifiers require a nonoverlapping clock
- Switched amplifiers only work during a portion of a clock period
- Bias conditions are setup on one clock phase and then maintained by capacitance on the active phase
- Switched amplifiers use switches and capacitors resulting in feedthrough problems
- Simplified circuits on the active phase minimize the parasitics

Typical clock:

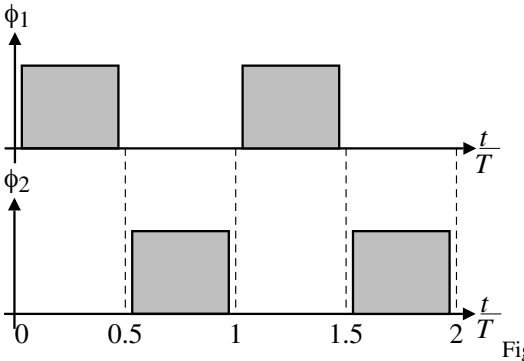


Fig. 7.2-3B

Dynamically Biased Inverting Amplifier

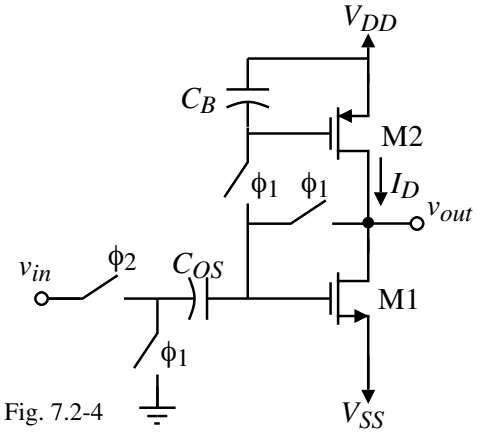


Fig. 7.2-4

During phase 1 the offset and bias of the inverter is sampled and applied to C_{OS} and C_B.

During phase 2 C_{OS} is connected in series with the input and provides offset canceling plus bias for M1. C_B provides the bias for M2.

(This circuit illustrates the concept of switched amplifiers but is too simple to illustrate the reduction of bias parasitics.)

Dynamically Biased, Push-Pull, Cascode Op Amp

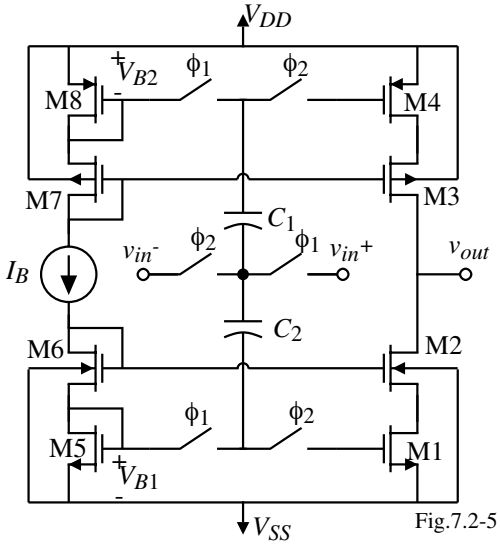


Fig.7.2-5

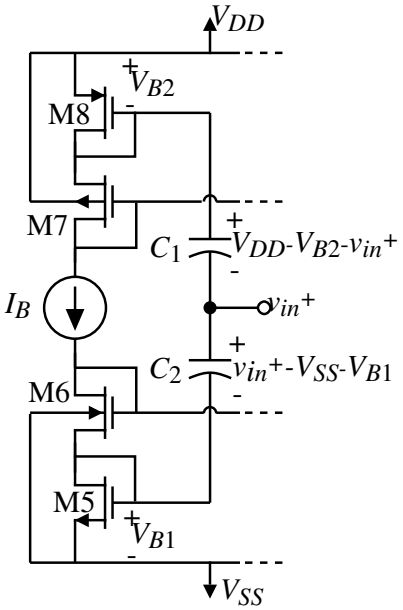
Push-pull, cascode amplifier: M1-M2 and M3-M4

Bias circuitry: M5-M6-C_2 and M7-M8-C_1

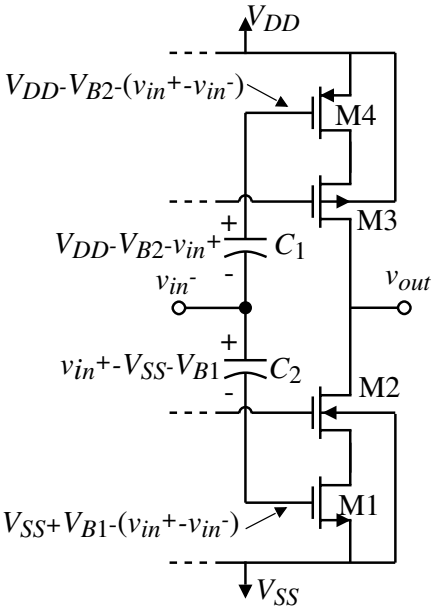
Parasitics can be further reduced by using a double-poly process to eliminate bulk-drain and bulk-source capacitances at the drain of M1-source of M2 and drain of M4-source of M3 (see Fig. 6.5-5).

Dynamically Biased, Push-Pull, Cascode Op Amp - Continued

Operation:



Equivalent circuit during the ϕ_1 clock period



Equivalent circuit during the ϕ_2 clock period.

Fig. 7.2-6

Dynamically Biased, Push-Pull, Cascode Op Amp - Continued

This circuit will operate on both clock phases[†] .

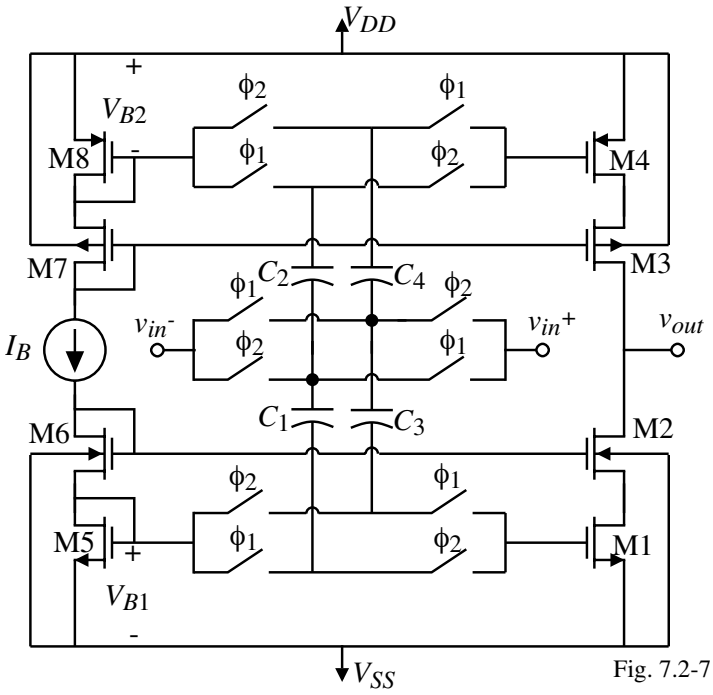


Fig. 7.2-7

Performance (1.5μm CMOS):

- 1.6mW dissipation
- $GB \approx 130$MHz (C_L=2.2pF)
- Settling time of 10ns (C_L=10pF)

This amplifier was used with a 28.6MHz clock to realize a 5th-order switched capacitor filter having a cutoff frequency of 3.5MHz.

[†] S. Masuda, et. al., "CMOS Sampled Differential Push-Pull Cascode Op Amp," *Proc. of 1984 International Symposium on Circuits and Systems*, Montreal, Canada, May 1984, pp. 1211-12-14.

Current Feedback Op Amps

Why current feedback:

- Higher *GB*
- Less voltage swing ⇒ more dynamic range

What is a current amplifier?

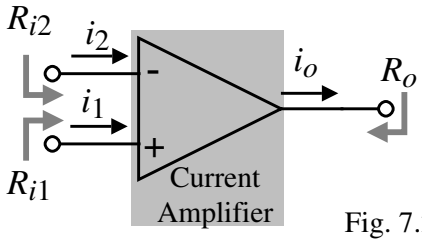


Fig. 7.2-8A

Requirements:

$i_o = A_i(i_1 - i_2)$

$R_{i1} = R_{i2} = 0\Omega$

$R_o = \infty$

Ideal source and load requirements:

$R_{source} = \infty$

$R_{Load} = 0\Omega$

Bandwidth Advantage of a Current Feedback Amplifier

Consider the inverting voltage amplifier shown using a current amplifier with negative current feedback:

The output current, i_o, of the current amplifier can be written as

$$i_o = A_i(s)(i_1-i_2) = -A_i(s)(i_{in} + i_o)$$

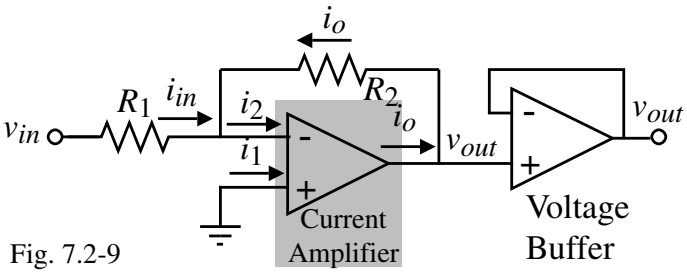


Fig. 7.2-9

The closed-loop current gain, i_o/i_{in}, can be found as

$$\frac{i_o}{i_{in}} = \frac{-A_i(s)}{1+A_i(s)}$$

However, $v_{out} = i_oR_2$ and $v_{in} = i_{in}R_1$. Solving for the voltage gain, v_{out}/v_{in} gives

$$\frac{v_{out}}{v_{in}} = \frac{i_oR_2}{i_{in}R_1} = \left(\frac{-R_2}{R_1}\right)\left(\frac{A_i(s)}{1+A_i(s)}\right)$$

If $A_i(s) = \dfrac{A_o}{\dfrac{s}{\omega_A}+1}$, then

$$\frac{v_{out}}{v_{in}} = \left(\frac{-R_2}{R_1}\right)\left(\frac{A_o}{1+A_o}\right)\left(\frac{\omega_A(1+A_o)}{s+\omega_A(1+A_o)}\right) \quad \Rightarrow \quad A_v(0) = \frac{-R_2A_o}{R_1(1+A_o)} \quad \text{and} \quad \boxed{\omega_{-3dB} = \omega_A(1+A_o)}$$

Bandwidth Advantage of a Current Feedback Amplifier - Continued

The unity-gainbandwidth is,

$$GB = |A_v(0)|\,\omega_{-3dB} = \frac{R_2A_o}{R_1(1+A_o)}\cdot\omega_A(1+A_o) = \frac{R_2}{R_1}A_o\cdot\omega_A = \frac{R_2}{R_1}GB_i$$

where GB_i is the unity-gainbandwidth of the current amplifier.

Note that if GB_i is constant, then increasing R_2/R_1 (the voltage gain) increases GB.

Illustration:

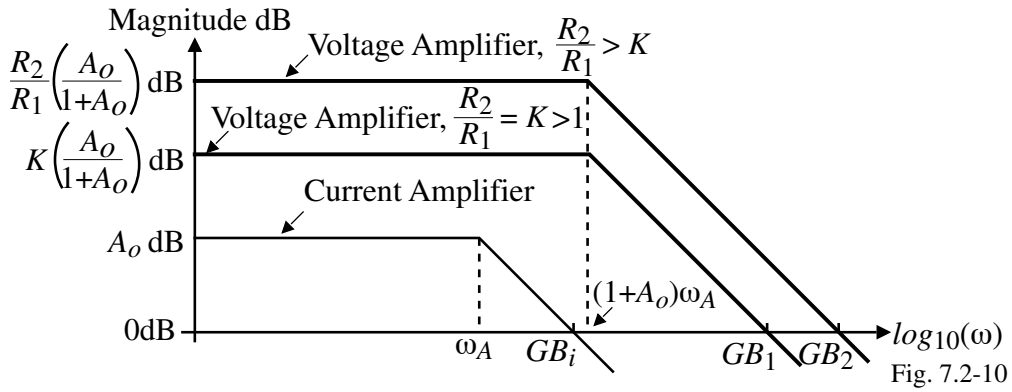


Fig. 7.2-10

Note that $GB_2 > GB_1 > GB_i$

The above illustration assumes that the *GB* of the voltage amplifier realizing the voltage buffer is greater than the *GB* achieved from the above method.

A Simple Current Mirror Implementation of a High Frequency Amplifier

Since the gain of the current amplifier does not need to be large, consider a unity-gain current mirror implementation:

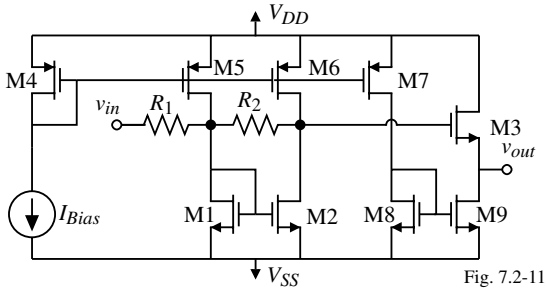


Fig. 7.2-11

An inverting amplifier with a gain of 10 is achieved if $R_2 = 20R_1$ assuming the gain of the current mirror is unity.

What is the *GB* of this amplifier?

$$GB = |A_v(0)|\omega_{-3dB} = \frac{R_2A_o}{R_1(1+A_o)} \cdot \frac{1}{R_2C_o} = \frac{A_o}{(1+A_o)R_1C_o} = \frac{1}{2R_1C_o}$$

where C_o is the capacitance seen at the output of the current mirror.

If $R_1 = 10k\Omega$ and $C_o = 250fF$, then $GB = 31.83MHz$.

Limitations:

$$R_1 > R_{in} = 1/g_{m1} \quad \text{and} \quad R_2 < r_{ds2}||r_{ds6} \quad \Rightarrow \quad \frac{R_2}{R_1} << g_{m1}(r_{ds2}||r_{ds6})$$

A Wide-Swing, Cascode Current Mirror Implementation of a High Frequency Amplifier

The current mirror shown below increases the value of R_2 by increasing the output resistance of the current mirror.

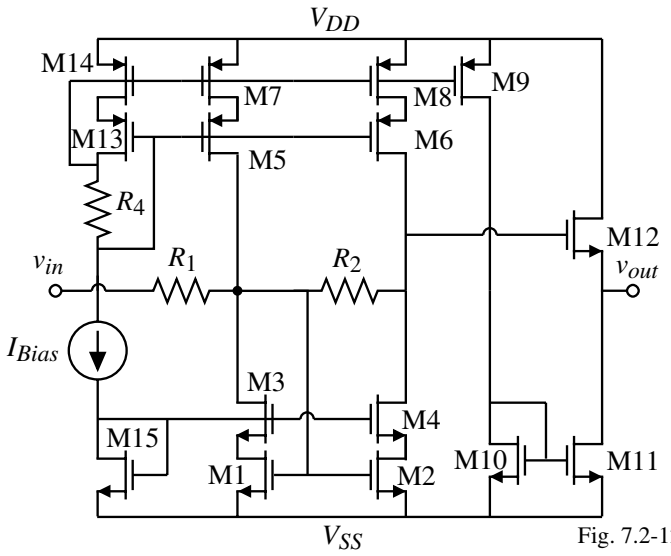


Fig. 7.2-12

New limitations:

$$R_1 > \frac{1}{g_{m1}} \quad \text{and} \quad R_2 < g_{m4}r_{ds4}r_{ds2}||g_{m6}r_{ds6}r_{ds8} \Rightarrow \frac{R_2}{R_1} << g_{m1}(g_{m4}r_{ds4}r_{ds2}||g_{m6}r_{ds6}r_{ds8})$$

Example 7.2-3 - Design of a High *GB* Voltage Amplifier using Current Feedback

Design the wide-swing, cascode voltage amplifier to achieve a gain of -10V/V and a *GB* of 500MHz which corresponds to a -3dB frequency of 50MHz.

Solution

Since we know what the gain is to be, let us begin by assuming that C_o will be 100fF. Thus to get a *GB* of 500MHz, R_1 must be 3.2kΩ and R_2 = 32kΩ. Therefore, $1/g_{m1}$ must be less than 3200Ω (say 300Ω). Therefore we can write

$$g_{m1} = \sqrt{2KI'(W/L)} = \frac{1}{300\Omega} \rightarrow \quad 5.56\text{x}10^{-6} = K'\cdot I\cdot\frac{W}{L} \quad \rightarrow \quad 0.0505 = I\cdot\frac{W}{L}$$

At this point we have a problem because if *W/L* is small to minimize C_o, the current will be too high. If we select *W/L* = 200μm/1μm we will get a current of 0.25mA. However, using this *W/L* for M4 and M6 will give a value of C_o that is greater than 100fF. Therefore, select *W/L* = 200 for M1, M3, M5 and M7 and *W/L* = 20μm/1μm for M2, M4, M6, and M8 which gives a current in these transistors of 25μA.

Since R_2/R_1 is multiplied by 1/11 let R_2 be 110 times R_1 or 352kΩ.

Now select a *W/L* for M12 of 20μm/1μm which will now permit us to calculate C_o. We will assume zero-bias on all voltage dependent capacitors. Furthermore, we will assume the diffusion area as 2μm times the *W*. C_o can be written as

$$C_o = C_{gd4} + C_{bd4} + C_{gd6} + C_{bd6} + C_{gs12}$$

Example 7.2-3 - Design of a High *GB* Voltage Amplifier using Current Feedback - Cont'd

The information required to calculate these capacitors is found from Table 3.2-1. The various capacitors are,

$C_{gd4} = C_{gd6} = CGDO\text{x}10\mu\text{m} = (220\text{x}10^{-12})(20\text{x}10^{-6}) = 4.4\text{fF}$

$C_{bd4} = CJ\text{x}AD_4 + CJSW\text{x}PD_4 = (770\text{x}10^{-6})(20\text{x}10^{-12}) + (380\text{x}10^{-12})(44\text{x}10^{-6}) = 15.4\text{fF} + 16.7\text{fF} = 32.1\text{fF}$

$C_{bd6} = (560\text{x}10^{-6})(20\text{x}10^{-12}) + (350\text{x}10^{-12})(44\text{x}10^{-6}) = 26.6\text{fF}$

$C_{gs12} = (220\text{x}10^{-12})(20\text{x}10^{-6}) + (0.67)(20\text{x}10^{-6}\cdot 10^{-6}\cdot 24.7\text{x}10^{-4}) = 37.3\text{fF}$

Therefore,

$C_o = 4.4\text{fF} + 32.1\text{fF} + 4.4\text{fF} + 26.6\text{fF} + 37.3\text{fF} = 105\text{fF}$

Note that if we had not reduced the *W/L* of M2, M4, M6, and M8 that C_o would have easily exceeded 100fF. Since 105fF is close to our original guess of 100fF, let us keep the values of R_1 and R_2. If this value was significantly different, then we would adjust the values of R_1 and R_2 so that the *GB* is 500MHz. One must also check to make sure that the input pole is greater than 500MHz.

The design is completed by assuming that I_{Bias} = 100μA and that the current in M9 through M12 be 100μA. Thus $W_{13}/L_{13} = W_{14}/L_{14}$ = 20μm,/1μm and W_9/L_9 through W_{12}/L_{12} are 20μm/1μm.

Example 7.2-3 - Continued

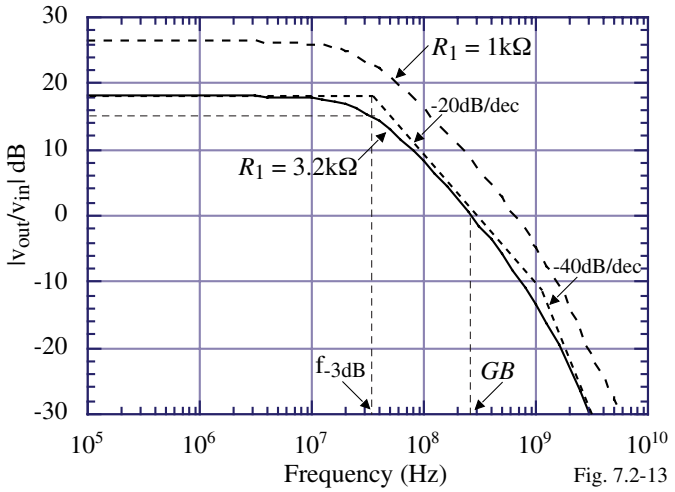


Fig. 7.2-13

Simulation Results:

$f_{-3dB} \approx$ 38MHz $GB \approx$ 300MHz Closed-loop gain = 18dB (Loss of -2dB is attributed to source follower and R_1)

Note second pole at about 1GHz. To get these results, it was necessary to bias the input at -1.7VDC using ±3V power supplies.

If R_1 is decreased to 1kΩ results in:

Gain of 26.4dB, f_{-3dB} = 32MHz, and GB = 630MHz

A 71 MHz Programmable Gain Amplifier using a Current Amplifier

The following circuit has been submitted for fabrication in 0.25μm CMOS:

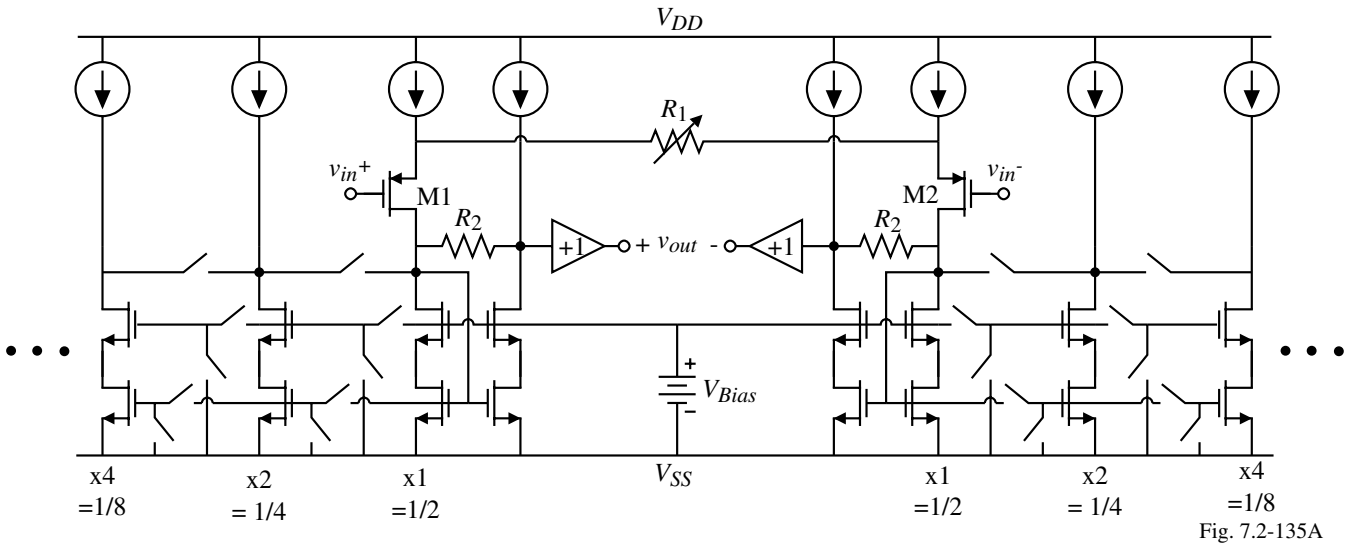


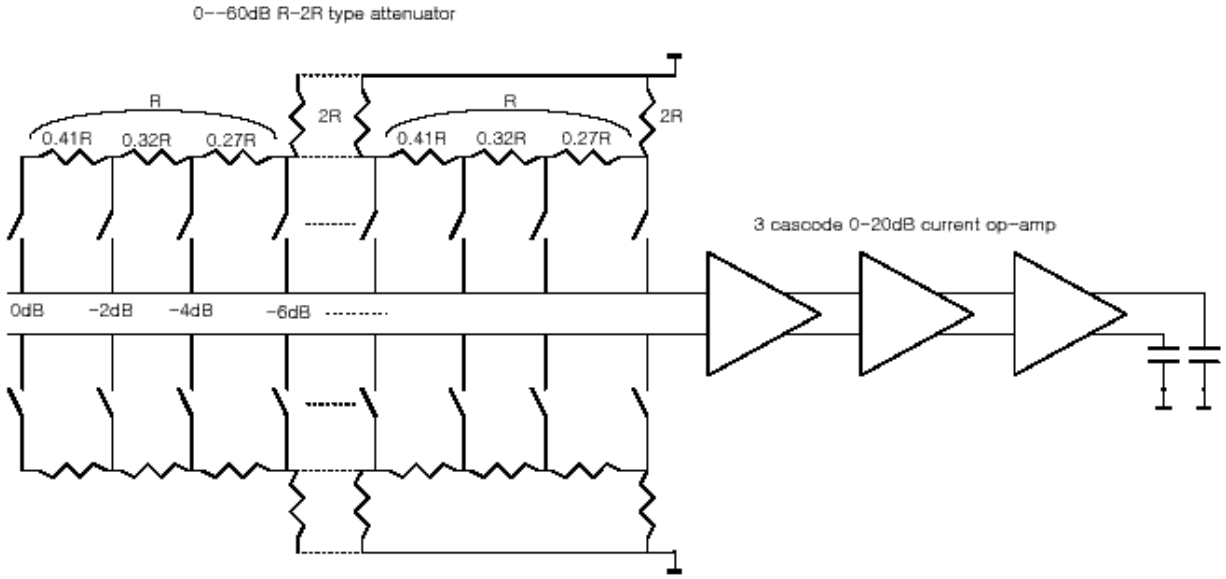
Fig. 7.2-135A

R_1 and the current mirrors are used for gain variation. R_2 is fixed.

Can cascade this amplifier for higher gains

$BW = BW_i\sqrt{2^{1/n}-1}$ for $n = 2$, $BW = 0.64\ BW_i$

Implementation of a 60dB Gain, 500MHz –3dB Frequency PGA



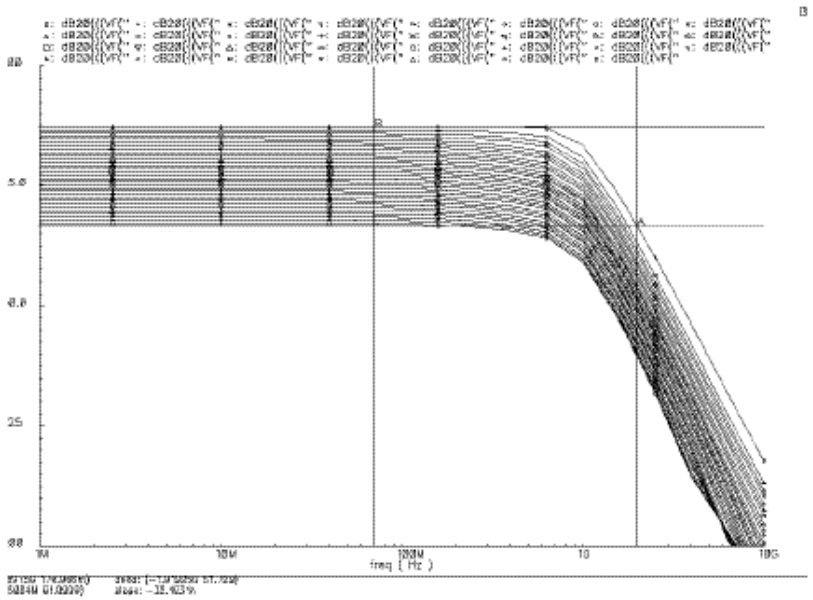
Simulation Results

Output voltage swing is 1.26V for a 2.5V power supply.

Voltage gain is 0 to 60dB in 2dB steps (gain error = ±0.17dB)

Maximum *GB* is 1.5GHz

Total current: 3.6mA



A 71 MHz CMOS Programmable Gain Amplifier†

Uses 3 ac-coupled stages.

First stage (0-20dB, common source for matching and NF):

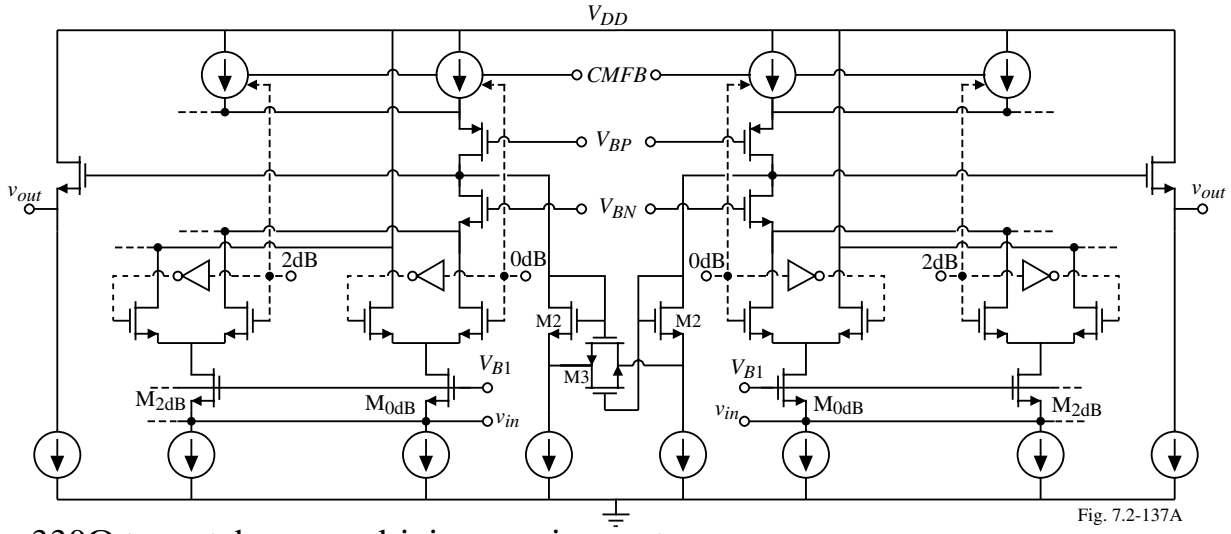


Fig. 7.2-137A

R_{in} = 330Ω to match source driving requirement

All current sinks are identical for the differential switches.

Dominant pole at 150MHz.

† P. Orsatti, F. Piazza, and Q. Huang, "A 71 MHz CMOS IF-Basdband Strip for GSM, *IEEE J. Solid-State Circuits*, vol. 35, No. 1, Jan. 2000, pp. 104-108.

A 71 MHz PGA – Continued

Second stage (-10dB to 20dB):

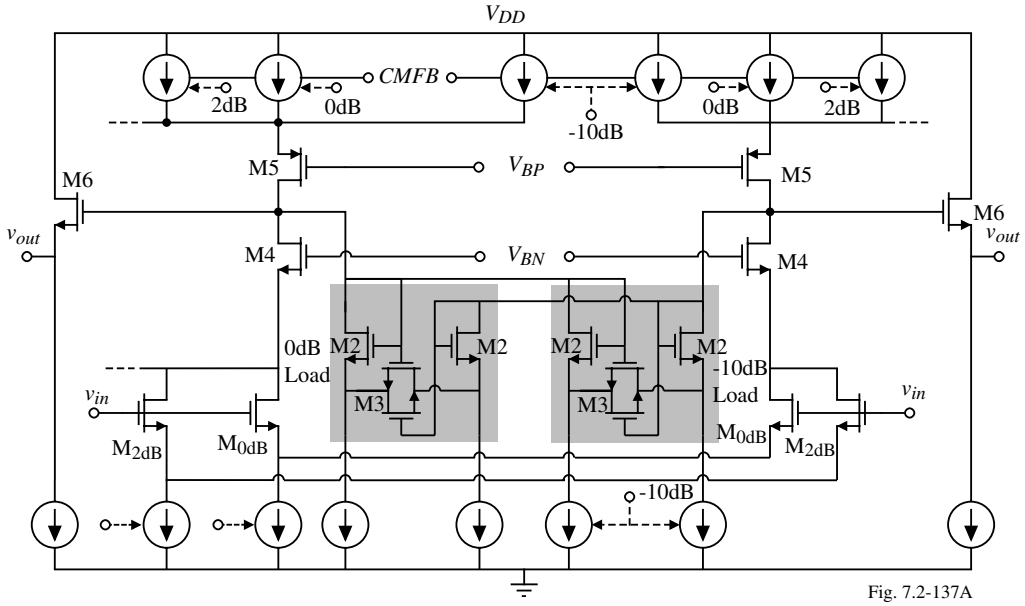


Fig. 7.2-137A

Dominant pole is also at 150MHz

For V_{DD} = 2.5V, at 60dB gain, the total current is 2.6mA

$IIP_3 \approx +1$dBm

Parallel Path Op Amps

This type of op amp combines a high-gain, low-frequency path with a low-gain, high-frequency path.

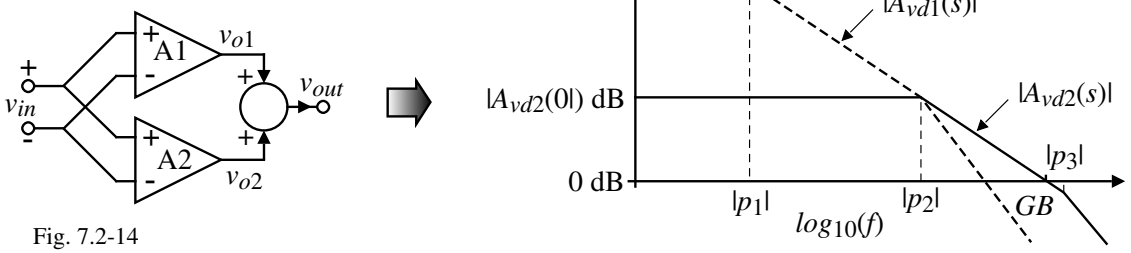


Fig. 7.2-14

Comments:

- Op amp will be conditionally stable
- Compensation will be challenging

Multipath Nested Miller Compensation[†]

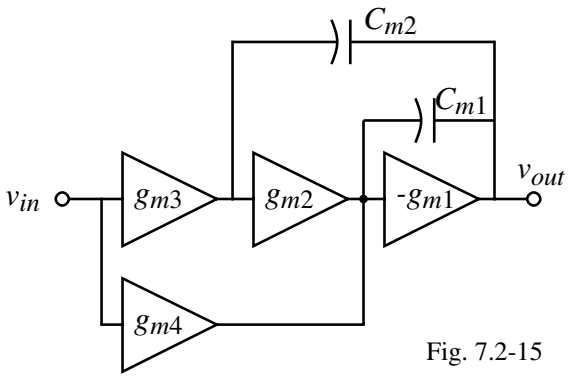


Fig. 7.2-15

Comments:

- All Miller capacitances must be around inverting stages
- Ensure that the RHP zeros generated by the Miller compensation are canceled
- Avoid pole-zero doublets which can introduce a slow time constant

[†] R.G.H. Eschauzier and J.H.Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers,* Kluwer Academic publishers, 1995, Chapter 6.

Illustration of Hybrid Nested Miller Compensation[†]

(Note that this example is not multipath.)

Compensating Results:

1) C_{m1} pushes p_4 to higher frequencies and p_3 down to lower frequencies

2) C_{m2} pushes p_2 to higher frequencies and p_1 down to lower frequencies

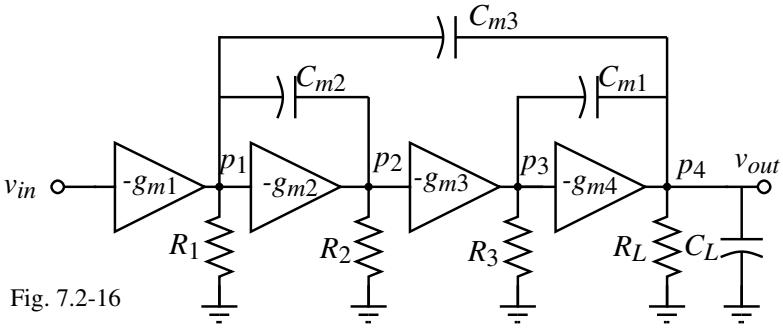


Fig. 7.2-16

3) C_{m3} pushes p_3 to higher frequencies (feedback path) & pulls p_1 further to lower frequencies

Equations:

$$GB \approx g_{m1}/C_{m3} \qquad p_2 \approx g_{m2}/C_{m3} \qquad p_3 \approx g_{m3}C_{m3}/(C_{m1}C_{m2}) \qquad p_4 \approx g_{m4}/C_L$$

Design:

$$GB < p_2, p_3, p_4$$

[†] R.G. H. Eschauzier *et. al.*, "A Programmable 1.5V CMOS Class-AB Operational Amplifier with Hybrid Nested Miller Compensation for 120dB Gain and 6MHz UGT," *IEEE J. of Solid State Circuits*, vol. 29, No. 12, pp. 1497-1504, Dec. 1994.

Illustration of the Hybrid Nested Miller Compensation Technique

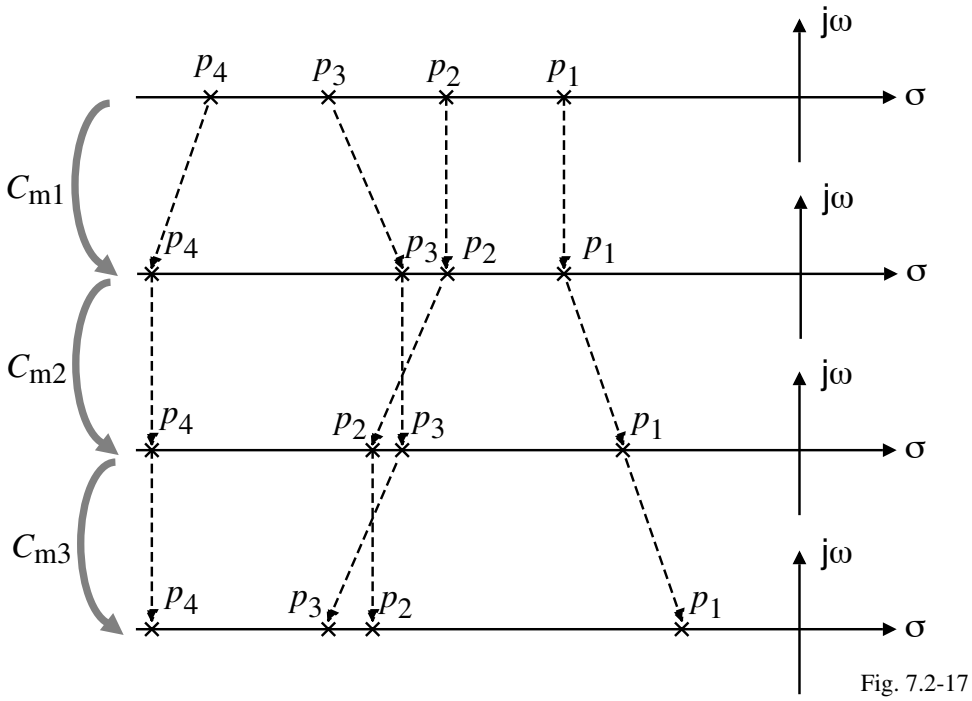


Fig. 7.2-17

SUMMARY

- Normal op amps limited by g_m/C
- Typical limit for CMOS op amp is $GB \approx 50$MHz
- Other approaches to high frequency CMOS op amps:
  - Current amplifiers (Transimpedance amplifiers)
  - Switched amplifier (simplifies the circuit ⇒ reduce capacitances)
  - Parallel path op amps (compensation becomes more complex)
- What does the future hold?
  - Reduction of channel lengths mean:
    - * Reduced capacitances ⇒ Higher *GB*'s
    - * Higher transconductances (larger values of *K*') ⇒ Higher *GB*'s
    - * Increased channel conductance ⇒ Lower gains (more stages required)
    - * Reduction of power supply ⇒ Increased capacitances

  In otherwords, there should be some improvement in op amp *GB*'s but it won't be inversely proportional to the decrease in channel length. I.e. maybe *GB*'s ≈ 100MHz for 0.2μm CMOS.