COURSE DETAILS AND INFORMATION FOR ECE6412 – ANALOG INTEGRATED CIRCUIT DESIGN II

Instructors: Dr. Phillip E. Allen, Room 292B, Van Leer, 894-6251 (office), (404) 603-9374 (home), pallen@ece.gatech.edu

Lecture: Monday, Wednesday, and Friday, 9:05am to 9:55am, Room 380, Bunger Henry

Office Hours: Allen: 10-1am, MF, 11-12pm W or by e-mail <pallen@ece.gatech.edu>.

Electronic Copies of Class Handouts: You may download pdf copies of all classroom material at the following web site: http://users.ece.gatech.edu/~pallen/Academic/

Prerequisite: EE 4430 Analog Integrated Circuit Design I or permission of instructor.

Texts:

Analysis and Design of Analog Integrated Circuits – Fourth Edition, Paul Gray, Paul Hurst, Steve Lewis and Robert Meyer, John Wiley and Sons, Inc., 2001

CMOS Analog Circuit Design – Second Edition, P.E. Allen and D.R. Holberg, Oxford University Press, 2002.

Objectives: The purpose of this course is to enable the student to model, analyze and design analog integrated circuits using bipolar and/or MOS technologies. At the conclusion of the course, the student should be able to successfully perform the electrical and physical design of an op amp or analog circuit of similar complexity in an industrial environment.

Examinations: There will be three, closed book midterm examinations each of 50 minute duration and a 3 hour final examination. The final examination will be given during the regularly scheduled time for the final exam. All grades become final one week after they are returned in class.

Final Exam: The final exam is on Thursday, May 5, 2005, from 2:50pm to 5:40pm.

Homework: Homework will be assigned and will be graded.

Course Grading Policy: Your grade will be determined using the following scheme:

Three midterm exams…….. 60%
Homework…… 10%
Final Exam…… 30%

Grades will be assigned on a curve and will not necessarily be consistent with 100>A>90, 90>B>80, etc..

Computer Usage: You are expected to be able to use HSPICE or PSPICE for classroom assignments. Most assignments using the computer will work on the student version of PSPICE. The educational version of PSpice for the PC is free and downloadable from:

http://www.orcad.com/products/pspice/eval_f.htm

Attendance: You are responsible for all course materials, announcements, notes, etc. made during our regular class meeting times. Prompt arrival to class is appreciated.

Academic Honesty: It is the responsibility of the instructor to encourage an environment where you can learn and your accomplishments will be rewarded fairly. Any behavior that compromises the basic rules of academic honesty as described in the General Catalog will not be tolerated.

Classroom Behavior: Smoking, drinking and eating is prohibited in the classroom by Institute rules.

Weekly Coverage of Topics for ECE6412

Week	Date	Lect. #	Topic	GHLM	AH
	1/10	010	Introduction, ECE 4430 Review	1-75	-
1	1/12	020	ECE 4430 Review, Continued	78-154	-
	1/14	030	ECE 4430 Review, Continued	170-336	-
	1/17		Holiday		
2	*1/19*	040	Common source, common emitter	384-398	218-221
	1/21	050	Followers	344-362	221-226
	1/24	060	Push-pull output stages	362-384	226-22
3	1/26	070	Frequency response, single stage I	488-504	-
	1/28	080	Frequency response, single stage II	504-516	-
	1/31	090	Multiple-stage frequency response I	516-527	-
4	2/2	100	Multiple-stage frequency response II	527-537	-
	2/4	110	Introduction and characterization of the op amp	404-424	243-249
	2/7	120	Compensation of Two-Stage Op Amps	425-434	249-260
5	2/9	130	Compensation of Two-Stage Op Amps	638-652	260-269
	2/11	140	Simple CMOS op amps	425-434	249-253
	2/14		Examination No. 1		
6	2/16	150	Simple BJT op amps	425-434	
				453-454	249-253
	2/18	160	MOSFET Op Amp Design	472-480	269-286
	2/21	170	Intuitive analysis of analog circuits	472-480	269-286
7	*2/23*	180	Power supply rejection ratio	-	286-293
	2/25	190	Cascode op amps-I	434-439	293-309
	2/28	200	Cascode op amps-II	443-453	293-309
8	3/2	210	DC analysis of the 741 op amp	454-462	-
	3/4	220	AC analysis of the 741 op amp	462-472	-
	3/7	230	741 frequency response	537-544	-
9	3/9	240	Simulation and measurement of op amps	579-587	310-323
	3/11	250	Introduction to feedback concepts	553-563	-
	3/14		Examination No. 2		
10	3/16	260	Shunt-shunt feedback	563-569	-
	3/18	270	Series-series feedback	569-579	-
	3/21-3/25		Spring Break		
	3/28	280	Series-shunt and shunt-series feedback	579-587	-
11	3/30	290	Feedback circuit analysis using return ratio	599-613	-
	4/1	300	Buffered op amps	-	384-393
	4/4		Guest Speaker – Alan Hastings, Texas Inst.		
12	4/6	310	High speed/frequency op amps	-	368-384
	4/8	320	Differential output op amps	808-85	384-393
	4/11	330	Low power op amps	-	393-402
13	4/13	340	Low noise op amps	788-798	402-414
	4/15	350	Low voltage op amps	-	415-432
	4/18		Examination No. 3		
14	4/20	360	Characterization of comparators	-	439-444
	4/22	370	Two-stage, open-loop comparators-	-	445-461
	4/25	380	Two-stage, open-loop comparators-II	-	445-461
15	4/27	390	Open-loop comparators	-	461-475
	4/29	400	Discrete-time, high-speed comparators	-	475-488
The final exam is scheduled for Thursday, May 5, 2005, from 2:50pm to 5:40pm.					