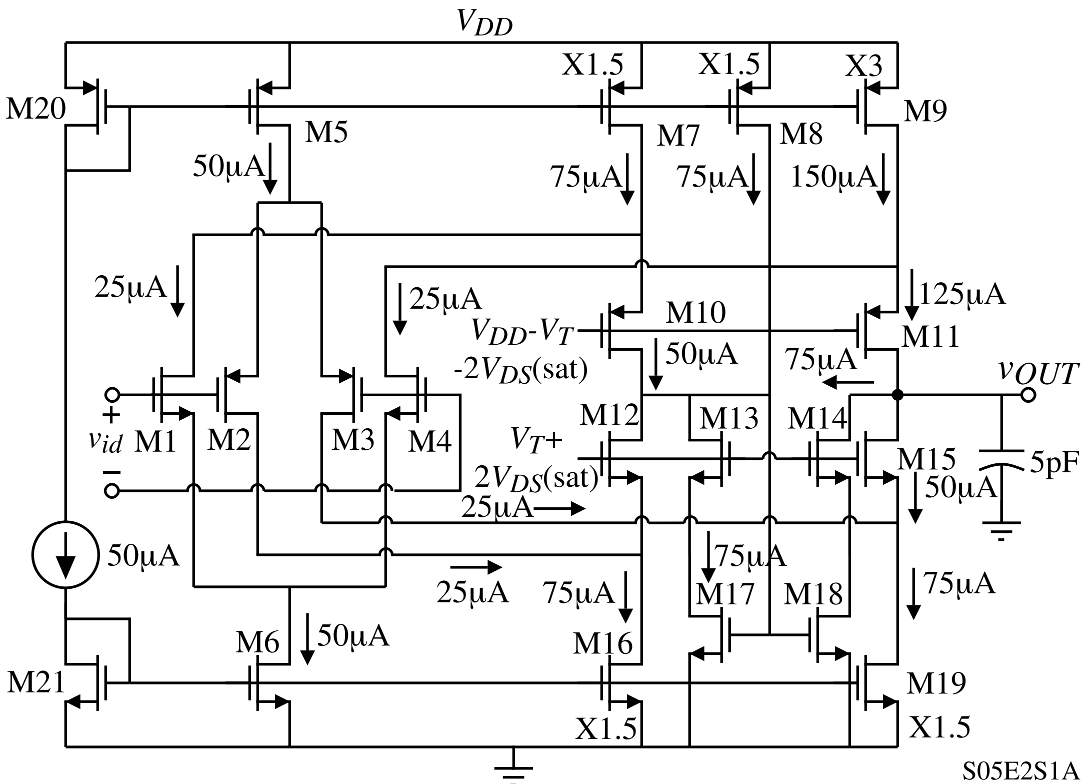
EXAMINATION NO. 2 - SOLUTIONS

(Average Score = 77/100)

Problem 1 - (50 points)

The CMOS op amp shown uses a complementary differential input stages to achieve a wider input voltage common mode range. Assume that all transistors are scaled from a X1 NMOS and PMOS that have been designed to have a small-signal transconductance of 100µS and a channel conductance of 1µS at 25µA of current. Use what you have learned in class to give your best estimate of the slew rate (V/µs), output resistance, R_{out}, small-signal voltage gain (v_{out}/v_{id}), and the gainbandwidth, GB, in MHz.



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Solution

The dc currents for $v_{id} = 0$ are shown above. One can show that the maximum amount of current available to the output capacitor is twice the 50µA current sink/source or 100µA. Therefore, the slew rate is SR = 100µA/5pF = 20V/µs.

The small-signal voltage gain can be written by inspection as (note the M13-M14-M17-M18 combination is used to recover the full differential output of both complementary input stages),

$$\frac{v_{out}}{v_{id}} = (g_{m1}+g_{m2})R_{out} \text{ where } g_{m1} = g_{m2} = 100\mu\text{S}$$

$$R_{out} \approx [(r_{ds9}||r_{ds4})g_{m11}r_{ds11}]||(r_{ds18}g_{m14}r_{ds14})||\ [(r_{ds3}||r_{ds19})g_{m15}r_{ds15}]$$

Scaling r_{ds} for the currents gives,

$$r_{ds9} = 1000\text{k}\Omega/6 = 166.7\text{k}\Omega,\ r_{ds11} = 1000\text{k}\Omega/5 = 200\text{k}\Omega,$$

$$r_{ds18} = r_{ds14} = r_{ds19} = 1000\text{k}\Omega/3 = 333.3\text{k}\Omega,\ r_{ds15} = 1000\text{k}\Omega/2 = 500\text{k}\Omega$$

Problem 1 – Continued

Scaling g_m for the currents gives,

$$g_{m11} = \sqrt{5}\ 100\mu S = 223.6\mu S,\ g_{m14} = \sqrt{3}\ 100\mu S = 173\mu S,\ g_{m15} = \sqrt{2}\ 100\mu S = 141\mu S$$

$\therefore\ R_{out} \approx$

$$[(167||1000)(0.224)(200k\Omega)]||[(333)(0.173)(333.3k\Omega)]||[(333||1000)(0.173)(500k\Omega)]$$

$$R_{out} = 6.390M\Omega||19.18M\Omega||17.62M\Omega = \underline{\underline{3.768M\Omega}}$$

Now,

$$\frac{v_{out}}{v_{id}} = 200\mu S(3.768M\Omega) = \underline{\underline{769\ V/V}}$$

The gainbandwidth is,

$$GB = \frac{g_{m1}+g_{m2}}{C_L} = \frac{200\mu S}{5pF} = 40x10^6 \text{ rads/sec or } \underline{\underline{6.28MHz}}$$

Problem 2 - (25 points)

If a two-stage, Miller compensated CMOS op amp has a RHP zero at $5GB$, a dominant pole due to the Miller compensation, and a second pole at $-p_2$, find the value of the first stage transconductance (g_{mI}), the second stage transconductance (g_{mII}), and the value of the Miller capacitor, C_c, if GB = 10MHz, the load capacitor is 10pF, and the phase margin is to be 50°. Assume that the unity gain magnitude frequency is GB.

Solution

1.) The phase margin gives p_2 which will give g_{mII}.

$$180° - 90° - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}(0.2) = 50° \qquad \rightarrow \tan^{-1}\left(\frac{GB}{|p_2|}\right) = 28.69°$$

$$\therefore \quad |p_2| = \frac{GB}{0.544} = \frac{20\pi\text{MHz}}{0.544} = 115.5\text{x}10^6 \text{ rads/sec.}$$

We know that,

$$|p_2| = \frac{g_{mII}}{C_L} \qquad \rightarrow \qquad g_{mII} = |p_2|C_L = (115.5\text{x}10^6 \text{ rads/sec.})(10\text{pF}) = \underline{\underline{1.155\text{mS}}}$$

2.) The Miller capacitor is found from the RHP zero location.

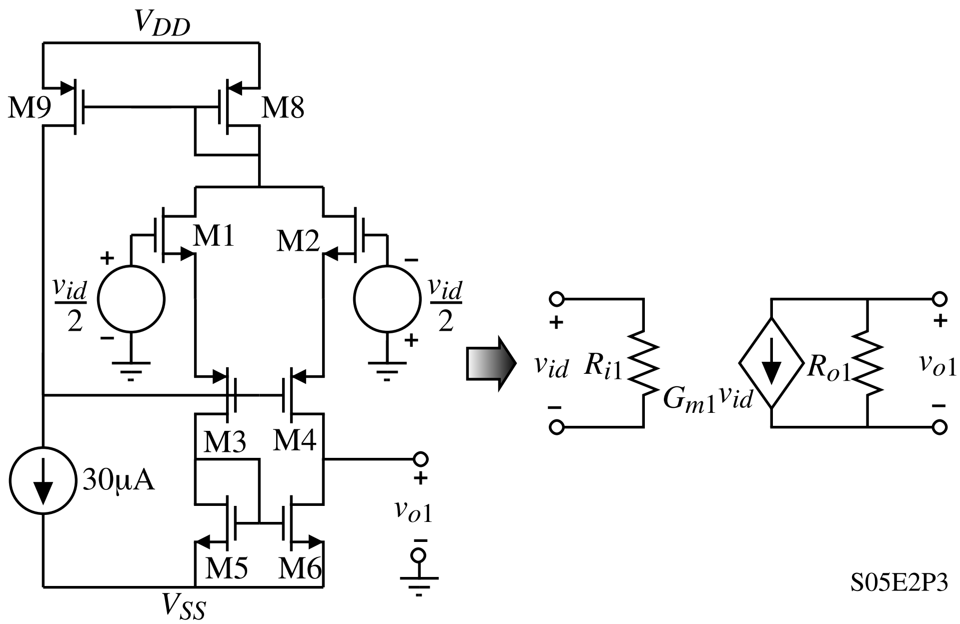
$$\frac{g_{mII}}{C_c} = z_1 \qquad \rightarrow \qquad C_c = \frac{g_{mII}}{z_1} = \frac{1.115\text{mS}}{5\cdot GB} = \frac{1.115\text{mS}}{10\pi\text{x}10^7} = \underline{\underline{3.55\text{pF}}}$$

3.) Finally, the input stage transconductance is given by,

$$GB = \frac{g_{mI}}{C_c} \qquad \rightarrow \qquad g_{mI} = GB\cdot C_c = (2\pi\text{x}10^7)(3.55\text{pF}) = \underline{\underline{223\mu\text{S}}}$$

Problem 3 - (25 points)

The CMOS equivalent of a 741 op amp input stage is shown. If the transistor model parameters are $K_N' = 300\mu A/V^2$, $V_{TN} = 0.5V$, $\lambda_N = 0.02V^{-1}$ and $K_P' = 70\mu A/V^2$, $V_{TP} = -0.5V$, $\lambda_P = 0.04V^{-1}$ find the numerical values of R_{i1}, G_{m1}, and R_{o1} for this input stage if all W/L's of every transistor are 10.



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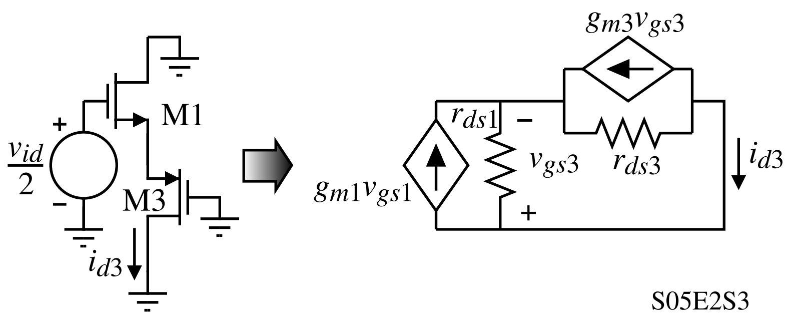
Solution

The small-signal model for this problem is shown. First find the small-signal model parameters:



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$g_{m1} = g_{m2} = \sqrt{2\cdot 300\cdot 10\cdot 15} = 300\mu S$

$g_{m3} = g_{m4} = \sqrt{2\cdot 70\cdot 10\cdot 15} = 145\mu S$

$r_{ds1} = r_{ds2} = r_{ds5} = r_{ds6} = 50/15\mu A = 3.33M\Omega$ and $r_{ds3} = r_{ds4} = 25/15\mu A = 1.67M\Omega$

Summing currents:

$$g_{m1}v_{gs1}+\frac{v_{gs3}}{r_{ds1}}+\frac{v_{gs3}}{r_{ds3}}+g_{m3}v_{gs3} = 300v_{gs1}+0.3v_{gs1}+0.6v_{gs3}+145v_{gs3} = 0$$

$$300.3v_{gs1}+145.6v_{gs3} = 0 \quad \rightarrow \quad v_{gs1} = -0.485v_{gs3}$$

Voltage loop through M1 and M3:

$$0.5g_{m1}v_{id} = v_{gs1} - v_{gs3} = -1.485v_{gs3} \quad \rightarrow \quad v_{gs3} = -0.337v_{id}$$

$$i_{d3} \approx -g_{m3}v_{gs3} = 0.337\cdot 145\mu S v_{id} = 48.82\mu S\ v_{id}$$

$$G_{m1}v_{id} = (i_{d3}+ i_{d4}) = 97.65\mu S\ v_{id} \qquad \therefore\ G_{m1} = \underline{\underline{97.65\mu S}} \qquad R_{i1} = \underline{\underline{\infty}}$$

Ouput resistance:

$$R_{o1} = r_{ds6}||[(1/g_{m2})g_{m4}r_{ds4}] = 3.33M\Omega||0.807M\Omega = \underline{\underline{0.650M\Omega}}$$