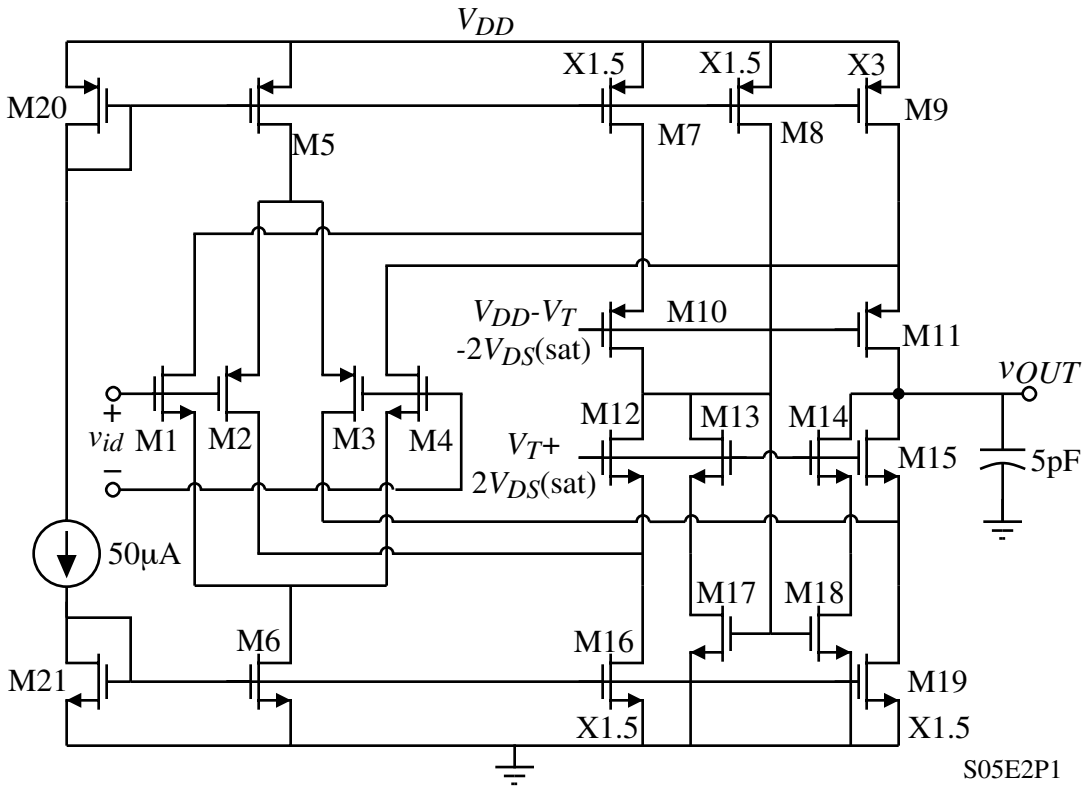
EXAMINATION NO. 2

NAME_____SCORE_____/100

INSTRUCTIONS: This exam is closed book with one sheet of notes permitted. The exam consists of 3 questions for a total of 100 points. Please show your work leading to your answers so that maximum partial credit may be given where appropriate. Be sure to turn in your exam with the problems in numerical order, firmly attached together.

Problem 1 - (50 points)

The CMOS op amp shown uses a complementary differential input stages to achieve a wider input voltage common mode range. Assume that all transistors are scaled from a X1 NMOS and PMOS that have been designed to have a small-signal transconductance of 100μS and a channel conductance of 1μS at 25μA of current. Use what you have learned in class to give your best estimate of the slew rate (V/μs), small-signal voltage gain (v_{out}/v_{id}), output resistance, R_{out}, and the gainbandwidth, GB, in MHz.



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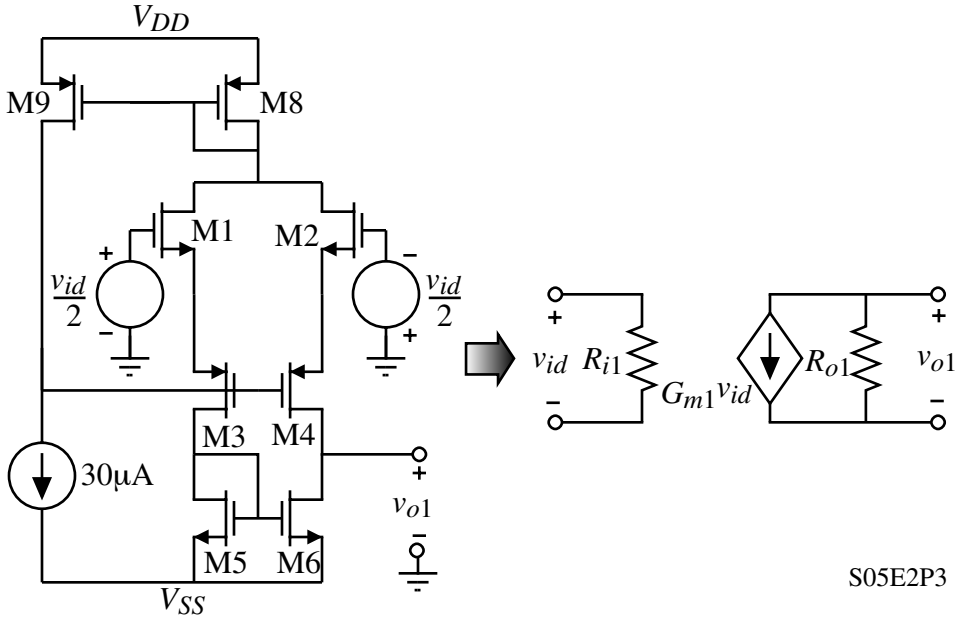
Problem 1 – Continued

Problem 2 - (25 points)

If a two-stage, Miller compensated CMOS op amp has a RHP zero at $5GB$, a dominant pole due to the Miller compensation, and a second pole at $-p_2$, find the value of the first stage transconductance ($g_{m\mathrm{I}}$), the second stage transconductance ($g_{m\mathrm{II}}$), and the value of the Miller capacitor, C_c, if GB = 10MHz, the load capacitor is 10pF, and the phase margin is to be 50°. Assume that the unity gain magnitude frequency is GB.

Problem 3 - (25 points)

The CMOS equivalent of a 741 op amp input stage is shown. If the transistor model parameters are $K_N' = 300\mu A/V^2$, $V_{TN} = 0.5V$, $\lambda_N = 0.02V^{-1}$ and $K_P' = 70\mu A/V^2$, $V_{TP} = -0.5V$, $\lambda_P = 0.04V^{-1}$ find the numerical values of R_{i1}, G_{m1}, and R_{o1} for this input stage if all W/L's of every transistor are 10.



Extra Sheet