EXAMINATION NO. 3 - SOLUTIONS

(Average score = 65/100)

Problem 1 – Alan Hasting's Lecture (20 points)

All questions are worth 4 points.

1.) What is the difference between random and systematic mismatches in IC layout?

Random mismatches are due to inherent uncertainty in the fabrication process and cannot be eliminated. There are represented by the standard deviation of a parameter. Systematic mismatches are due to process biases and can be eliminated. Systematic mismatches are represented by the average or mean of a parameter.

2.) Give two ways in which random mismatches can be reduced.

1.) Make the circuit bigger – sacrifice speed

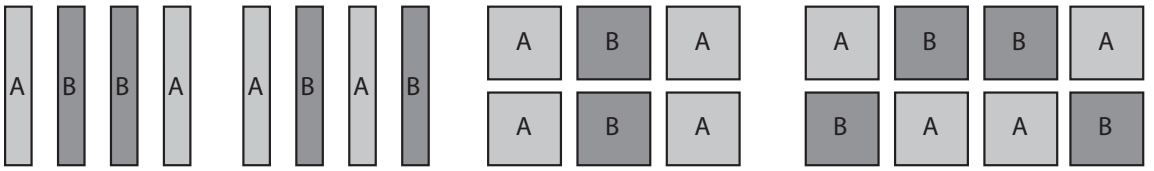
2.) Redesign the circuit

3.) What is the difference in collector current between two identical BJTs whose base-emitter voltages are identical when there is 1°C difference in operating temperature at room temperature?

The base-emitter voltage decreases approximately -2mV/°C. A 2mV difference gives 8% difference in collector currents. The calculations to support this are:

$$\frac{I_s\exp(V_{BE}/V_t)}{I_s\exp[(V_{BE}\text{-}2\text{mV})/V_t]} = \frac{\exp(V_{BE}/V_t)}{\exp(V_{BE}/V_t)\exp(\text{-}2\text{mV}/V_t)} = \exp(2\text{mV}/25.9\text{mV}) = 1.08$$

4.) Which of the following structures have common centroids?



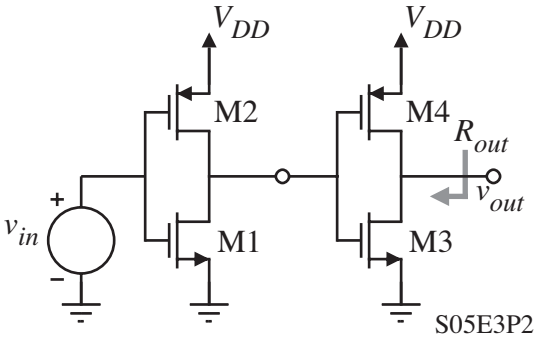
Common centroid | No common centroid | Common centroid | Common centroid

5.) Order the various rules for layout matching in order of importance. Place the number 1, 2, 3, or 4 beside the appropriate rule to indicate the importance (1 being the most important and 4 the least important).

Coincidence (1) Symmetry (3) Dispersion (4) Compactness (2)

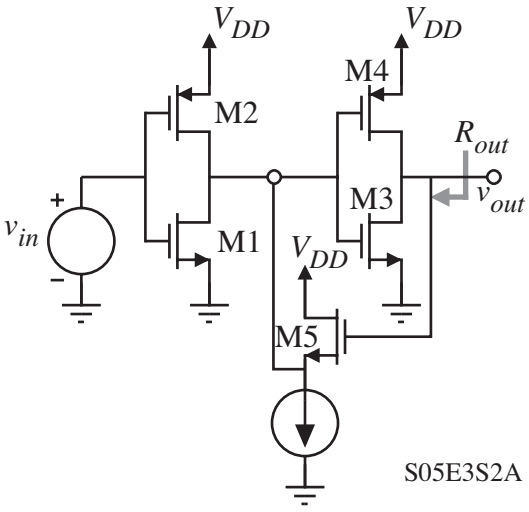
Problem 2 – (40 points)

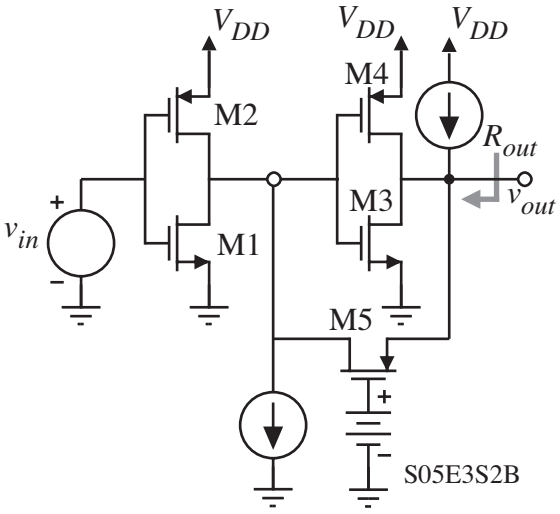
A simple amplifier consisting of two cascaded CMOS inverters is shown. By using one transistor (either NMOS or PMOS) and ideal current sources and batteries as necessary, show how you would reduce the output resistance to as small as possible. Estimate the output resistance of your circuit assuming that all transistors (those in the amplifier and the one you use) have the same value of g_m and r_{ds}. Further assume, that the CMOS inverters are operating in class AB.



Solution

There are two possibilities which will be examined below.





$R_{out}(\text{no fb.}) = 0.5 r_{ds}$

Loop gain $\approx 1 \cdot g_m r_{ds}$

$$R_{out}(\text{fb.}) \approx \frac{0.5 r_{ds}}{g_m r_{ds}} = \frac{1}{2 g_m}$$

$R_{out}(\text{no fb.}) \approx 1/g_m$

Loop gain $\approx 2\, g_m (r_{ds}/3) = 0.667\, g_m r_{ds}$

$$R_{out}(\text{fb.}) \approx \frac{1/g_m}{0.667 g_m r_{ds}} = \frac{3}{2 g_m^2 r_{ds}}$$

Therefore, the solution on the right has a low resistance by the amount of $3/g_m r_{ds}$.

10 points base

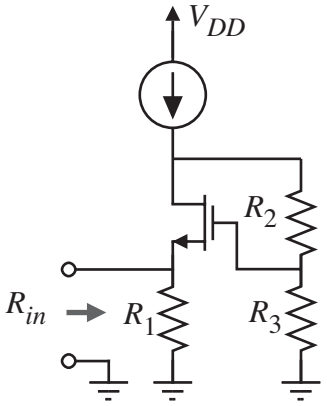
20 points for a workable solution

30 points for a workable solution with the correct supporting calculations

40 points for the optimum solution with the correct supporting calculations

Problem 3 - (40 points)

Use Blackmnn's formula to calculate the small-signal input resistance, R_{in}, of the circuit shown. Your answer should be in terms of the resistances R_1, R_2, R_3, g_m, and r_{ds}. Simplify your answer if $g_m r_{ds} >> 1$. Blackman's formula is,

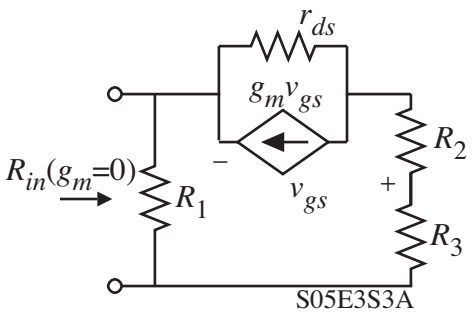


$$R_{in} = R_{in}(g_m=0)\left[\frac{1 + RR(\text{port shorted})}{1 + RR(\text{port opened})}\right]$$

Solution

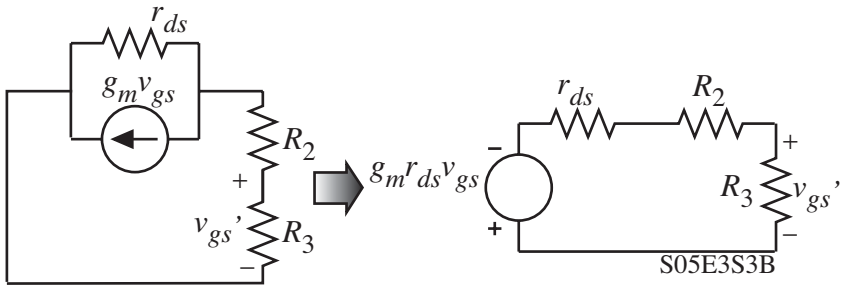
$R_{in}(g_m=0)$:

$$R_{in}(g_m=0) = R_1 \| (r_{ds} + R_2 + R_3)$$



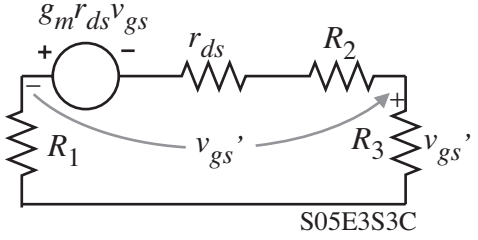
RR(port shorted):

$$RR(0) = \frac{-g_m r_{ds} R_3}{r_{ds} + R_2 + R_3}$$



RR(port opened):

$$RR(\infty) = \frac{-g_m r_{ds}(R_1 + R_3)}{r_{ds} + R_1 + R_2 + R_3}$$



Therfore,

$$R_{in} = \frac{R_1(r_{ds} + R_1 + R_3)}{r_{ds} + R_1 + R_2 + R_3}\left[\frac{1 + \dfrac{g_m r_{ds} R_3}{r_{ds} + R_2 + R_3}}{1 + \dfrac{g_m r_{ds}(R_1 + R_3)}{r_{ds} + R_1 + R_2 + R_3}}\right]$$

$$= R_1\left[\frac{r_{ds} + R_2 + R_3 + g_m r_{ds} R_3}{r_{ds} + R_1 + R_2 + R_3 + g_m r_{ds}(R_1 + R_3)}\right] = R_1\left[\frac{r_{ds} + R_2 + R_3(1 + g_m r_{ds})}{r_{ds} + R_1 + (R_2 + R_3)(1 + g_m r_{ds})}\right]$$

$$R_{in} \approx \frac{R_1 R_3}{R_1 + R_3} \text{ if } g_m r_{ds} >> 1.$$