Homework Assignment No. 3

Due Monday, January 31, 2005 in class

Problem 1 - (10 points) (Prob. 7.1 of 3rd and 4th edition)

(a) Use the Miller approximation to calculate the –3dB frequency of the small-signal voltage gain of a common-emitter transistor stage as shown in Fig. 7.2a using the following transistor parameters:

$R_S = 5\text{k}\Omega$ $r_b = 300\Omega$ $I_C = 0.5\text{mA}$ $\beta = 200$ $f_T = 500\text{MHz}$ (at $I_C = 0.5\text{mA}$)

$C_\mu = 0.3\text{pF}$ $R_L = 3\text{k}\Omega$ $C_{cs} = 0$ $V_A = \infty$

(b) Calculate the nondominant pole magnitude for the circuit in (a). Compare your answer with a SPICE simulation.

Problem 2 - (10 points) (Prob. 7.2 of 4th edition)

Repeat Problem 1 for the MOS common-source stage shown using $R_I = 10\text{k}\Omega$, $R_L = 5\text{k}\Omega$, $I_D = 0.5\text{mA}$, and the following NMOS transistor data:

$W = 100\mu\text{m}$, $L_{drawn} = 2\mu\text{m}$, $L_d = 0.2\mu\text{m}$, $X_d = 0$, $\lambda = 0$, $k'_n = 60\mu\text{A/V}^2$, $\gamma = 0$, $C_{sb} = C_{db} = 0$, $C_{ox} = 0.7\text{fF}/\mu\text{m}^2$, and $C_{gd} = 14\text{fF}$.

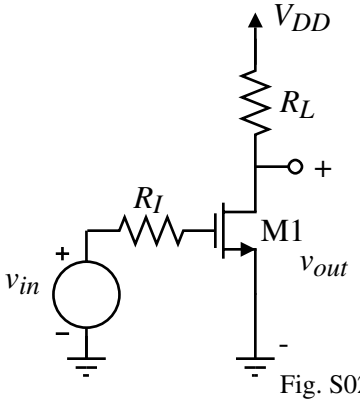

Fig. S02H3P2

Problem 3 - (10 points) (Prob. 7.5 of 3rd and 7.8 of the 4th edition)

A lateral *pnp* emitter follower has $R_S = 250\Omega$, $r_b = 200\Omega$, $\beta = 50$, $I_C = -300\mu\text{A}$, $f_T = 4$ MHz, $R_E = 4\text{k}\Omega$, $C_\mu = 0$, and $r_o = \infty$. Calculate the small-signal voltage gain as a function of frequency. Sketch the magnitude of the voltage gain in decibels from $f = 10\text{kHz}$ to $f = 20$ MHz, using a log frequency scale.

Problem 4 - (10 points) (Prob. 7.6 of 3rd and 7.9 of the 4th edition)

Calculate the values of the elements in the small-signal equivalent circuits for the input and output impedances of the emitter follower of the previous problem. Sketch the magnitudes of these impedances as a function of frequency from $f = 10\text{kHz}$ to $f = 20$ MHz, using log frequency scales. Use SPICE to determine the small-signal step response of the circuit for a resistive load of 1kΩ and then a capacitive load of 400pF. Use a 1-mV input pulse amplitude with zero rise time. Comment on the shape of the time-domain responses. (Bias the circuit with an ideal 300μA current source connected to the emitter for the capacitive load test.)

Problem 5 (40 points) - Design Problem #1

You are to design a CMOS output amplifier having a single-ended input and single-ended output and a voltage gain of +1. This amplifier is to use ±2V power supplies and all W/L values should be between 1 and 100. You may only use MOSFETs or substrate or vertical BJTs (only one type, NPN) in your design with the exception of a load capacitor (C_L) and load resistor (R_L). You should use the following model parameters for SPICE. Use $\beta_F = 100$ and $I_s = 10$fA for the BJT.

	K' (μA/V^2)	V_T (V)	$\gamma(\sqrt{\text{V}})$	$2\phi_F$(V)	λ (V^{-1})
NMOS	110	0.7	0.4	0.7	0.04(L=1μm) 0.01(L=2μm)
PMOS	50	-0.7	0.57	0.8	0.05(L=1μm) 0.01(L=2μm)

The various definitions used in the specifications of this design are:

1.) Slew rate (SR) is the smallest ±output voltage rate across a 1nF load capacitance when the output voltage is between ±1V.

2.) The peak output voltage (V_P) is the maximum ±deviation from the quiescent output voltage when a sinusoid is applied to the input and a 100Ω resistor is attached to the output.

3.) Efficiency in percent (η) is defined as

$$\eta = \left(\frac{\text{Power to the load resistor of 100}\Omega}{\text{Power from the supplies}}\right)\text{x}100$$

4.) Voltage gain (A_v) is the output voltage (peak-to-peak) over the input voltage (peak-to-peak) when the output is loaded with a 100Ω load resistor.

Your score for this problem will be determined as follows:

$$\text{SCORE} = 1.0\text{x}10^6 \cdot \min[SR, 10\text{V}/\mu\text{s}] + 10 \cdot \min[V_P, 1] + 0.4 \cdot \min[\eta, 25] + \frac{10}{|A_v - 1| + 1}$$