Homework Assignment No. 6 - Solutions

Problem 1 - (10 points)

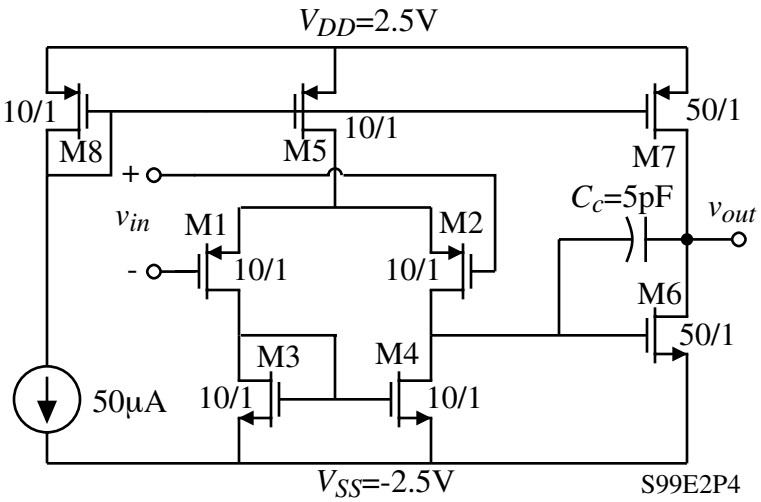
For the CMOS op amp shown, find the following quantities.

1.) Slew rate (V/sec.)

2.) Positive and negative output voltage limits (all transistors remain in saturation)

3.) Positive and negative input common voltage limits (all transistors remain in saturation and use nominal parameter values)

4.) Small signal voltage gain



5.) Unity-gainbandwidth (MHz) and 6.) Power dissipation (mW).

Solution

1.) $SR = \frac{I_5}{C_c} = \frac{50\mu A}{5pF} = 10^7 V/second \quad \Rightarrow \quad \boxed{SR = 10^7 V/sec}$

2.) $V_{SD7} = \sqrt{\frac{2I_7}{K_P(W/L)}} = \sqrt{\frac{500\mu A}{50 \cdot 50}} = 0.447V$ and $V_{DS6} = \sqrt{\frac{500\mu A}{110 \cdot 50}} = 0.3015V$

$\therefore \boxed{V_{out}(max) = 2.5\text{-}0.447 = 2.053V}$ &

$\boxed{V_{out}(min) = -2.5V + 0.3015V = -2.198V}$

3.) ICM (min) = $-2.5V + V_{GS3} - |V_{TP}| = -2.5V + \sqrt{\frac{2 \cdot 25}{110 \cdot 10}} + 0.7V - 0.7V$

$\therefore ICM(min) = -2.5 + 0.213 = -2.287V \quad \Rightarrow \quad \boxed{ICM(min) = -2.287V}$

$ICM(max) = ? \quad V_{SD5}(sat) = \sqrt{\frac{2 \cdot 50}{50 \cdot 10}} = 0.4472V$ and $V_{SG1} = \sqrt{\frac{2 \cdot 25}{50 \cdot 10}} + 0.7 = 1.016V$

$\therefore ICM(max) = 2.5 - V_{SD5}(sat) - V_{SG1} = 2.5 - 0.4472 - 1.016 = 1.0366V$

$\boxed{ICM(max) = 1.0366V}$

4.) $A_v = \frac{g_{m1}g_{m6}}{(g_{sd2}+g_{ds4})(g_{ds6}+g_{sd7})} \qquad g_{m1} = \sqrt{\frac{2K_P W_1 I_1}{L_1}} = \sqrt{2 \cdot 50 \cdot 10 \cdot 25} = 158\mu S$

$g_{m6} = \sqrt{\frac{2K_P W_6 I_6}{L_6}} = \sqrt{2 \cdot 110 \cdot 50 \cdot 250} = 1658\mu S \qquad G_I = 0.09 \cdot 25\mu A = 2.25\mu S$

and $G_{II} = 0.09 \cdot 250\mu A = 22.5\mu S$

$\therefore \quad A_v = \frac{158 \cdot 1658}{2.25 \cdot 22.5} = 3{,}489V/V \quad \Rightarrow \quad \boxed{A_v = 5{,}176V/V}$

5.) $GB = \frac{g_{m1}}{C_c} = \frac{158\mu S}{5pF} = 31.6Mrads/sec \quad \Rightarrow \quad \boxed{GB = 5.03MHz}$

6.) $P_{diss} = 5x350\mu A = 1.75mW \quad \Rightarrow \quad \boxed{P_{diss} = 1.75mW}$

Problem 2 - (10 points)

Bias current calculation:

$$V_{T8} + V_{ON8} + I_8.R_S = V_{dd} - V_{ss} \quad \text{or,} \qquad V_{T8} + \sqrt{\frac{2.I_8}{3.K_p'}} = 5 - I_8.R_s \ . \tag{1}$$

Solving for I_8 quadratically would give, I_8 _36μA_, I_5 _36μA_, and I_7 _60μA_

Using the formula, $g_m = \sqrt{2.K' \frac{W}{L} I}$ and $g_{ds} = \lambda I$ we get,

$$g_{m2} = 60\mu S \ , \ g_{ds2} = 0.9\mu S \ , \ g_{ds4} = 0.72\mu S \tag{2}$$

$$g_{m6} = 363\mu S \ , \ g_{ds6} = 3\mu S \ , \ g_{ds7} = 2.4\mu S \tag{3}$$

Small-signal open-loop gain:

The small-signal voltage gain can be expressed as,

$$A_{V1} = \frac{-g_{m2}}{(g_{ds2} + g_{ds4})} = -37 \quad \text{and} \quad A_{V2} = \frac{-g_{m6}}{(g_{ds6} + g_{ds7})} = -67$$

Thus, total open-loop gain is,

$$A_v = A_{v1} \cdot A_{v2} = \underline{2489 \text{V/V}} \tag{3}$$

Output resistance:

$$R_{out} = \frac{1}{(g_{ds6} + g_{ds7})} = 185K\Omega \tag{5}$$

Power dissipation:

$$P_{diss} = 5(36 + 36 + 60)\mu W = 660\mu W \tag{6}$$

ICMR:

$$V_{in,\max} = 2.5 - V_{T1} - V_{ON1} - V_{ON5} = 0.51V \tag{7}$$

$$V_{in,\min} = -2.5 - V_{T1} + V_{T3} + V_{ON3} = -2.21V \tag{8}$$

Output voltage swing:

$$V_{0,\max} = 2.5 - V_{ON7} = 1.81V \tag{9}$$

Slew Rate:

Slew rate under no load condition can be given as,

$$SR = \frac{I_5}{C_C} = 6V / \mu s$$

In presence of a load capacitor of 20 pF, slew rate would be,

$$SR = \min\left[\frac{I_5}{C_c}, \frac{I_7}{C_L}\right]$$

Problem 6.3-7 - Continued

CMRR:

Under perfectly balanced condition where $I_1 = I_2$, if a small signal common-mode variation occurs at the two input terminals, the small signal currents $i_1 = i_2 = i_3 = i_4$ and the differential output current at node (7) is zero. So, ideally, common-mode gain would be zero and the value for CMRR would be infinity.

GBW:

Let us design M9 and M10 first. Both these transistors would operate in triode region and will carry zero dc current. Thus, $V_{ds9} = V_{ds10} \cong 0$. The equation of drain current in triode region is given as,

$$I_D \cong K' \frac{W}{L}(V_{GS} - V_T)V_{DS} .$$

The on resistance of the MOS transistor in triode region of operation would be,

$$R_{ON} = K' \frac{W}{L}(V_{GS} - V_T) .$$

It is intended to make the effective resistance of M9 and M10 equal to $\frac{1}{g_{m6}}$.

So,
$$K'_9\left(\frac{W_9}{L_9}\right)(V_{GS9}\text{-}V_{T9}) + K'_{10}\left(\frac{W_{10}}{L_{10}}\right)(V_{GS10}\text{-}V_{T10}) = g_{m6} \qquad (11)$$

$$V_{D4} = V_{D3} = -2.5 + V_{T3} + V_{ON3} = -1.51V$$

Thus,

$$V_{GS9} \cong 4V \quad \text{and} \quad V_{GS10} \cong -1V .$$

Putting the appropriate values in (11), we can solve for the aspect ratios of M9 and M10. One of the solutions could be,

$$K'_9\left(\frac{W_9}{L_9}\right) = \frac{1}{1} \quad \text{and} \quad K'_{10}\left(\frac{W_{10}}{L_{10}}\right) = \text{very small} \qquad (12)$$

The dominant pole could be calculated as,

$$p_1 = \frac{-(g_{ds4} + g_{ds2})}{2\pi . A_{V1} . C_C} = -1.16KHz.$$

And the load pole would be,

$$p_2 = \frac{-g_{m6}}{2\pi . C_L} = -2.8MHz. \quad \text{for a 20 pF load.}$$

It can be noted that in this problem, the product of the open-loop gain and the dominant pole is approximately equal to the load pole. Thus, the gain bandwidth is approximately equal to 2.8 MHz and the phase margin would be close to 45 degrees.

Problem 6.3-7 - Continued

PSRR:

If a small ripple v_S is applied at the V_{dd} terminal, then the gain of this ripple from this terminal to the output can be expressed as,

$$\frac{v_o}{v_s} = \frac{\left(1-\frac{R_S}{R_S+(1/g_{m8})}\right)g_{m7}}{g_{ds6}+g_{ds7}} = 2.8\text{V/V}$$

Thus, PSRR due to variations in V_{dd} would be, $A_V / 2.8 = 2489/2.8 = 889$.

SPICE file:

```
.model nmos nmos vto=0.7 lambda=0.04 kp=110u
.model pmos pmos vto=-0.8 lambda=0.05 kp=50u

vdd 1 0 dc 2.5 ac 0
vss 10 0 dc -2.5 ac 0
vinp 5 0 dc 0 ac 1
*vinn 4 0 dc 0 ac 0

m8 2 2 1 1 pmos w=3u l=1u
rs 2 10 100k
m5 3 2 1 1 pmos w=3u l=1u
m1 6 8 3 3 pmos w=2u l=1u
m2 7 5 3 3 pmos w=2u l=1u
m3 6 6 10 10 nmos w=4u l=1u
m4 7 6 10 10 nmos w=4u l=1u
m7 8 2 1 1 pmos w=5u l=1u
m6 8 7 10 10 nmos w=10u l=1u
cc 7 9 6p
cl 8 0 20p
m9 8 1 9 9 nmos w=1u l=1u
m10 8 10 9 9 pmos w=1u l=100u

.op
.ac dec 10 1 100meg
.option post
.end
```

Operating points:

```
****  mosfets


subckt
element  0:m8       0:m5       0:m1       0:m2       0:m3       0:m4
model    0:pmos     0:pmos     0:pmos     0:pmos     0:nmos     0:nmos
region      Cutoff     Cutoff     Cutoff     Cutoff    Saturati   Saturati
 id       -35.3708u  -34.8506u  -17.4107u  -17.4399u   17.4107u   17.4399u
 ibs       0.         0.         0.         0.         0.         0.
 ibd        14.6292f   11.4726f   28.7676f   28.3314f   -9.7598f  -10.1959f
```

Problem 6.3-7 - Continued

```
 vgs       -1.4629    -1.4629    -1.3517    -1.3527   975.9818m  975.9818m
 vds       -1.4629    -1.1473    -2.8768    -2.8331   975.9818m    1.0196
 vbs       0.         0.         0.         0.        0.         0.
 vth       -800.0000m -800.0000m -800.0000m -800.0000m  700.0000m
700.0000m
 vdsat   -662.9217m -662.9217m -551.7476m -552.7377m 275.9818m
275.9818m
 beta      160.9719u  158.6045u  114.3838u  114.1657u  457.1773u  457.9449u
 gam  eff   527.6252m 527.6252m 527.6252m 527.6252m 527.6252m 527.6252m
 gm        106.7118u  105.1423u   63.1110u   63.1037u  126.1726u  126.3844u
 gds         1.6480u    1.6480u  761.0636n  763.7975n  670.2604n  670.2604n
 gmb        36.9704u   36.4266u   21.8648u   21.8623u   43.7126u   43.7860u
 cdtot     2.021e-18  1.585e-18  2.649e-18  2.609e-18  1.797e-18  1.878e-18
 cgtot     7.005e-16  7.000e-16  4.693e-16  4.692e-16  9.467e-16  9.467e-16
 cstot     6.906e-16  6.906e-16  4.604e-16  4.604e-16  9.208e-16  9.208e-16
 cbtot     7.806e-18  7.806e-18  6.216e-18  6.205e-18  2.402e-17  2.402e-17
 cgs       6.906e-16  6.906e-16  4.604e-16  4.604e-16  9.208e-16  9.208e-16
 cgd       2.021e-18  1.585e-18  2.649e-18  2.609e-18  1.797e-18  1.878e-18


subckt
element  0:m7       0:m6       0:m9       0:m10
model    0:pmos     0:nmos     0:nmos     0:pmos
region       Cutoff   Saturati    Linear     Cutoff
 id       -61.7971u   61.7971u    0.         0.
 ibs       0.         0.         0.         0.
 ibd       24.9901f  -25.0099f   0.         0.
 vgs       -1.4629     1.0196     2.4990    -2.5010
 vds       -2.4990     2.5010     0.         0.
 vbs       0.         0.         0.         0.
 vth       -800.0000m  700.0000m  700.0000m -800.0000m
 vdsat   -662.9217m  319.5939m    0.         0.
 beta      281.2376u    1.2100m  110.0000u  500.0000n
 gam  eff   527.6252m  527.6252m  527.6252m  527.6252m
 gm        186.4385u  386.7225u    0.         0.
 gds         2.7467u    2.2471u  197.8911u  850.4951n
 gmb        64.5917u  133.9802u    0.         0.
 cdtot     5.753e-18  1.152e-17  1.727e-16   17.2658f
 cgtot      1.1698f    2.3660f  3.463e-16   34.6349f
 cstot      1.1511f    2.3021f  1.727e-16   17.2658f
 cbtot     1.301e-17  5.233e-17  9.769e-19  1.033e-16
 cgs        1.1511f    2.3021f  1.727e-16   17.2658f
 cgd       5.753e-18  1.152e-17  1.727e-16   17.2658f
```

Results from SPICE simulation:

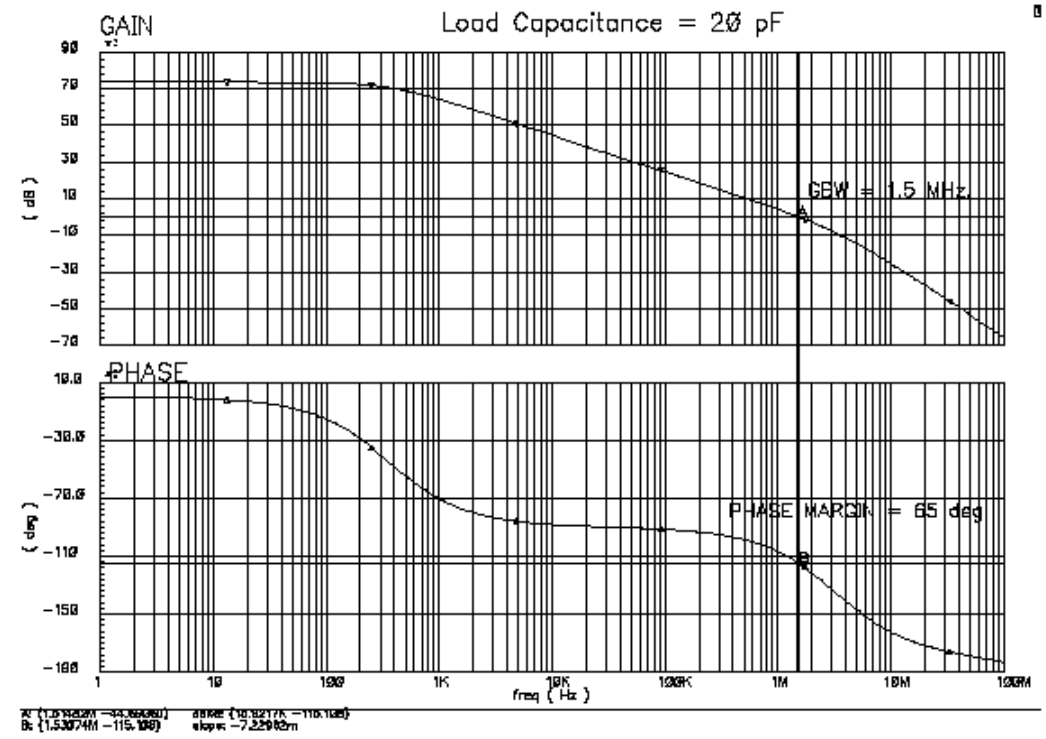
i. Unloaded output (load capacitor = 0)

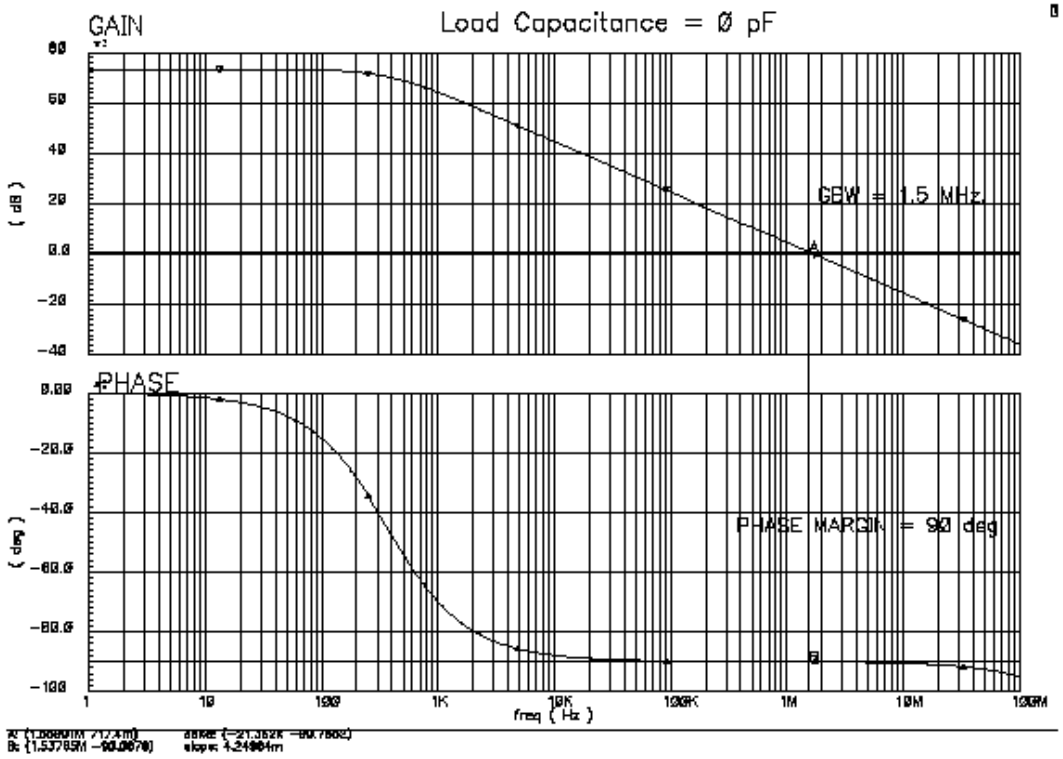
GBW = 1.5 MHz., Phase Margin = 90 deg, 1% settling time = 0.39 us.

ii. Loaded output (load capacitor = 20 pF)

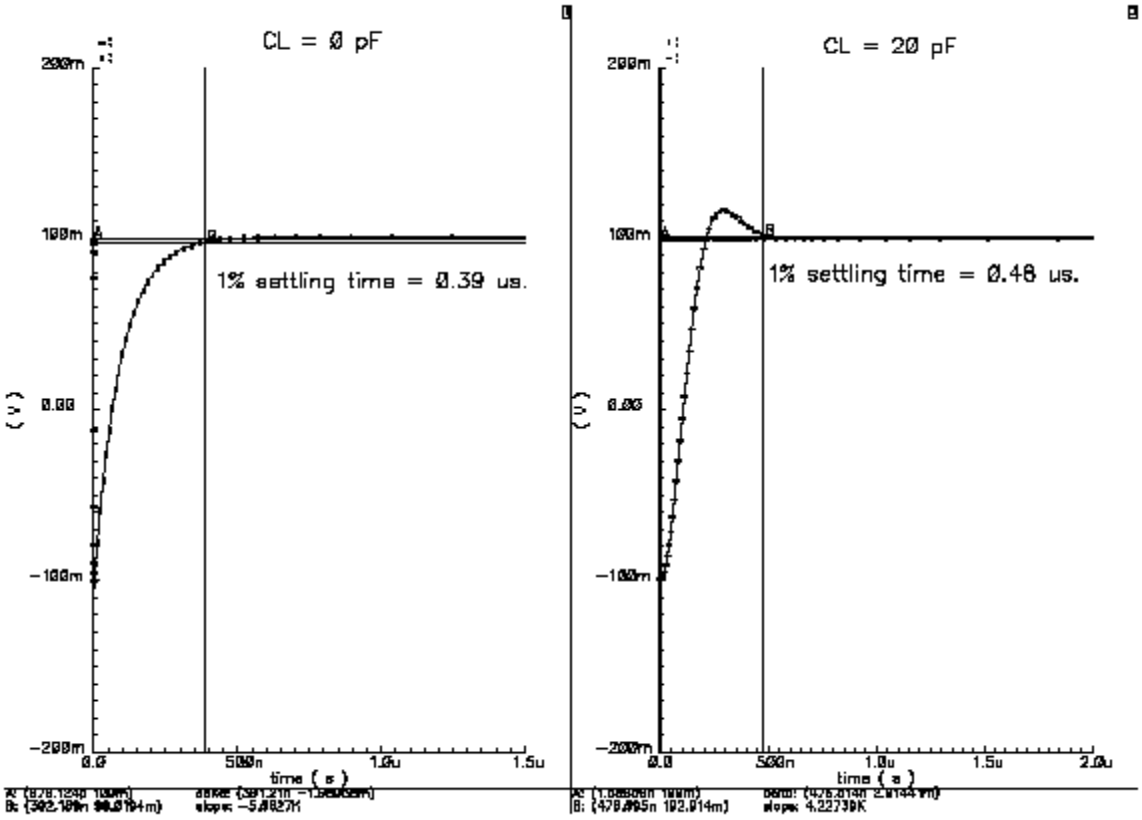
GBW = 1.5 MHz., Phase Margin = 65 deg, 1% settling time = 0.48 us.

Problem 6.3-7 - Continued





Problem 6.3-7 - Continued



Problem 3 - (10 points)

Small signal differential voltage gain:

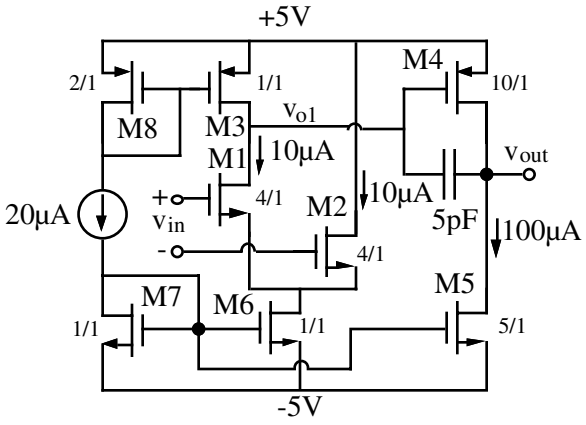
By intuitive analysis methods,

$$\frac{v_{o1}}{v_{in}} = \frac{-0.5g_{m1}}{g_{ds1} + g_{ds3}}$$

and

$$\frac{v_{out}}{v_{o1}} = \frac{-g_{m4}}{g_{ds4} + g_{ds5}}$$

$$\therefore \quad \frac{v_{out}}{v_{in}} = \frac{0.5g_{m1}g_{m4}}{(g_{ds1}+g_{ds3})(g_{ds4}+g_{ds5})}$$



$$g_{m1} = \sqrt{\frac{2K_N W_1 I_{D1}}{L_1}} = \sqrt{24\cdot 2\cdot 4\cdot 10}\ \text{x}10^{-6} = 43.82\mu S$$

$$g_{ds1} = \lambda_N I_{D1} = 0.01\cdot 10\mu A = 0.1\mu S, \quad g_{ds3} = \lambda_P I_{D3} = 0.02\cdot 10\mu A = 0.2\mu S$$

$$g_{m4} = \sqrt{\frac{2K_P W_4 I_{D4}}{L_4}} = \sqrt{2\cdot 8\cdot 10\cdot 100}\ \text{x}10^{-6} = 126.5\mu S$$

$$g_{ds4} = \lambda_P I_{D4} = 0.02\cdot 100\mu A = 2\mu S, \quad g_{ds5} = \lambda_N I_{D5} = 0.01\cdot 100\mu A = 1\mu S$$

$$\therefore \quad \boxed{\frac{v_{out}}{v_{in}} = \frac{0.5\cdot 43.82\cdot 126.5}{(0.1+0.2)(1+2)} = 3{,}079 V/V}$$

Output resistance:

$$\boxed{R_{out} = \frac{1}{g_{ds4}+g_{ds5}} = \frac{10^6}{1+2} = 333k\Omega}$$

Dominant pole, p_1:

$$|p_1| = \frac{1}{R_1 C_1} \quad \text{where } R_1 = \frac{1}{g_{ds1}+g_{ds3}} = \frac{10^6}{0.1+0.2} = 3.33M\Omega$$

and

$$C_1 = C_c(1+|A_{v2}|) = 5pF\left(1 + \frac{g_{m4}}{g_{ds4}+g_{ds5}}\right) = 5\left(1+\frac{126.5}{3}\right) = 215.8pF$$

$$\therefore \ |p_1| = \frac{10^6}{3.33\cdot 2.15.8} = 1{,}391 \text{ rads/sec} \rightarrow \boxed{|p_1| = 1{,}391 \text{ rads/sec} = 221Hz}$$

$$GB = \frac{0.5\cdot g_{m1}}{C_c} = \frac{0.5\cdot 43.82\text{x}10^{-6}}{5\text{x}10^{-12}} = 4.382M\text{rads/sec}$$

$$\boxed{GB = 4.382 \text{ Mrads/sec} = 0.697MHz}$$

$$\boxed{SR = \frac{I_{D6}}{C_c} = \frac{10\mu A}{5pF} = 2V/\mu s} \qquad \boxed{P_{diss} = 10V(140\mu A) = 1.4mW}$$

Problem 4 - Design Problem 2 (50 points)