## Homework Assignment No. 6

Due Monday, February 21, 2005 in class

Problem 1 - (10 points)

For the CMOS op amp shown, find the following quantities. Use the MOS parameters of Table 3.1-2.

1.) Slew rate (V/sec.)

2.) Positive and negative output voltage limits (all transistors remain in saturation)

3.) Positive and negative input common voltage limits (all transistors remain in saturation and use nominal parameter values)

4.) Small signal voltage gain (V/V).

5.) Unity-gainbandwidth (MHz)

6.) Power dissipation (mW). (Include the 50µA current sink)
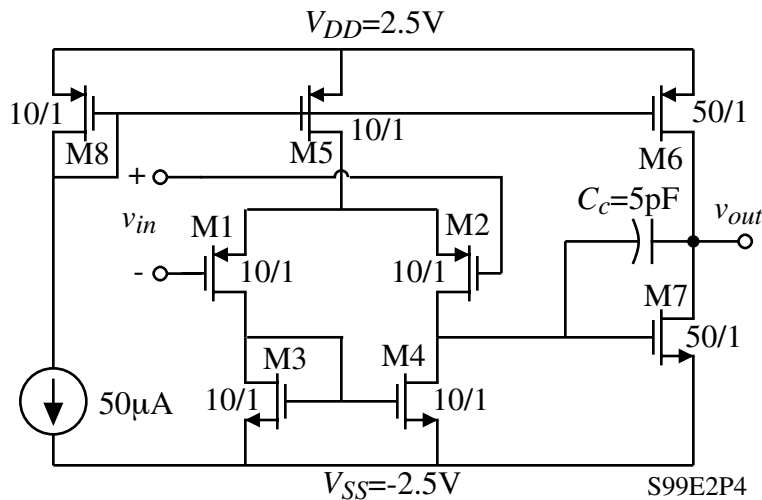
Table 3.1-2 Model Parameters for a Typical CMOS Bulk Process Suitable for Hand Calculations Using the Simple Model. These Values Are Based upon a 0.8 µm Silicon-Gate Bulk CMOS n-Well Process.

| Parameter Symbol	Parameter Description	Typical Parameter Value N-Channel	P-Channel	Units
V_{T0}	Threshold Voltage (V_{BS} = 0)	0.7 ± 0.15	-0.7 ± 0.15	V
K'	Transconductance Parameter (in saturation)	$110.0 \pm 10\%$	$50.0 \pm 10\%$	$\mu A/V^2$
γ	Bulk threshold parameter	0.4	0.57	$(V)^{1/2}$
λ	Channel length modulation parameter	0.04 (L=1 μm) 0.01 (L=2 μm)	0.05 (L = 1 μm) 0.01 (L = 2 μm)	$(V)^{-1}$
$2|\phi_F|$	Surface potential at strong inversion	0.7	0.8	V

Problem 2 - (10 points)

Problem 6.3-7 from the Second Edition of Allen and Holberg text.

Problem 3 - (10 points)

Problem 6.3-11 from the Second Edition of the Allen and Holberg text.

Problem 4 - Design Problem 2 (50 points)

The operational transconductance amplifier (OTA) shown is powered from ±2.5V power supplies. You are to perform a design of an OTA using only MOSFETs to best meet the following specifications:
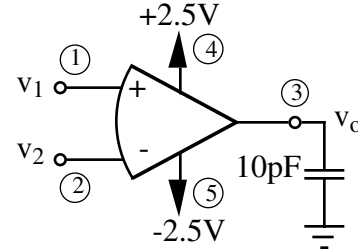
1.) The differential voltage gain: $A_{vd} \geq 80dB$.

2.) Output voltage swing range: OVSR = $|V_o(max)| + |V_o(min)| \geq 4.5V$.

The OVSR is determined by the maximum and minimum output voltages for which 50µA can be sourced or sunk into a load.

3.) Slew rate: SR $\geq$ 10V/µS into 10pF.

4.) Differential input resistance: $R_{id} \geq 1M\Omega$.

5.) Input common mode range: ICMR $\geq$ 3V. Please note that input ICMR is measured by sweeping the input common mode voltage and monitoring both the output voltage and input stage current (see Slide 8.56).

6.) The common mode rejection ratio: CMRR $\geq$ 60dB.

7.) Gain-bandwidth: GB $\geq$ 25MHz with a 10pF load capacitance.

8.) Phase margin: $\phi(GB) \geq 60°$ with a 10pF load capacitance.

9.) Power dissipation: $P_{diss} \leq 1mW$.

When you have completed your design and have made hand calculations to support your performance expectations, use the SPICE models on the following pages and verify your design using SPICE. Use the simplest models possible although you must include all capacitances. Use the following approximations to estimate the size of the D/S areas and perimeters.

$$AD = AS = (Wx10µm)$$

$$PS = PS = 2W + 20µm$$

Please fill out the following table to be included in your problem submission.

	A_{vd}	OVSR	SR	R_{id}	ICMR	CMRR	GB	$\phi(GB)$	P_{diss}
Hand Values									
SPICE Values									

The score on this design problem will be as follows:

$$Score = min\left[5,5\left(\frac{A_{vd}}{10^4}\right)\right] + min\left[5,5\left(\frac{OVSR}{4.5}\right)\right] + min\left[5,5\left(\frac{SR}{10V/\mu s}\right)\right] + min\left[5,5\left(\frac{R_{id}}{1M\Omega}\right)\right]$$

$$+ min\left[5,5\left(\frac{ICMR}{3V}\right)\right] + min\left[5,5\left(\frac{CMRR}{10^3}\right)\right] + min\left[5,5\left(\frac{GB}{25MHz}\right)\right] + min\left[5,5\left(\frac{\phi(GB)}{60°}\right)\right]$$

$$+ min\left[5,5\left(\frac{1mW}{P_{diss}}\right)\right] + 5(Simplicity\ factor)$$

You are responsible for verifying your score via the correct SPICE analysis. Please evaluate your own score providing sufficient detail for your instructor to verify your assessment of your grade. The simplicity factor is your instructors evaluation of your ability to keep the design straight-forward and simple and will be added to your score based on the specifications. This project is simply an exercise in learning design, do not spend more time on it than can be justified!

CMOS SPICE Model Parameters

Use the appropriate SPICE model parameters corresponding to a MOSIS T2BM (LO_EPI) SCN025 test run (see the web site below). You must determine the appropriate model parameters to use and be able to justify the use of those models. Please provide an output listing (.OP) for your CMOS models used in SPICE. You do not need to use BSIM3 model if you wish but you must properly include all capacitances into your model. If you have trouble finding the large signal model parameters from the MOSIS data, one method to get them is to use the BSIM model to plot the transconductance and output characteristics and then extract the model parameters for the simple large signal model from these curves. If you do this, you should check your model parameters by comparing appropriate simulations using both the simple large signal and the BSIM3 models.

http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/tsmc-025/t2bm_lo_epi-params.txt.