Homework Assignment No. 12

Due Friday April 15 in class

Problem 1 - (10 points)

Problem 7.2-1 of Allen and Holberg, 2nd edition.

Problem 2 - (10 points)

Problem 7.2-4 of Allen and Holberg, 2nd edition.

Problem 3 - (10 points)

Problem 7.3-7 of Allen and Holberg, 2nd edition.

Problem 4 - (10 points)

Problem 7.4-1 of Allen and Holberg, 2nd edition.

Problem 5 - (50 points) (You may turn in this problem on 4/20)

Pre-charge Buffer Design Problem

In this design problem you are required to design a so called pre-charge buffer which has rail to rail input and output capability. The main duty of the pre-charge buffer is to charge the sampling capacitor C_S at the input of an analog to digital converter (ADC) close to the input voltage in a short amount of time. After this pre-charging phase, the input is directly connected to the sampling capacitor and fine settling is achieved over a switch, Figure 1.

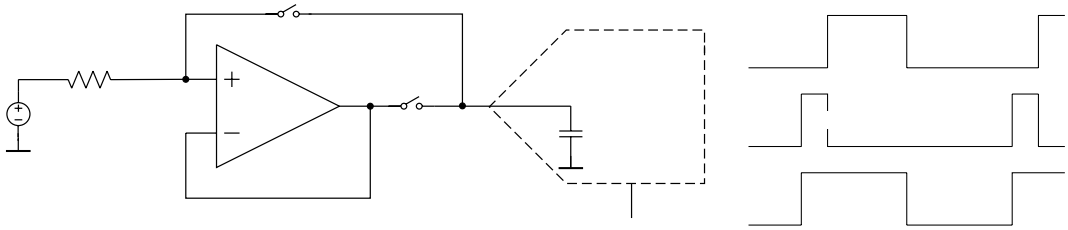

Fig. 1. Pre-charge Buffer and timing scheme.

By doing so, the charge/ current required from the input source is reduced. As a result input impedance of the ADC is effectively increased. The reduction in the current, increase in impedance is dependent on the settling performance of the pre-charge buffer, which is directly related to slew rate, gain-bandwidth product and DC gain.

In this design you are required to design an amplifier, A(s), which should have a settling accuracy of 2%, settling time of 100ns with a capacitive load of 10 pf and total power dissipation of 2 mW. Note that you may need excessive currents to have sufficient slew rate thus you may need to dynamically change the tail current or you may use input structures whose slew rate are not defined by the tail current. From the settling accuracy you can come up with the minimum DC gain you should have. Other design specs are tabulated in Table 1.

Table 1. Design Specs.

Quantity	Condition	Value
GBW	C_S=10pf	>10 MHz
Settling time	< 2% accuracy	<100 ns
Input CMR	.	Rail to rail
Output Swing	With capacitive load	Rail to rail
Supply	Single	5 V
Power Dissipation	Nominal	2 mW

For the settling accuracy and settling time, use the test bench given in Figure 2. Apply a step input and see the settling time and accuracy.

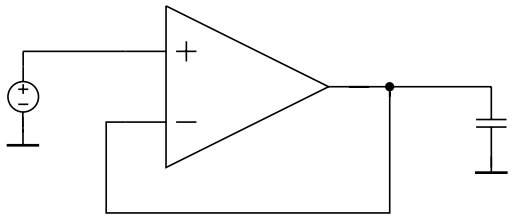

Fig. 2. Test bench for settling time and settling accuracy simulation.

You are required to use AMI 0.5 µm process. The Transistor models for this process can be downloaded from the MOSIS website:

http://www.mosis.org/Technical/Testdata/ami-c5-prm.html

Go to this website and download the spice models for any of the runs, preferably T51A. If you click on any one of the runs, you will see the spice models for NMOS and PMOS transistors for that run. At the end of the model page you will see a link "Download Text File". You can use this link to download the model files as a text file. You may need to do some syntax correction depending on the simulator you are using.

Further information about pre-charge buffers can be found at:

http://www.cirrus.com/en/pubs/appNote/an30.pdf

Grading will be as follows;

$$\text{Total grade} = 20\times\min\left[1,\left(\frac{2}{\text{Settling accuracy in \%}}\right)^2\right]+20\times\min\left[1,\left(\frac{2mW}{\text{Power dissipation}}\right)^2\right]+10\times\min\left[1,\left(\frac{\text{GBW}}{10MHz}\right)\right]$$

$$+20\times\min\left[1,\left(\frac{5V}{\text{ICMR}}\right)\right]+10\times\min\left[1,\left(\frac{5V}{\text{Output swing}}\right)\right]$$