LECTURE 030 – ECE 4430 REVIEW III

(READING: GHLM - Chaps. 3 and 4)

Objective

The objective of this presentation is:

1.) Identify the prerequisite material as taught in ECE 4430

2.) Insure that the students of ECE 6412 are adequately prepared

Outline

- Models for Integrated-Circuit Active Devices
- Bipolar, MOS, and BiCMOS IC Technology
- Single-Transistor and Multiple-Transistor Amplifiers
- Transistor Current Sources and Active Loads

SINGLE-TRANSISTOR AND MULTIPLE-TRANSISTOR AMPLIFIERS

Characterization of Amplifiers

Amplifiers will be characterized by the following properties:

- Large-signal voltage transfer characteristics (.DC)
- Large-signal voltage swing limitations (.DC and .TRAN)
- Small-signal, frequency independent performance (.TF)
- Gain (.TF)
- Input resistance (.TF)
- Output resistance (.TF)
- Small-signal, frequency response (.AC)
- Other properties (.TEMP, .FOUR, etc.)
- Noise (.NOISE)
- Power dissipation (.OP)
- Slew rate (.TRAN)
- Etc.

Types of Single Transistor Amplifiers

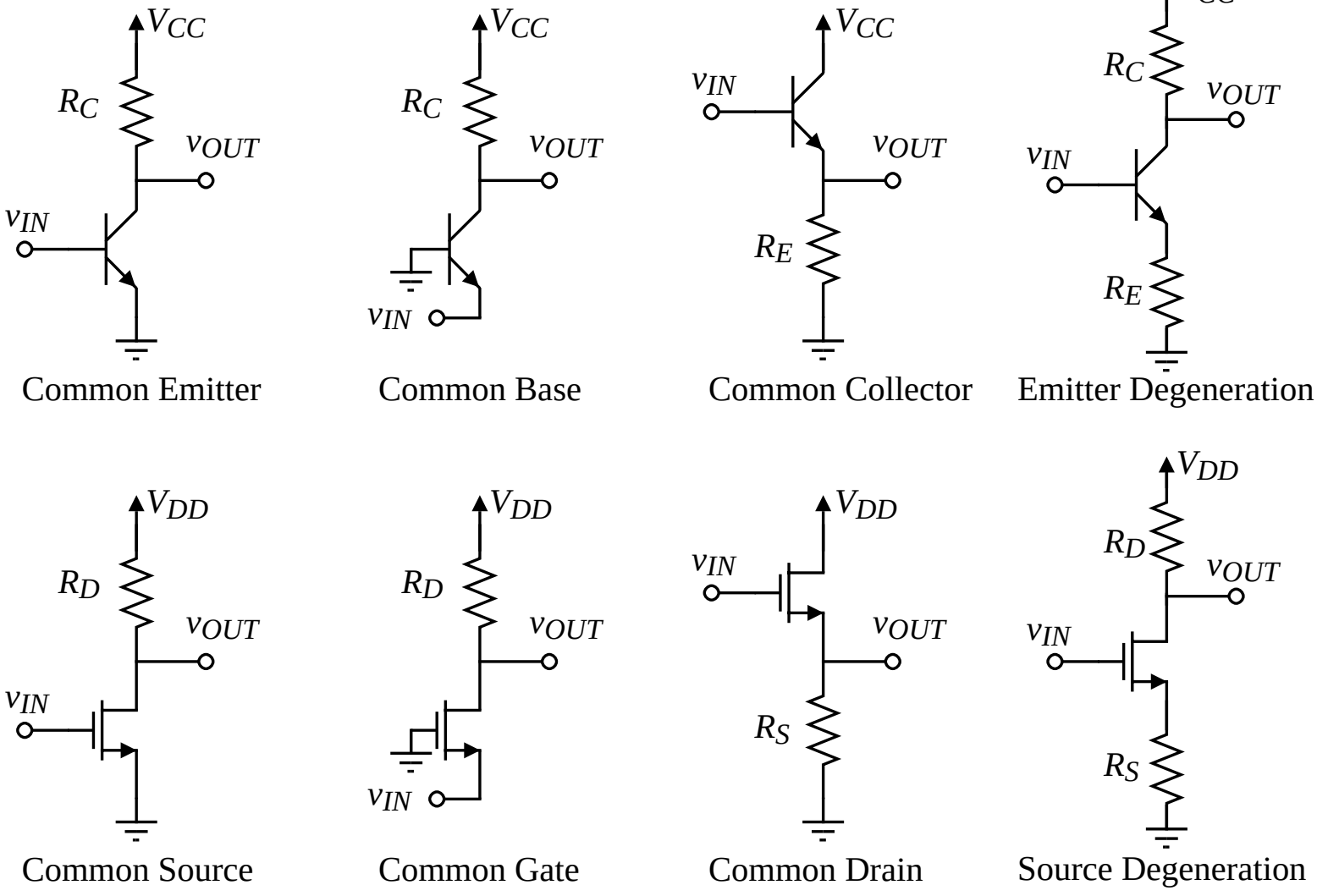

Fig. 030-01

Signal Flow in Transistors

It is important to recognize that ac signals can only flow into and out of certain transistor terminals.

Illustration:

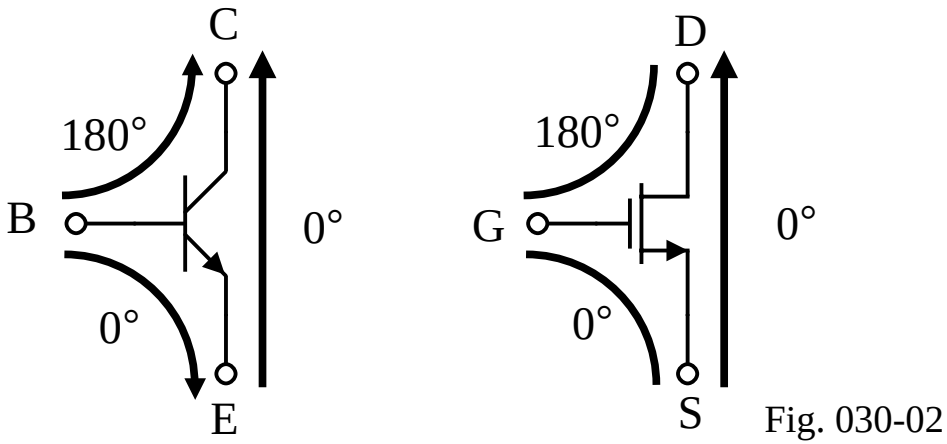

Fig. 030-02

Rules:

The collector or drain can never be an input terminal.

The base or gate can never be an output terminal.

In addition it is important to note polarity reversals on these signal paths.

The base-collector or gate-drain path inverts. All other paths are noninverting.

(This of course assumes that there are no reactive elements causing phase shifts)

Common Emitter Amplifer

Large-Signal:

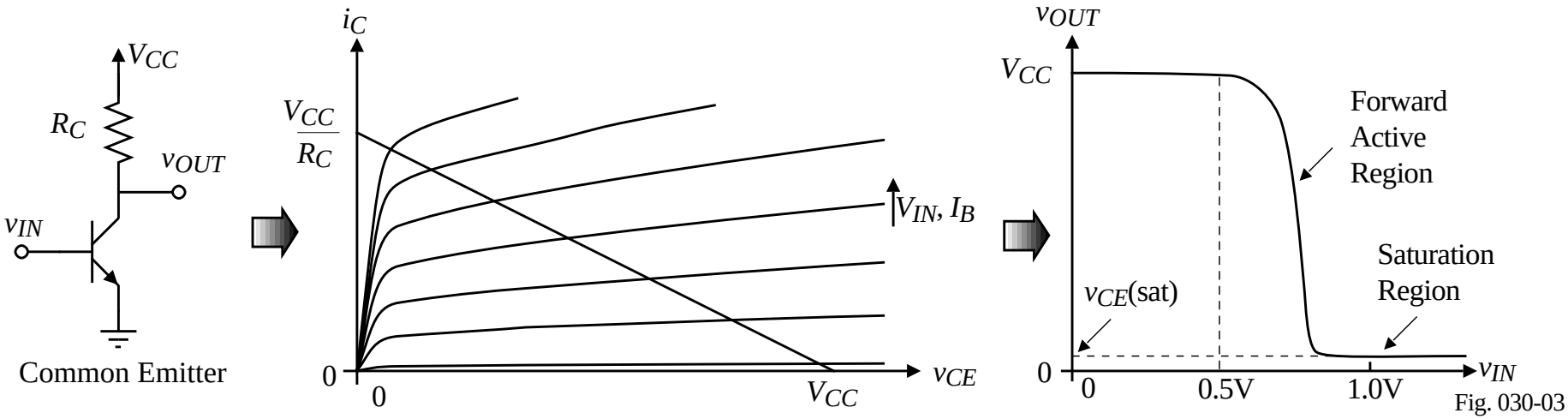

Fig. 030-03

Small-Signal:

$$g_m = \frac{I_C}{V_t} \qquad \text{and} \quad r_o = \frac{V_A}{I_C}$$

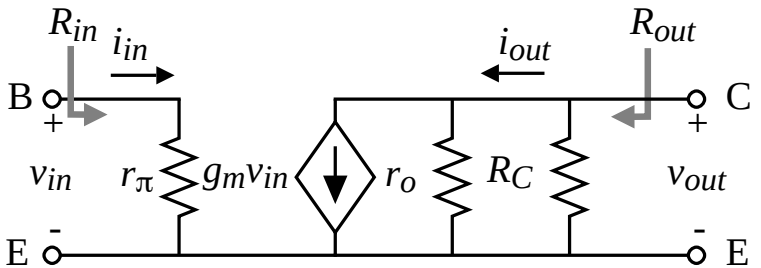

Fig. 030-04

$$R_{in} = r_\pi = \frac{\beta_o}{g_m}, \quad R_{out} = \frac{r_o R_C}{r_o + R_C}, \quad \frac{v_{out}}{v_{in}} = \frac{-g_m \cdot r_o \cdot R_C}{r_o + R_C} \quad \text{and} \quad \frac{i_{out}}{i_{in}} = \frac{\beta_o \cdot r_o}{r_o + R_C}$$

(One should also consider the case of a source resistance, R_S, in series with the input)

Common Source Amplifier

Large-Signal:

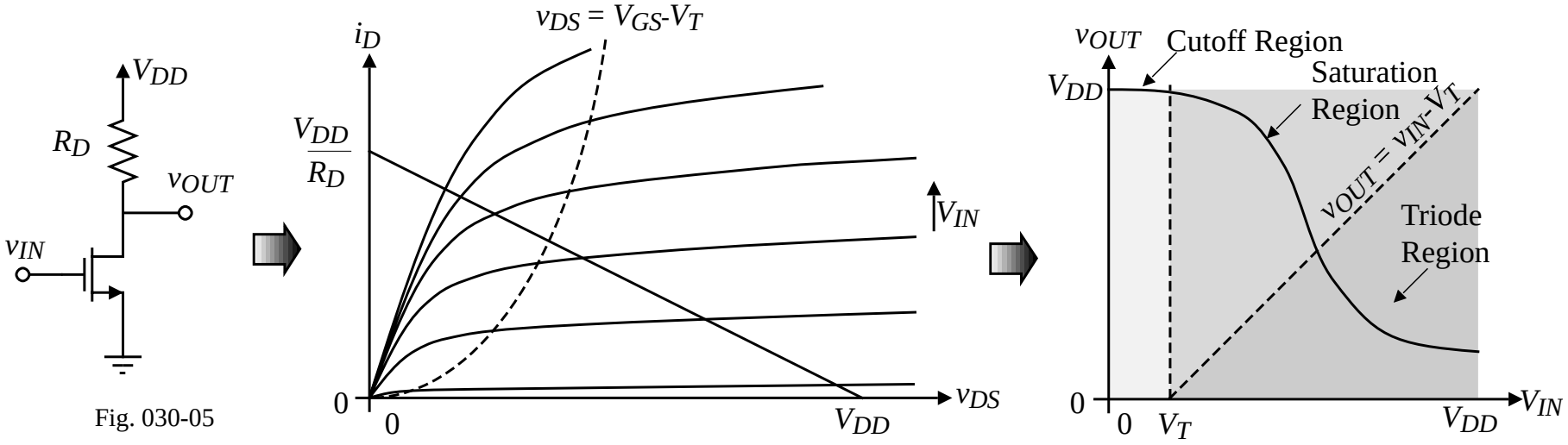

Fig. 030-05

Small-Signal:

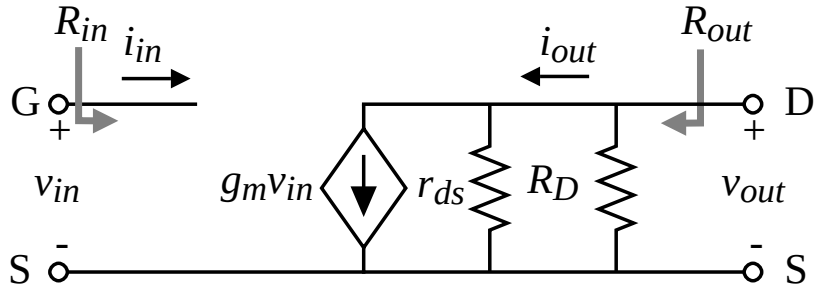

Fig. 030-055

$$R_{in} = \infty, \qquad R_{out} = \frac{r_{ds}R_D}{r_{ds} + R_D}, \qquad \frac{v_{out}}{v_{in}} = \frac{-g_m \cdot r_{ds} \cdot R_D}{r_{ds} + R_D} \qquad \text{and} \quad \frac{i_{out}}{i_{in}} = \infty$$

Summary of Single BJT Transistor Amplifiers

Small-Signal Performance	Common Emitter	Common Base	Common Collector
Input Resistance	r_π (Medium)	$\frac{r_\pi}{1+\beta_o}$ (Low)	$r_\pi+(1+\beta_o)R_E$ (High)
Output Resistance	r_o (High)	$r_o(1+\beta_o)$ (Very high)	$\frac{r_\pi+R_S}{1+\beta_o}$ (Very low)
Voltage Gain	$-g_mR_L$	g_mR_L	1
Current Gain	β_o	$-\alpha$	$-(1+\beta_o)$

Summary of Single MOSFET Transistor Amplifiers

Small-Signal Performance	Common Source	Common Gate	Common Drain
Input Resistance	∞	$\frac{r_{ds}+R_D}{1+g_m r_{ds}}$	∞
Output Resistance	$\frac{r_{ds}R_D}{r_{ds}+R_D}$	$\frac{r_{ds}R_D}{r_{ds}+R_D}$	$\frac{R_S}{1+g_m R_S}$
Voltage Gain	$\frac{-g_m \cdot r_{ds} \cdot R_D}{r_{ds}+R_D}$	$g_m R_D$	0.8
Current Gain	∞	-1	∞

BJT Cascode Amplifer

Circuit and small-signal model:

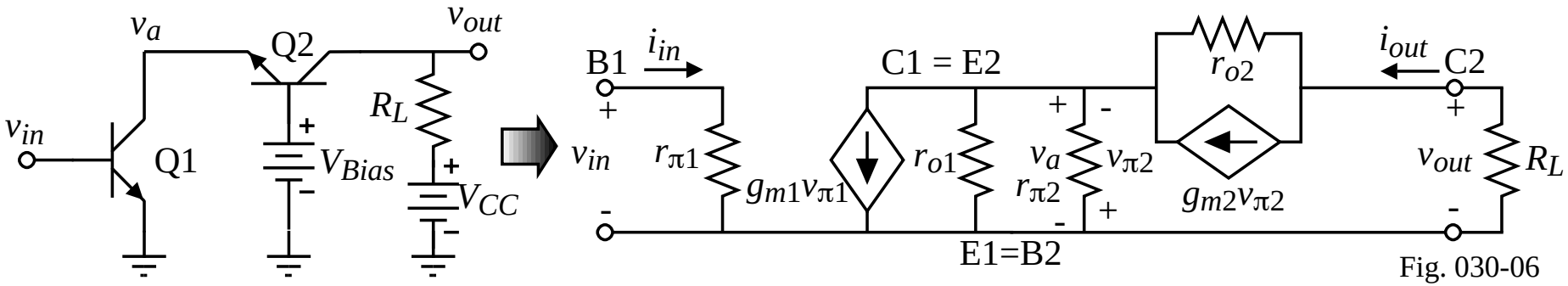

Fig. 030-06

If $\beta_1 \approx \beta_2$ and r_o can be neglected, then:

$$R_{in} = r_{\pi 1}$$

$$R_{out} \approx \beta_2 r_{o2} \quad \text{(not including } R_L\text{)}$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_{out}}{v_a}\right)\left(\frac{v_a}{v_{in}}\right) = (g_{m2}R_L)\left(\frac{r_{\pi 2}}{1+\beta_{o2}}\cdot\frac{-\beta_{o1}}{r_{\pi 1}}\right) \approx (g_{m2}R_L)\,(-1) = -\,g_{m2}R_L$$

$$\frac{i_{out}}{i_{in}} = \alpha_2\beta_1$$

The advantage of the cascode is that the gain of Q1 is -1 and therefore the Miller capacitor, C_μ, is not translated to the base-emitter as a large capacitor.

MOS Cascode Amplifier

Circuit and small-signal model:

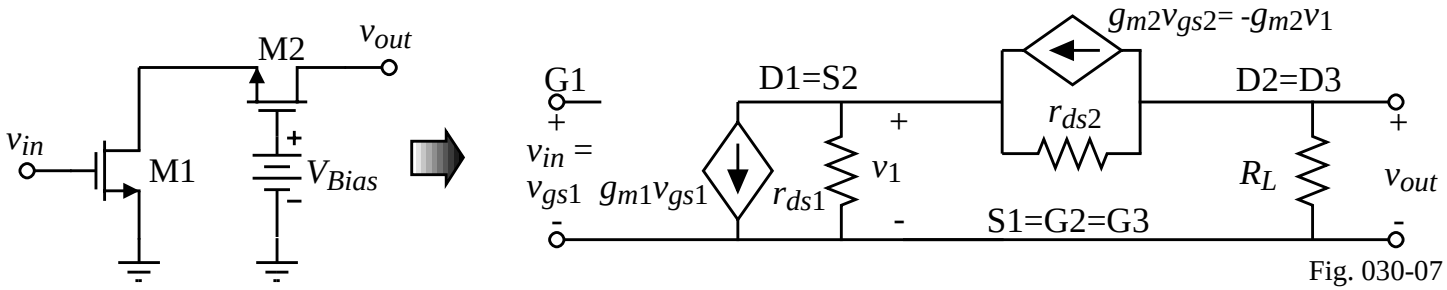

Fig. 030-07

Small-signal performance (assuming a load resistance in the drain of R_L):

$R_{in} = \infty$

Using nodal analysis, we can write,

$[g_{ds1} + g_{ds2} + g_{m2}]v_1 - g_{ds2}v_{out} = -g_{m1}v_{in}$ and $-[g_{ds2} + g_{m2}]v_1 + (g_{ds2} + G_L)v_{out} = 0$

Solving for v_{out}/v_{in} yields,

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}(g_{ds2} + g_{m2})}{g_{ds1}g_{ds2} + g_{ds1}G_L + g_{ds2}G_L + G_Lg_{m2}} \cong \frac{-g_{m1}}{G_L} = -g_{m1}R_L$$

Note that unlike the BJT cascode, the voltage gain, v_1/v_{in} is greater than -1.

$$\frac{v_1}{v_{in}} = -g_{m1}\left[r_{ds1}\left\|\left(\frac{r_{ds2}+R_L}{1+g_{m2}r_{ds2}}\right)\right.\right] \approx -\frac{r_{ds2}+R_L}{r_{ds2}} = -\left(1+\frac{R_L}{r_{ds2}}\right)$$ ($R_L < r_{ds2}$ for the gain to be -1)

The small-signal output resistance is,

$r_{out} = [r_{ds1} + r_{ds2} + g_{m2}r_{ds1}r_{ds2}]\,||\,R_L \cong R_L$, assuming that R_L is small.

Transconductance Characteristic of the BJT Differential Amplifier

Consider the following NPN-BJT differential amplifier (sometimes called an emitter-coupled pair):

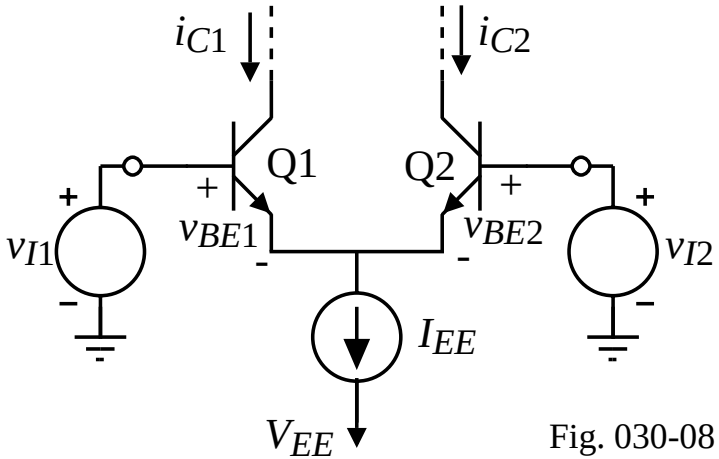

Fig. 030-08

Large-Signal Analysis:

1.) Input loop eq.:

$$v_{I1}\text{-}v_{BE1}\text{+}v_{BE2}\text{-}v_{I2} = v_{I1}\text{-}v_{I2}\text{-}v_{BE1}\text{+}v_{BE2}$$
$$= v_{ID}\text{-}v_{BE1}\text{+}v_{BE2} = 0$$

2.) Forward-active region:

$$v_{BE1} = V_t \ln\left(\frac{i_{C1}}{I_{S1}}\right) \quad \text{and} \quad v_{BE2} = V_t \ln\left(\frac{i_{C2}}{I_{S2}}\right)$$

3.) If $I_{S1} = I_{S2}$ then $\dfrac{i_{C1}}{i_{C2}} = \exp\left(\dfrac{v_{I1}\text{-}v_{I2}}{V_t}\right) = \exp\left(\dfrac{v_{ID}}{V_t}\right)$

4.) Nodal current equation at the emitters: $-(i_{E1}+i_{E2}) = I_{EE} = \dfrac{1}{\alpha_F}(i_{C1} + i_{C2})$

5.) Combining the above equations gives: $i_{C1} = \dfrac{\alpha_F I_{EE}}{1 + \exp\left(\dfrac{-v_{ID}}{V_t}\right)}$ and $i_{C2} = \dfrac{\alpha_F I_{EE}}{1 + \exp\left(\dfrac{v_{ID}}{V_t}\right)}$

Differential and Common-mode Small-Signal BJT Amplifier Performance

The small-signal performance of a differential amplifier can be separated into a differential mode and common mode analysis. This separation allows us to take advantage of the following simplifications.

Half-Circuit Concept:

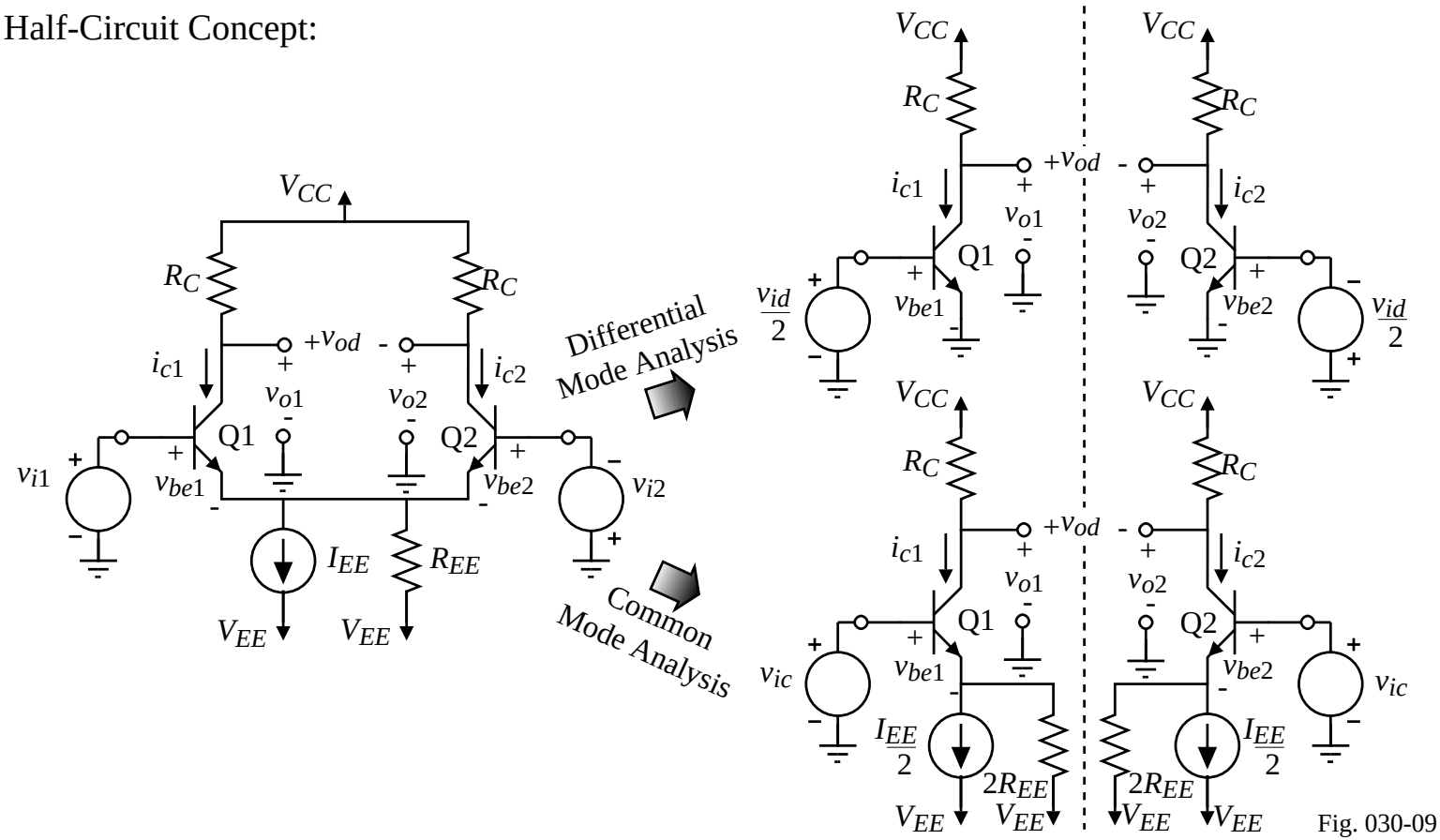

Fig. 030-09

Note: The half-circuit concept is valid as long as the resistance seen looking into each emitter is approximately the same.

Transconductance Performance of the Differential Amplifier

Consider the following n-channel differential amplifier:

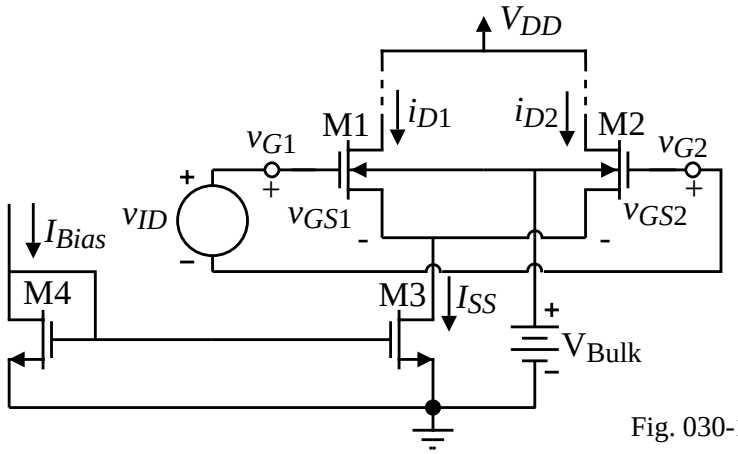

Fig. 030-10

Where should bulk be connected? Consider a p-well, CMOS technology,

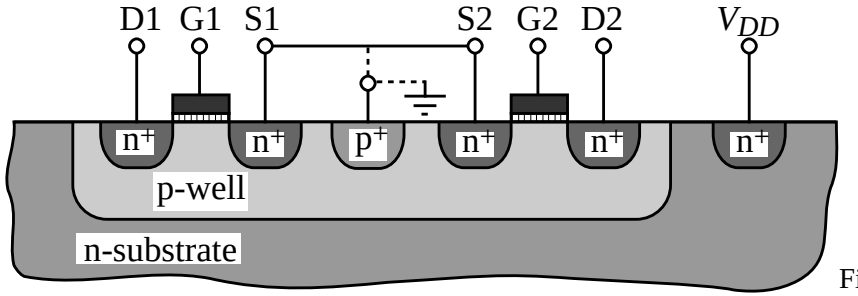

Fig. 030-11

1.) Bulks connected to the well: No modulation of V_T but large common mode parasitic capacitance.

2.) Bulks connected to ground: Smaller common mode parasitic capacitors, but modulation of V_T.

If the technology is n-well CMOS, the bulks must be connected to ground.

Transconductance Performance of the Differential Amplifier - Continued

Defining equations (Assume that the MOSFETs are in saturation):

$$v_{ID} = v_{GS1} - v_{GS2} = \left(\frac{2i_{D1}}{\beta}\right)^{1/2} - \left(\frac{2i_{D2}}{\beta}\right)^{1/2} \quad \text{and} \quad I_{SS} = i_{D1} + i_{D2}$$

Solution:

$$i_{D1} = \frac{I_{SS}}{2} + \frac{I_{SS}}{2}\left(\frac{\beta v_{ID}^2}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I_{SS}^2}\right)^{1/2} \quad \text{and} \quad i_{D2} = \frac{I_{SS}}{2} - \frac{I_{SS}}{2}\left(\frac{\beta v_{ID}^2}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I_{SS}^2}\right)^{1/2}$$

which are valid for $v_{ID} < (2I_{SS}/\beta)^{1/2}$.

Illustration of the result:

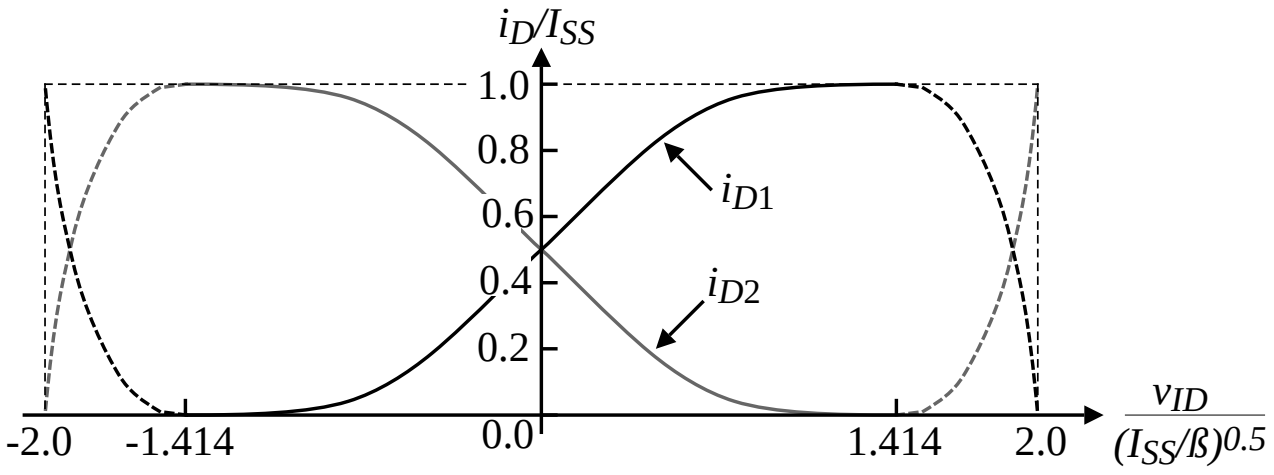

Fig. 030-12

Differential and Common-mode Small-Signal Performance

The small-signal performance of a differential amplifier can be separated into a differential mode and common mode analysis. This separation allows us to take advantage of the following simplifications.

Half-Circuit Concept:

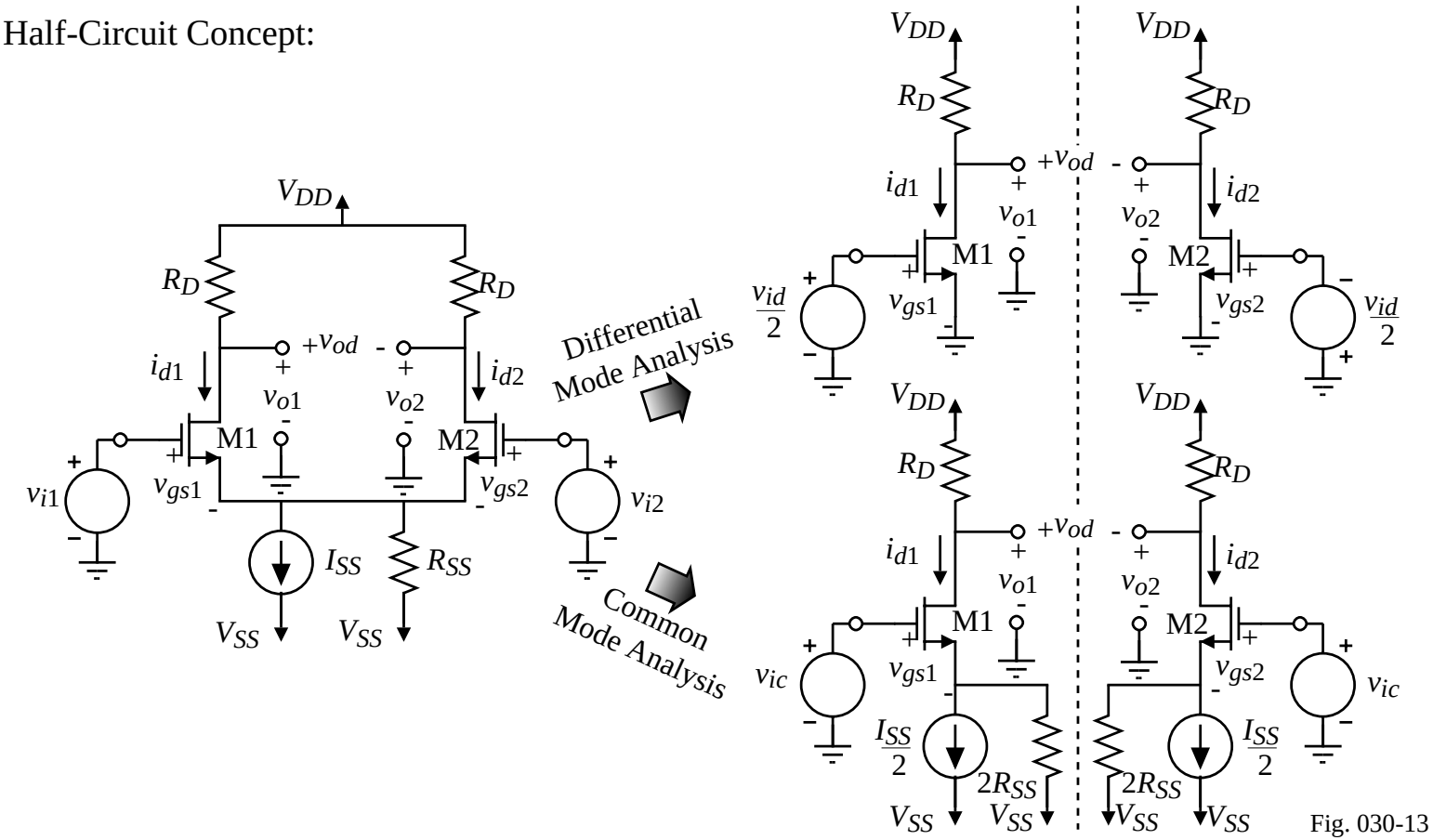

Fig. 030-13

Note: The half-circuit concept is valid as long as the resistance seen looking into each source is approximately the same.

Other Characteristics of the Differential Amplifier

- Common-mode rejection ratio
- Input common-mode range
- Slew rate

BJT:

ICMR: The maximum and minimum input common mode range is:

$$v_{ic}(\max) = V_{CC} - 0.5I_{EE}R_C - v_{CE1}(\text{sat}) + V_{BE1}$$

$$v_{ic}(\min) = V_{EE} + v_{CE3}(\text{sat}) + V_{BE1}$$

SR: The differential amplifier has a slew rate limit of I_{EE}/C_{eq} where C_{eq} is the capacitance seen to ground from either collector.

MOSFET:

ICMR: The maximum and minimum input common mode range is:

$$v_{ic}(\max) = V_{DD} - 0.5I_{SS}R_D + V_{T1}$$

$$v_{ic}(\min) = V_{SS} + v_{DS3}(\text{sat}) + V_{GS1}$$

SR: The differential amplifier has a slew rate limit of I_{SS}/C_{eq} where C_{eq} is the equivalent capacitance seen from either of the drains to ground.

TRANSISTOR CURRENT SOURCES AND ACTIVE LOADS

Summary of Current Sinks and Sources

Current Sink/Source	r_{OUT}	V_{MIN}
Simple MOS Current Sink	$r_{ds} = \frac{1}{\lambda I_D}$	$V_{DS}(\text{sat}) = V_{ON}$
Simple BJT Current Sink	$r_o = \frac{V_A}{I_C}$	$V_{CE}(\text{sat}) \approx 0.2\text{V}$
Cascode MOS	$\approx g_{m2} r_{ds2} r_{ds1}$	$V_T + 2V_{ON}$
Cascode BJT	$\approx \beta_F r_o$	$2V_{CE}(\text{sat})$
Minimum V_{MIN} Cascode Current Sink	$\approx g_{m2} r_{ds2} r_{ds1}$	$2V_{ON}$
Regulated Cascode Current Sink	$\approx r_{ds3} g_{m3} r_{ds2} g_{m4} (r_{ds4} \| r_{ds5})$	$\approx V_T + V_{ON}$
Minimum V_{MIN} Regulated Cascode Current Sink	$\approx r_{ds3} g_{m3} r_{ds2} g_{m4} (r_{ds4} \| r_{ds5})$	$\approx V_{ON}$

Summary of MOS Current Mirrors

Current Mirror	Accuracy	Output Resistance	Input Resistance	Minimum Output Voltage	Minimum Input Voltage
Simple	Poor	r_{ds}	$\frac{1}{g_m}$	V_{ON}	V_T+V_{ON}
Cascode	Excellent	$g_m r_{ds}^2$	$\frac{2}{g_m}$	V_T+2V_{ON}	$2(V_T+V_{ON})$
Wide Output Swing Cascode	Excellent	$g_m r_{ds}^2$	$\frac{1}{g_m}$	$2V_{ON}$	V_T+V_{ON}
Self-biased Cascode	Excellent	$g_m r_{ds}^2$	$R+\frac{1}{g_m}$	$2V_{ON}$	V_T+2V_{ON}
Wilson	Poor	$g_m r_{ds}^2$	$\frac{2}{g_m}$	$2(V_T+V_{ON})$	V_T+2V_{ON}
Regulated Cascode	Good-Excellent	$g_m^2 r_{ds}^3$	$\frac{1}{g_m}$	V_T+2V_{ON} (min. is $2V_{ON}$)	V_T+V_{ON} (min. is V_{ON})

Summary of BJT Current Mirrors

Current Mirror	Accuracy	Output Resistance	Input Resistance	Minimum Output Voltage	Minimum Input Voltage
Simple	Poor	r_o	$\frac{1}{g_m}$	V_{CE}(sat)	V_{BE}
Cascode	Excellent	$\beta_F r_o$	$\frac{2}{g_m}$	V_{CE}(sat)+V_{BE}	$2V_{BE}$
Wide Output Swing Cascode	Excellent	$\beta_F r_o$	$\frac{1}{g_m}$	$2V_{CE}$(sat)	V_{BE}
Self-biased Cascode	Excellent	$\beta_F r_o$	$R+\frac{1}{g_m}$	$2V_{CE}$(sat)	V_{CE}(sat)+V_{BE}
Wilson	Poor	$\beta_F r_o$	$\frac{2}{g_m}$	V_{CE}(sat)+V_{BE}	V_{CE}(sat)+V_{BE}
Regulated Cascode	Good-Excellent	$\beta_F r_o$	$\frac{1}{g_m}$ or less	V_{CE}(sat)*	V_{CE}(sat)*

* One can design the regulated cascode so that effectively the minimum value of V_{MIN} (out) is just V_{CE}(sat).

Active Load Amplifiers

What is an active load amplifier?

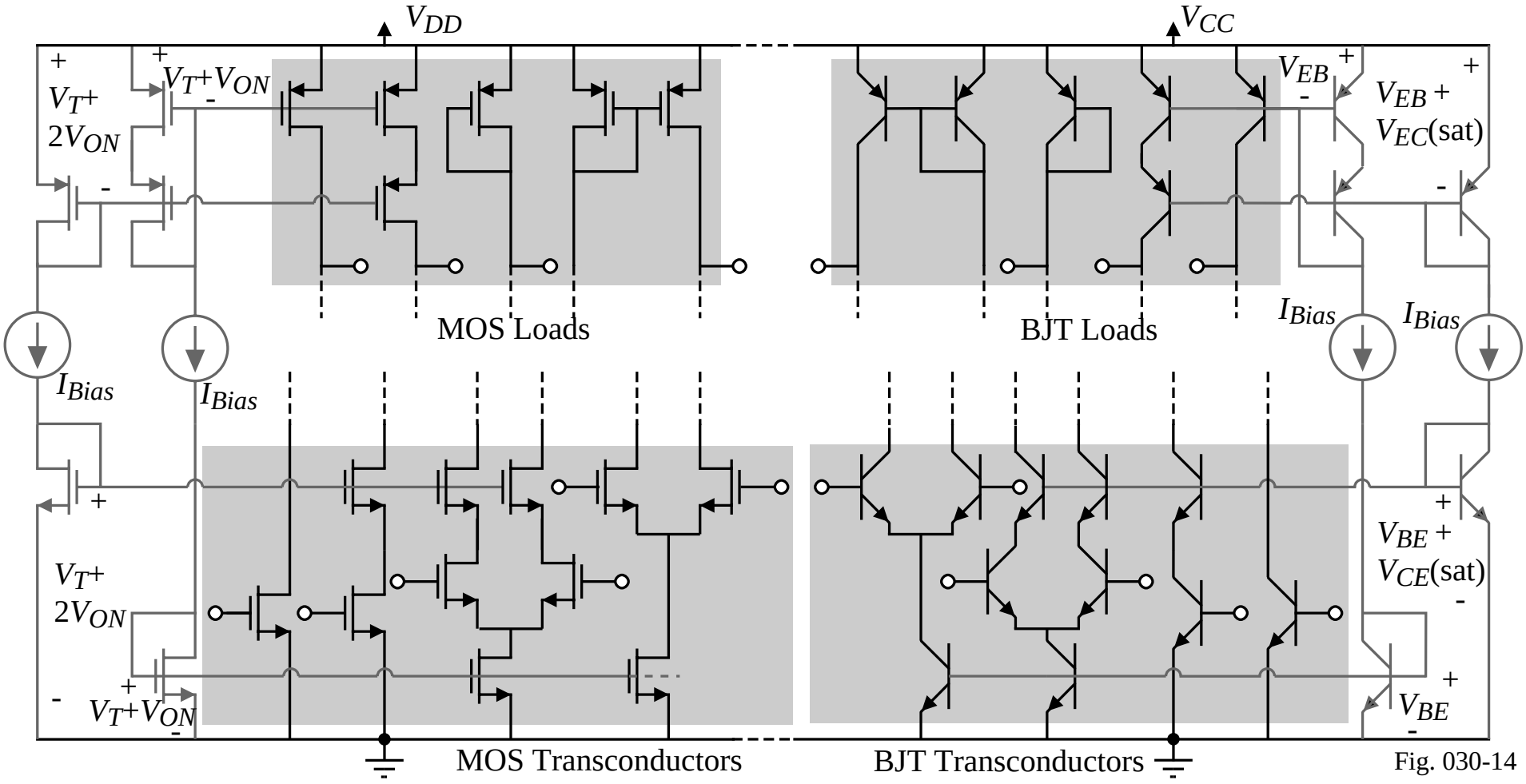

Fig. 030-14

It is a combination of any of the above transconductors and loads to form an amplifier. (Remember that the above are only *some* of the examples of transconductors and loads.)

BJT Differential Amplifier with a Current Mirror Load

Design Considerations:

Constraints	Specifications
Power supply	Small-signal gain
Technology	Frequency response (C_L)
Temperature	ICMR
	Slew rate (C_L)
	Power dissipation

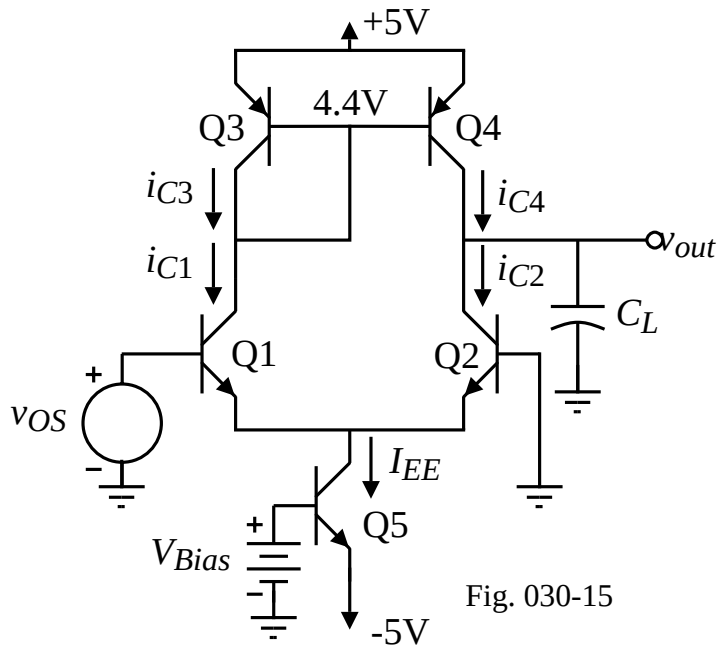

Fig. 030-15

Relationships

$A_v = g_{m1}R_{out}$

$\omega_{\text{-3dB}} = 1/R_{out}C_L$

$v_{IC}(\text{max}) = V_{CC} - |V_{BE3}| - V_{CE1}(\text{sat}) + V_{BE1} \approx V_{CC} - V_{CE1}(\text{sat})$

$v_{IC}(\text{min}) = V_{EE} + V_{CE5}(\text{sat}) + V_{BE1}$

$SR = I_{EE}/C_L$

$P_{diss} = (V_{CC}+|V_{EE}|)\cdot$All dc currents flowing from V_{CC} or to V_{EE}

CMOS Differential Amplifier with a Current Mirror Load

Design Considerations:

Constraints	Specifications
Power supply	Small-signal gain
Technology	Frequency response (C_L)
Temperature	ICMR
	Slew rate (C_L)
	Power dissipation

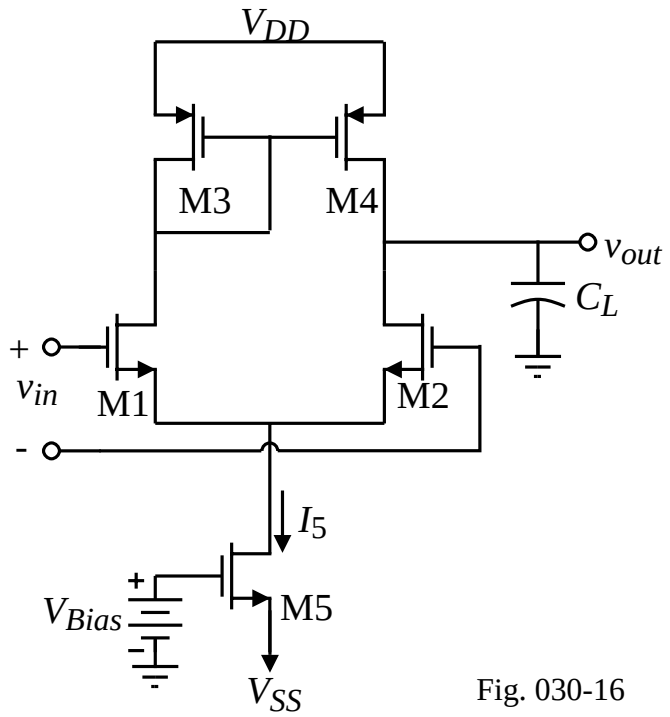

Fig. 030-16

Relationships

$A_v = g_{m1}R_{out}$

$\omega_{-3dB} = 1/R_{out}C_L$

$V_{IC}(\text{max}) = V_{DD} - V_{SG3} + V_{TN1}$

$V_{IC}(\text{min}) = V_{DS5}(\text{sat}) + V_{GS1} = V_{DS5}(\text{sat}) + V_{GS2}$

$SR = I_{SS}/C_L$

$P_{diss} = (V_{DD}+|V_{SS}|)\cdot$All dc currents flowing from V_{DD} or to V_{SS}

Summary of Active Load Amplifiers

- Active load amplifier consists of a transconductor and a load

  There are a large number of combinations of loads and transconductors possible. We have not considered the many cascoded possibilities and other configurations.
- The BJT amplifier generally has more gain and wider signal swing than the MOS amplifier
- The voltage gain of the MOS transconductor with a current source or current mirror load is inversely proportional to the square root of the bias current.
- The current mirror load differential amplifier is a widely used input stage
- The frequency response is generally determined by the dominant pole which is found at points in the circuit that are high impedance to ac ground and large capacitance
- The active load amplifier is the primary gain stage in operational amplifiers and other applications and will be a fundamental building block in more complex circuits
- Performance not considered include slew rate and noise

SUMMARY

- Single and Multiple Transistor Amplifiers
  - Characterization
  - BJT: Common emitter, common-base, common-collector, general
  - MOSFET: Common source, common-gate, common-drain, general
- Cascode Amplifiers
- Differential Amplifiers
  - Differential mode analysis (balance requirements) $\Rightarrow$ Half-circuit concept
  - Common mode analysis $\Rightarrow$ Half-circuit concept
  - Input common mode range and slew rate
- Transistor Current Sources and Current Mirrors
- Active Load Amplifiers
- Other Material not Included in this Review
  - Voltage and Current References
  - Bandgap Voltage Reference
  - Simple two-stage op amps