REVIEW FOR EXAMINATION NO.1

Examination No. 1 will be given during class on Wednesday, June 18, 2003 from 10:40am to 11:50am. It will last for 70 minutes and is open lecture notes. If relationships you need are not available, ask your proctor or make reasonable assumptions and continue with the problem. The exam will consist of approximately 4 problems. Below is a list of the material for which you are responsible.

Introduction to Frequency Synthesizers

Characterization of frequency synthesizers
Types of frequency synthesizers
- Incoherent synthesis
- Coherent direct synthesis
- Cohernet direct digital synthesis
- Coherent indirect synthesis

Frequency translation
Filters

Discrete and Integrated Circuit Technology

Discrete components
- Passive components – definition and characteristics, types, range of values, variable components

Integrated components
- Characteristics of a modern technology
- Passive elements compatible with IC technology – characteristics, range of values

LPLL and DPLLs

Phase detectors - Multipliers, EXOR, JK, PFD
Filters – Passive, active, charge pump
Locked relationships
Open loop – phase margin, crossover frequency
Closed loop – transfer functions in the frequency domain for various stimulations (phase step, frequency step, frequency ramp)
Steady-state phase error
Unlocked state – acquisition process
- Hold, Pull-In, Pull-Out, and Lock ranges and times

Noise relationships
LPLL and DPLL design

ADPLLs

General concepts only

PLL Design Equations and Relationships

Type and order of the loop
Be able to develop the design equations given a different configuration
Know the design equations for Type I, first- and second-order loops and for Type II, second-order loop