Homework No. 8

Due: Monday, July 14, 2003

Problem 1 – (50 points)

Use the National Semiconductor website (www.national.com) to design a DPLL frequency synthesizer for the GSM (935-960MHz) application. The channel spacing is 200kHz. Choose an appropriate VCO from a manufacturer. Assume a 0.25µm CMOS process with a 3.3V power supply. If you are not familiar with the GSM standard the key information is:

- Frequency band: 935 MHz ~ 960 MHz
- Channel spacing: 200 kHz
- Power supply: 3.3 V
- Technology: 0.25 µm CMOS
- Switching time: < 800 µs (by GSM standard)

Your homework should show a block diagram for the resulting frequency synthesizer with the blocks identified. Give the following parameters that you selected for your design:

1.) $N$, the divider ratio.
2.) $\zeta$, the damping ratio
3.) The type of PD/PFD and the value of $K_d$.
4.) The type of VCO, $K_v$, and $V_{min}$ and $V_{max}$.
5.) $\tau_L$, the lock-in time or settling time and $\omega_n$, the natural frequency of the PLL
6.) Design of the loop filter including the time constants and component values.

Illustrate the performance of your frequency synthesizer with any appropriate simulation results that may be available from the website.

There is a design procedure for digital PLLs in Sec. 3.4 of “Phase-Locked Loops – Design, Simulation, and Applications” 4th ed. by Roland Best, McGraw-Hill, 1999 that may be of use to you.

Problem 2 – (10 points)

The phase noise of an oscillator is –40 dBc at 10 Hz offset and has a straight-line variation (on a dBc vs. log$f$ scale) variation to –85 dBc at 15 kHz offset. Determine the residual phase modulation in the range of 300 Hz to 3 kHz.

Problem 3 – (10 points)

On page 160-33 of the class lecture notes, the approximate $rms$ value of the impulse sensitivity function for single-ended ring oscillators is given as

$$\Gamma_{rms} \approx \sqrt{\frac{2\pi^2}{3\eta^3}} \frac{1}{N^{1.5}}$$

Derive this approximate impulse sensitivity function.