Objective
The objective of this presentation is:
1.) Illustrate and model the passive components compatible with IC technology
2.) The passive components examined will be those suitable for frequency synthesizers

Outline
• Resistors
• Capacitors
• Inductors
• Summary

RESISTORS

MOS Resistors - Source/Drain Resistor

Diffusion:
10-100 ohms/square
Absolute accuracy = ±35%
Relative accuracy = 2% (5µm), 0.2% (50µm)
Temperature coefficient = +1500 ppm/°C
Voltage coefficient ≈ 200 ppm/V

Ion Implanted:
500-2000 ohms/square
Absolute accuracy = ±15%
Relative accuracy = 2% (5µm), 0.15% (50µm)
Temperature coefficient = +400 ppm/°C
Voltage coefficient ≈ 800 ppm/V

Comments:
• Parasitic capacitance to substrate is voltage dependent.
• Piezoresistance effects occur due to chip strain from mounting.
**Polysilicon Resistor**

![Polysilicon Resistor Diagram](image)

- 30-100 ohms/square (unshielded)
- 100-500 ohms/square (shielded)
- Absolute accuracy $\pm 30\%$
- Relative accuracy $2\%$ (5 µm)
- Temperature coefficient $500$-$1000$ ppm/°C
- Voltage coefficient $\approx 100$ ppm/V

**Comments:**
- Used for fuzes and laser trimming
- Good general resistor with low parasitics

**N-well Resistor**

![N-well Resistor Diagram](image)

- 1000-5000 ohms/square
- Absolute accuracy $\pm 40\%$
- Relative accuracy $5\%$
- Temperature coefficient $4000$ ppm/°C
- Voltage coefficient is large $\approx 8000$ ppm/V

**Comments:**
- Good when large values of resistance are needed.
- Parasitics are large and resistance is voltage dependent
CAPACITORS

Types of Capacitors Considered
- pn junction capacitors
- Standard MOS capacitors
- Accumulation mode MOS capacitors
- Poly-poly capacitors
- Metal-metal capacitors

Characterization of Capacitors
Assume $C$ is the desired capacitance:
1.) Dissipation (quality factor) of a capacitor is
   \[ Q = \omega CR_p \]
   where $R_p$ is the equivalent resistance in parallel with the capacitor, $C$.
2.) $C_{\text{max}}/C_{\text{min}}$ ratio is the ratio of the largest value of capacitance to the smallest when the capacitor is used as a variable capacitor called varactor.
3.) Variation of capacitance with the control voltage.
4.) Parasitic capacitors from both terminal of the desired capacitor to ac ground.

Desirable Characteristics of Varactors
1.) A high quality factor
2.) A control voltage range compatible with supply voltage
3.) Good tunability over the available control voltage range
4.) Small silicon area (reduces cost)
5.) Reasonably uniform capacitance variation over the available control voltage range
6.) A high $C_{\text{max}}/C_{\text{min}}$ ratio

Some References for Further Information
**PN Junction Capacitors**

Generally made by diffusion into the well.

![Diagram of PN Junction Capacitors](image_url)

**Layout:**

Minimize the distance between the $p^+$ and $n^+$ diffusions.

Two different versions have been tested.

1.) Large islands – 9µm on a side
2.) Small islands – 1.2µm on a side

Experimental data ($Q$ at 2GHz, 0.5µm CMOS):

<table>
<thead>
<tr>
<th>Terminal Under Test</th>
<th>Small Islands (598 1.2µm x 1.2µm)</th>
<th>Large Islands (42 9µm x 9µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$C_{max}/C_{min}$</td>
<td>$Q_{min}$</td>
</tr>
<tr>
<td>Anode</td>
<td>1.23</td>
<td>94.5</td>
</tr>
<tr>
<td>Cathode</td>
<td>1.21</td>
<td>8.4</td>
</tr>
</tbody>
</table>

Electrons as majority carriers lead to higher $Q$ because of their higher mobility.
The resistance, $R_{wj}$, is reduced in small islands compared with large islands $\Rightarrow$ higher Q.
Single-Ended and Differential PN Junction Capacitors
Differential configurations can reduce the bulk resistances and increase the effective $Q$.

An examination of the electric field lines shows that because the symmetry inherent in the differential configuration, the path to the small-signal ground can be shortened if devices with opposite polarity alternate.

Standard MOS Capacitor ($D = S = B$)
Conditions:
- $D = S = B$
- Operates from accumulation to inversion
- Nonmonotonic
- Nonlinear
**Inversion Mode MOS Capacitors**

Conditions:
- \( D = S, B = V_{DD} \)
- Accumulation region removed by connecting bulk to \( V_{DD} \)
- Channel resistance:
  \[
  R_{on} = \frac{L}{12K_P(V_{BG}-|V_T|)}
  \]
- LDD transistors will give lower \( Q \) because of the increased series resistance

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**Experimental Results for Standard and Inversion Mode 0.25µm CMOS Varactors**

\( n \)-well:
**Inversion Mode MOS Capacitors – Continued**

Bulk tuning of the polysilicon-oxide-channel capacitor (0.35µm CMOS)

![Capacitance Graph]

$C_{max}/C_{min} = 4$

**Interpretation:**

![Diagrams](Fig. 2.5-3)

$C_{max}/C_{min} = 4$

**Interpretation:**

![Capacitance Graph](Fig. 2.5-34)

**Inversion Mode NMOS Varactor – Continued**

More Detail - Includes the LDD transistor

![Varactor Diagram](Fig. 2.5-2)

Best results are obtained when the drain-source are on ac ground.

**Experimental Results ($Q$ at 2GHz, 0.5µm CMOS):**

$$V_G = 1.8V: \quad C_{max}/C_{min} \text{ ratio} = 2.15 (1.91), \quad Q_{max} = 34.3 (5.4), \quad \text{and} \quad Q_{min} = 25.8(4.9)$$
Accumulation Mode MOS Capacitors

Conditions:
- Remove p+ drain and source and put n+ bulk contacts instead
- Generally not supported (yet) in most silicon foundries

![Accumulation Mode MOS Capacitors](image)

Accumulation-Mode Capacitor – More Detail

Best results are obtained when the drain-source are on ac ground.

Experimental Results ($Q$ at 2GHz, 0.5µm CMOS):

$$V_G = 0.6V: \frac{C_{max}}{C_{min}} \text{ ratio} = 1.69 \ (1.61), \ Q_{max} = 38.3 \ (15.0), \text{ and } Q_{min} = 33.2 \ (13.6)$$
Differential Varactors†

![Diode Varactor](image1.png) ![Inversion-PMOS Varactor](image2.png) ![Accumulation-PMOS Varactor](image3.png)

Fig. 040-01


<table>
<thead>
<tr>
<th>Varactor</th>
<th>(f_L-f_H) (GHz)</th>
<th>(f_C) (GHz)</th>
<th>Tuning Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode</td>
<td>1.73-1.93</td>
<td>1.83</td>
<td>10.9%</td>
</tr>
<tr>
<td>I-MOS</td>
<td>1.71-1.91</td>
<td>1.81</td>
<td>11.0%</td>
</tr>
<tr>
<td>A-MOS</td>
<td>1.70-1.89</td>
<td>1.80</td>
<td>10.6%</td>
</tr>
</tbody>
</table>

Compensated MOS-Capacitors in Depletion with Substrate Biasing†

Substrate biasing keeps the MOS capacitors in a broad depletion region and extends the usable voltage range and achieves a first-order cancellation of the nonlinearity effect.

Principle:

![Compensated MOS-Capacitors](image4.png)


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### Compensated MOS-Capacitors in Depletion – Continued

Measured CV plot of a series compensated MOS capacitor with different substrate biases (0.25µm CMOS, $t_{ox} = 5$nm, $W_1=W_2=20$µm and $L_1=L_2=20$µm):

![CV plot](image1)

Example of a realization of the series compensation without using floating batteries.

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### MOS Capacitors - Continued

Polysilicon-Oxide-Polysilicon (Poly-Poly):

Best possible capacitor for analog circuits
Less parasitics
Voltage independent
Possible approach for increasing the voltage linearity:
Implementation of Capacitors using Available Interconnect Layers


Horizontal Metal Capacitors
Capacitance between conductors on the same level and use lateral flux.

These capacitors are sometimes called fractal capacitors because the fractal patterns are structures that enclose a finite area with an infinite perimeter.

The capacitor/area can be increased by a factor of 10 over vertical flux capacitors.
## MOS Passive RC Component Performance Summary

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Range of Values</th>
<th>Absolute Accuracy</th>
<th>Relative Accuracy</th>
<th>Temperature Coefficient</th>
<th>Voltage Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly-oxide-semiconductor Capacitor</td>
<td>0.35-0.5 fF/µm²</td>
<td>10%</td>
<td>0.1%</td>
<td>20ppm/°C</td>
<td>±20ppm/V</td>
</tr>
<tr>
<td>Poly-Poly Capacitor</td>
<td>0.3-0.4 fF/µm²</td>
<td>20%</td>
<td>0.1%</td>
<td>25ppm/°C</td>
<td>±50ppm/V</td>
</tr>
<tr>
<td>Diffused Resistor</td>
<td>10-100 Ω/sq.</td>
<td>35%</td>
<td>2%</td>
<td>1500ppm/°C</td>
<td>200ppm/V</td>
</tr>
<tr>
<td>Ion Implanted Resistor</td>
<td>0.5-2 kΩ/sq.</td>
<td>15%</td>
<td>2%</td>
<td>400ppm/°C</td>
<td>800ppm/V</td>
</tr>
<tr>
<td>Poly Resistor</td>
<td>30-200 Ω/sq.</td>
<td>30%</td>
<td>2%</td>
<td>1500ppm/°C</td>
<td>100ppm/V</td>
</tr>
<tr>
<td>n-well Resistor</td>
<td>1-10 kΩ/sq.</td>
<td>40%</td>
<td>5%</td>
<td>8000ppm/°C</td>
<td>10kppm/V</td>
</tr>
</tbody>
</table>

### Inductors

**Inductors**

What is the range of values for on-chip inductors?

Consider an inductor used to resonate with 5pF at 1000MHz.

\[
L = \frac{1}{4\pi^2 f_o^2 C} = \frac{1}{(2\pi \cdot 10^9)^2 \cdot 2.5 \times 10^{-12}} = 5\text{nH}
\]

Note: Off-chip connections will result in inductance as well.
**Candidates for inductors in CMOS technology are:**

1.) Bond wires  
2.) Spiral inductors  
3.) Multi-level spiral  
4.) Solenoid  

**Bond wire Inductors:**

- Function of the pad distance $d$ and the bond angle $\beta$  
- Typical value is $1\text{nH/mm}$ which gives $2\text{nH}$ to $5\text{nH}$ in typical packages  
- Series loss is $0.2 \ \Omega/\text{mm}$ for $1 \text{ mil diameter aluminum wire}$  
- $Q \approx 60$ at $2 \text{ GHz}$

**Planar Spiral Inductors**

Spiral Inductors on a Lossy Substrate:

- Design Parameters:
  - Inductance, $L = \Sigma(L_{self} + L_{mutual})$  
  - Quality factor, $Q = \frac{\omega L}{R}$  
  - Self-resonant frequency: $f_{self} = \frac{1}{\sqrt{LC}}$  
- Trade-off exists between the $Q$ and self-resonant frequency  
- Typical values are $L = 1-8\text{nH}$ and $Q = 3-6$ at $2\text{GHz}$
Planar Spiral Inductors - Continued

Inductor Design

![Diagram of a spiral inductor with labels: N_{\text{turns}} = 2.5, W, S, I, L, R, C_1, C_2, R_1, R_2, C_{\text{Load}}.]

Typically: $3 < N_{\text{turns}} < 5$ and $S = S_{\text{min}}$ for the given current

Select the OD, $N_{\text{turns}}$, and W so that ID allows sufficient magnetic flux to flow through the center.

Loss Mechanisms:
- Skin effect
- Capacitive substrate losses
- Eddy currents in the silicon

Influence of a Lossy Substrate

![Diagram of an equivalent circuit with labels: L, R, C_1, C_2, R_1, R_2, C_{Load}.]

where:
- $L$ is the desired inductance
- $R$ is the series resistance
- $C_1$ and $C_2$ are the capacitance from the inductor to the ground plane
- $R_1$ and $R_2$ are the eddy current losses in the silicon

Guidelines for using spiral inductors on chip:
- Lossy substrate degrades $Q$ at frequencies close to $f_{\text{self}}$
- To achieve an inductor, one must select frequencies less than $f_{\text{self}}$
- The $Q$ of the capacitors associated with the inductor should be very high
Planar Spiral Inductors - Continued

Comments concerning implementation:

1.) Put a metal ground shield between the inductor and the silicon to reduce the capacitance.
   - Should be patterned so flux goes through but electric field is grounded
   - Metal strips should be orthogonal to the spiral to avoid induced loop current
   - The resistance of the shield should be low to terminate the electric field

2.) Avoid contact resistance wherever possible to keep the series resistance low.

3.) Use the metal with the lowest resistance and farthest away from the substrate.

4.) Parallel metal strips if other metal levels are available to reduce the resistance.

Example:

![Multi-Level Spiral Inductors](image)

Multi-Level Spiral Inductors

Use of more than one level of metal to make the inductor.

- Can get more inductance per area
- Can increase the interwire capacitance so the different levels are often offset to get minimum overlap.
- Multi-level spiral inductors suffer from contact resistance (must have many parallel contacts to reduce the contact resistance).
- Metal especially designed for inductors is top level approximately 4µm thick.

\[ Q = 5-6, f_{SR} = 30-40\text{GHz} \]
\[ Q = 10-11, f_{SR} = 15-30\text{GHz} \]

Good for high \( L \) in small area.
**Inductors - Continued**

Self-resonance as a function of inductance. Outer dimension of inductors.

- Magnetic flux is small due to planar structure
- Capacitive coupling to substrate is still present
- Potentially best with a ferromagnetic core
Transformers
Transformer structures are easily obtained using stacked inductors as shown below for a 1:2 transformer.

Method of reducing the interwinding capacitances.

Transformers – Continued
A 1:4 transformer:
Structure-

Measured voltage gain-

\( C_L = 0, 50\text{fF}, 100\text{fF}, 500\text{fF} \) and 1pF. \( C_L \) is the capacitive loading on the secondary.
SUMMARY

• This section has presented and characterized passive components suitable for implementation on silicon integrated circuit technologies.

• Resistors
  Source/drain diffusions, base/emitter diffusions, polysilicon and n-well/collector

• Capacitors
  pn-junction, MOS capacitors (depletion and accumulation), poly-poly, metal-metal

• Varactors – varied using a voltage and vary from 10% to as much as 100% or more

• Inductors
  Limited to nanohenrys
  Very low $Q$ (3-5)
  Not variable

• Transformers
  Reasonably easy to build and work using stacked inductors

• Did not cover several important aspects of IC components
  - Errors
  - Matching
  - Physical aspects (layout)