LECTURE 040 – INTEGRATED CIRCUIT TECHNOLOGY - II

(Reference [7,8])

Objective

The objective of this presentation is:

1.) Illustrate and model the passive components compatible with IC technology

2.) The passive components examined will be those suitable for frequency synthesizers

Outline

- Resistors
- Capacitors
- Inductors
- Summary

© P.E. Allen - 2003

RESISTORS

MOS Resistors - Source/Drain Resistor

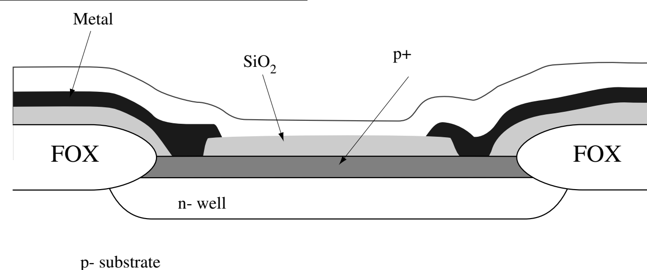


Fig. 2.5-16

Diffusion:

10-100 ohms/square
Absolute accuracy = ±35%
Relative accuracy=2% (5µm), 0.2% (50µm)
Temperature coefficient = +1500 ppm/°C
Voltage coefficient ≈ 200 ppm/V

Ion Implanted:

500-2000 ohms/square
Absolute accuracy = ±15%
Relative accuracy=2% (5µm), 0.15% (50µm
Temperature coefficient = +400 ppm/°C
Voltage coefficient ≈ 800 ppm/V

Comments:

- Parasitic capacitance to substrate is voltage dependent.
- Piezoresistance effects occur due to chip strain from mounting.

© P.E. Allen - 2003

Polysilicon Resistor

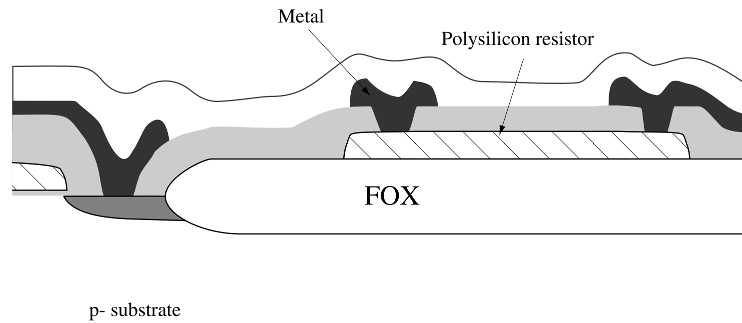


Fig. 2.5-17

30-100 ohms/square (unshielded)

100-500 ohms/square (shielded)

Absolute accuracy = ±30%

Relative accuracy = 2% (5 μm)

Temperature coefficient = 500-1000 ppm/°C

Voltage coefficient ≈ 100 ppm/V

Comments:

- Used for fuzzes and laser trimming
- Good general resistor with low parasitics

© P.E. Allen - 2003

N-well Resistor

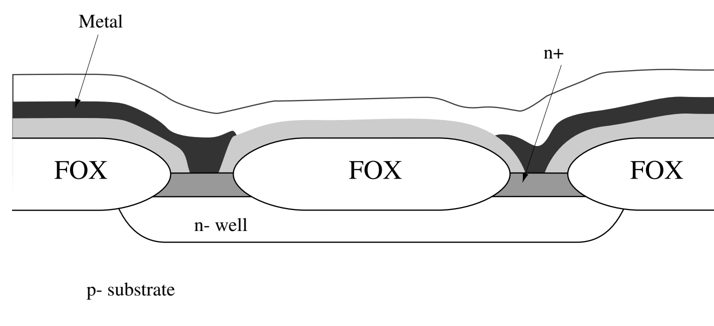


Fig. 2.5-18

1000-5000 ohms/square

Absolute accuracy = ±40%

Relative accuracy ≈ 5%

Temperature coefficient = 4000 ppm/°C

Voltage coefficient is large ≈ 8000 ppm/V

Comments:

- Good when large values of resistance are needed.
- Parasitics are large and resistance is voltage dependent

© P.E. Allen - 2003

CAPACITORS

Types of Capacitors Considered

- pn junction capacitors
- Standard MOS capacitors
- Accumulation mode MOS capacitors
- Poly-poly capacitors
- Metal-metal capacitors

Characterization of Capacitors

Assume C is the desired capacitance:

1.) Dissipation (quality factor) of a capacitor is

$$Q = \omega C R_p$$

where R_p is the equivalent resistance in parallel with the capacitor, C.

2.) C_{max}/C_{min} ratio is the ratio of the largest value of capacitance to the smallest when the capacitor is used as a variable capacitor called *varactor*.

3.) Variation of capacitance with the control voltage.

4.) Parasitic capacitors from both terminal of the desired capacitor to ac ground.

Desirable Characteristics of Varactors

1.) A high quality factor

2.) A control voltage range compatible with supply voltage

3.) Good tunability over the available control voltage range

4.) Small silicon area (reduces cost)

5.) Reasonably uniform capacitance variation over the available control voltage range

6.) A high C_{max}/C_{min} ratio

Some References for Further Information

1.) P. Andreani and S. Mattisson, “On the Use of MOS Varactors in RF VCO’s,” *IEEE J. of Solid-State Circuits*, vol. 35, no. 6, June 2000, pp. 905-910.

2.) A-S Porret, T. Melly, C. Enz, and E. Vittoz, “Design of High-Q Varactors for Low-Power Wireless Applications Using a Standard CMOS Process,” *IEEE J. of Solid-State Circuits*, vol. 35, no. 3, March 2000, pp. 337-345.

3.) E. Pedersen, “RF CMOS Varactors for 2GHz Applications,” *Analog Integrated Circuits and Signal Processing*, vol. 26, pp. 27-36, Jan. 2001

PN Junction Capacitors

Generally made by diffusion into the well.

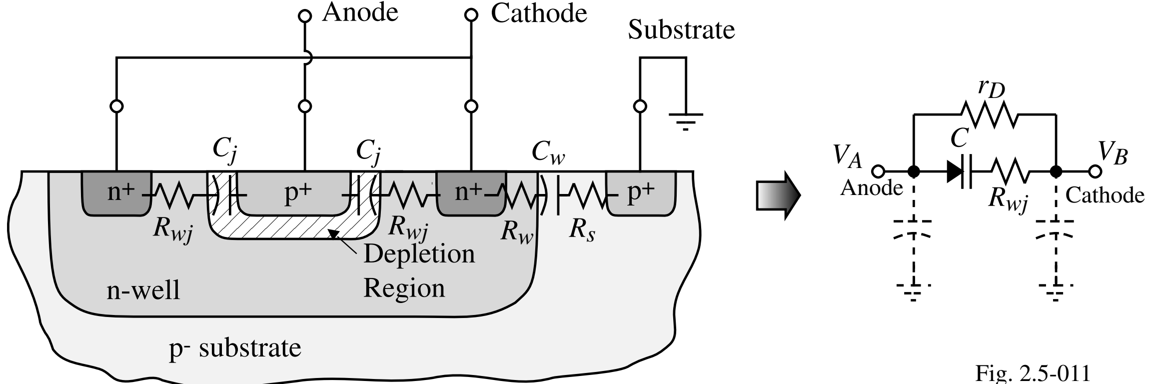


Fig. 2.5-011

Layout:

Minimize the distance between the p+ and n+ diffusions.

Two different versions have been tested.

1.) Large islands – 9µm on a side

2.) Small islands – 1.2µm on a side

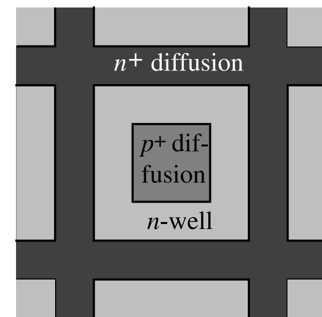


Fig. 2.5-1A

© P.E. Allen - 2003

PN-Junction Capacitors – Continued

The anode should be the floating node and the cathode must be connected to ac ground.

Experimental data (Q at 2GHz, 0.5µm CMOS):

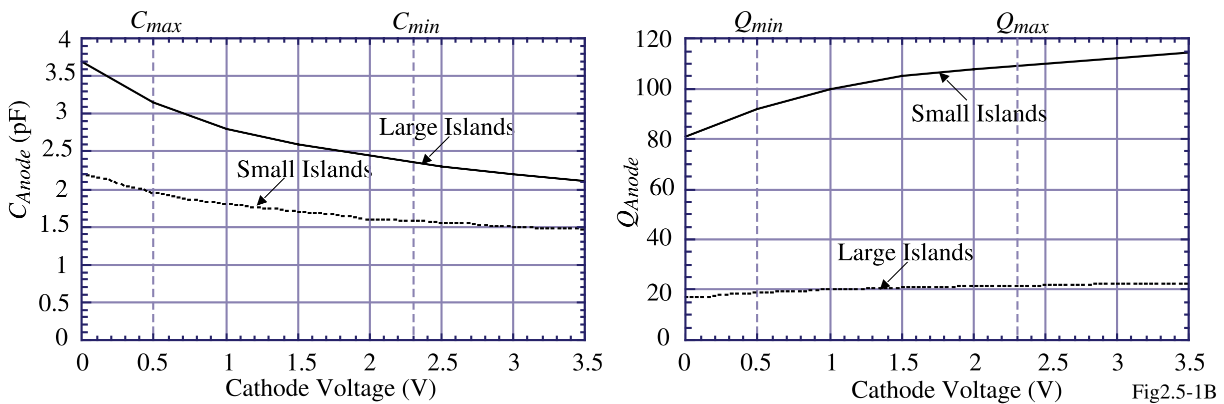


Fig2.5-1B

Summary:

Terminal Under Test	Small Islands (598 1.2µm x1.2µm)			Large Islands (42 9µm x 9µm)		
	C_{max}/C_{min}	Q_{min}	Q_{max}	C_{max}/C_{min}	Q_{min}	Q_{max}
Anode	1.23	94.5	109	1.32	19	22.6
Cathode	1.21	8.4	9.2	1.29	8.6	9.5

Electrons as majority carriers lead to higher Q because of their higher mobility.

The resistance, R_{wj}, is reduced in small islands compared with large islands ⇒ higher Q.

© P.E. Allen - 2003

Single-Ended and Differential PN Junction Capacitors

Differential configurations can reduce the bulk resistances and increase the effective Q.

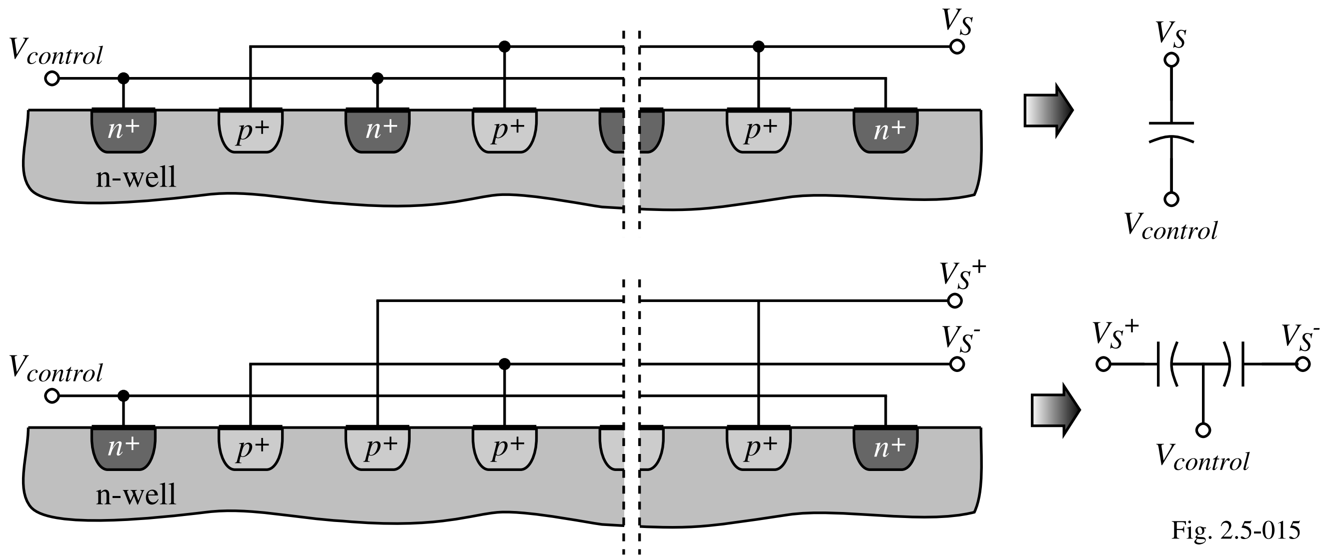


Fig. 2.5-015

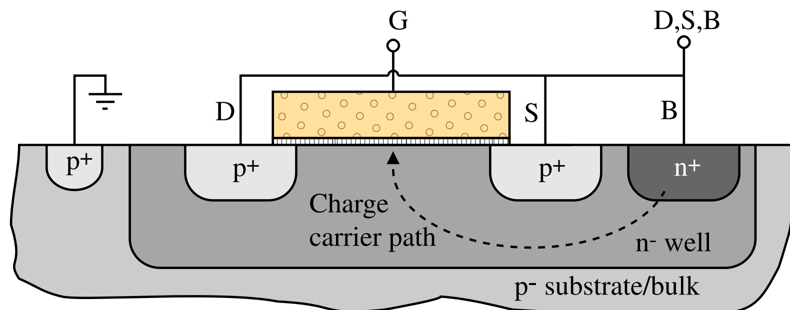
An examination of the electric field lines shows that because the symmetry inherent in the differential configuration, the path to the small-signal ground can be shortened if devices with opposite polarity alternate.

© P.E. Allen - 2003

Standard MOS Capacitor (D = S = B)

Conditions:

- D = S = B
- Operates from accumulation to inversion
- Nonmonotonic
- Nonlinear



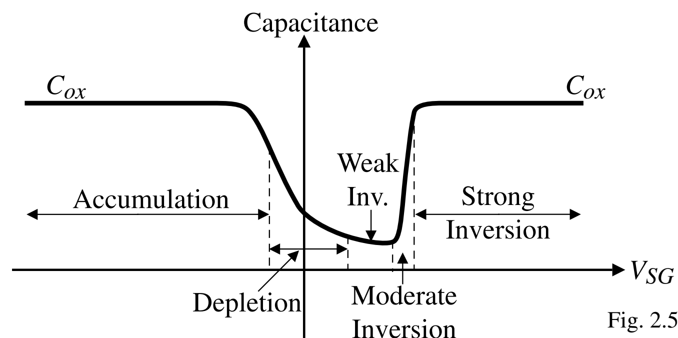


Fig. 2.5-012

© P.E. Allen - 2003

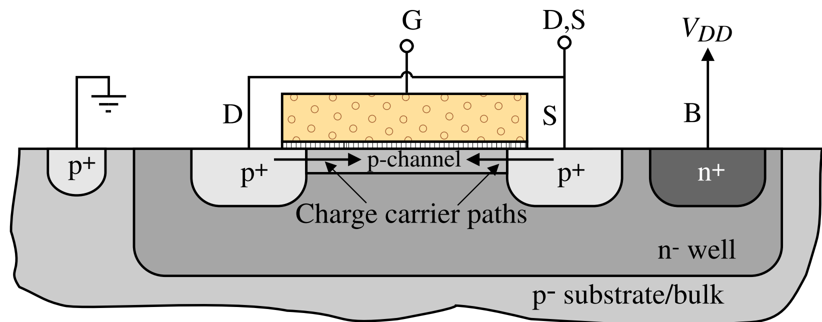
Inversion Mode MOS Capacitors

Conditions:

- D = S, B = V_{DD}
- Accumulation region removed by connecting bulk to V_{DD}
- Channel resistance:

$$R_{on} = \frac{L}{12K_P'(V_{BG}-|V_T|)}$$

- LDD transistors will give lower Q because of the increased series resistance



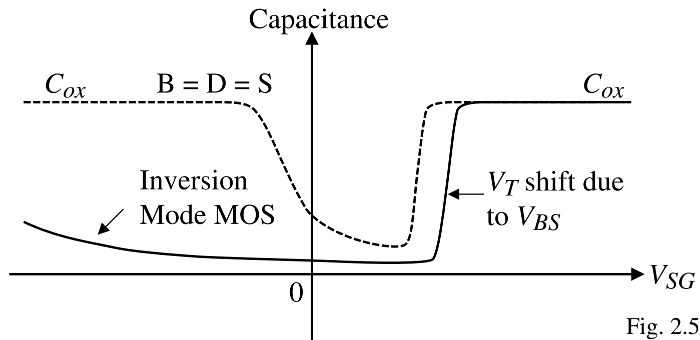
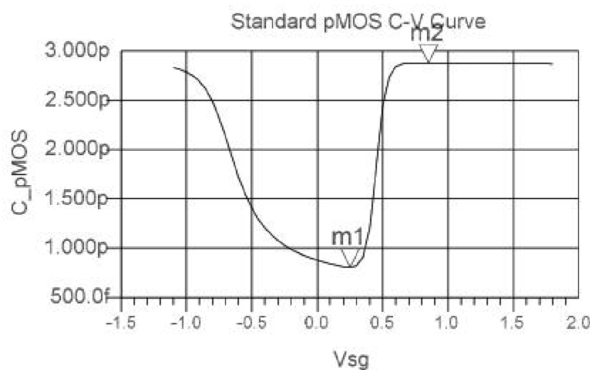
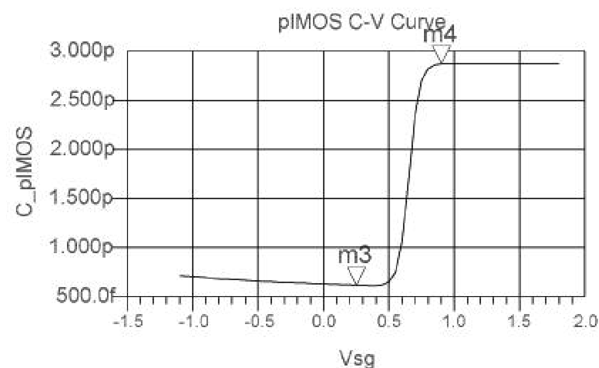


Fig. 2.5-013

Experimental Results for Standard and Inversion Mode 0.25µm CMOS Varactors

n-well:





Inversion Mode MOS Capacitors – Continued

Bulk tuning of the polysilicon-oxide-channel capacitor (0.35μm CMOS)

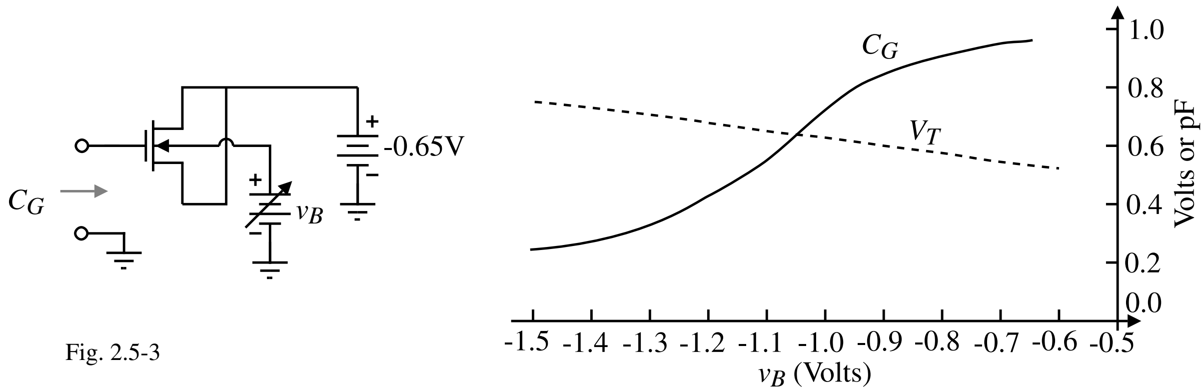


Fig. 2.5-3

$C_{max}/C_{min} \approx 4$

Interpretation:

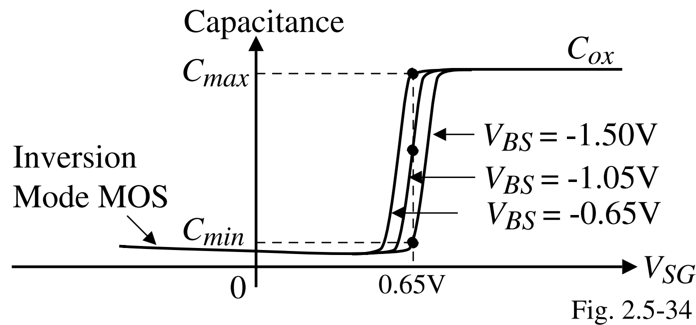


Fig. 2.5-34

© P.E. Allen - 2003

Inversion Mode NMOS Varactor – Continued

More Detail - Includes the LDD transistor

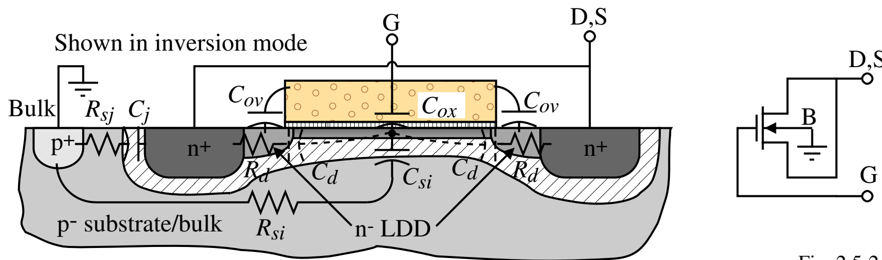


Fig. 2.5-2

Best results are obtained when the drain-source are on ac ground.

Experimental Results (Q at 2GHz, 0.5μm CMOS):

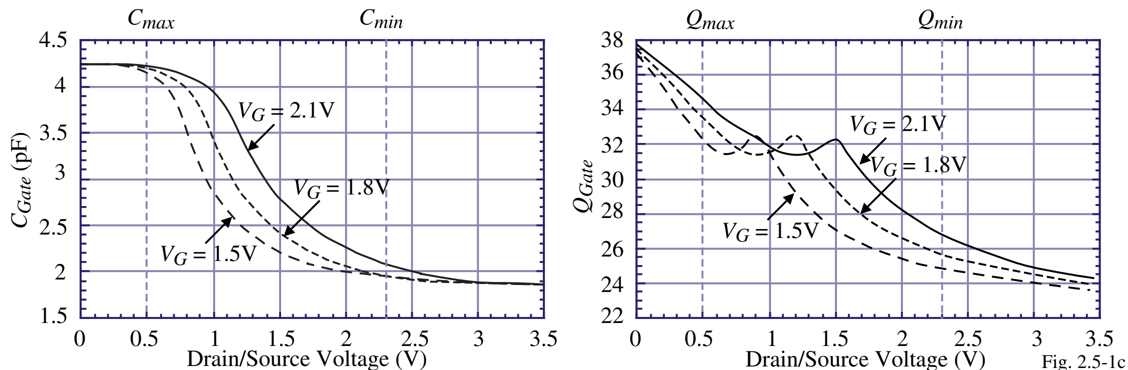


Fig. 2.5-1c

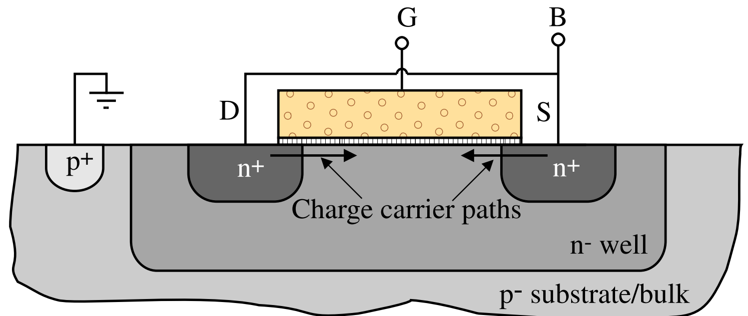
V_G =1.8V: C_{max}/C_{min} ratio = 2.15 (1.91), Q_{max} = 34.3 (5.4), and Q_{min} = 25.8(4.9)

© P.E. Allen - 2003

Accumulation Mode MOS Capacitors

Conditions:

- Remove p+ drain and source and put n+ bulk contacts instead
- Generally not supported (yet) in most silicon foundries



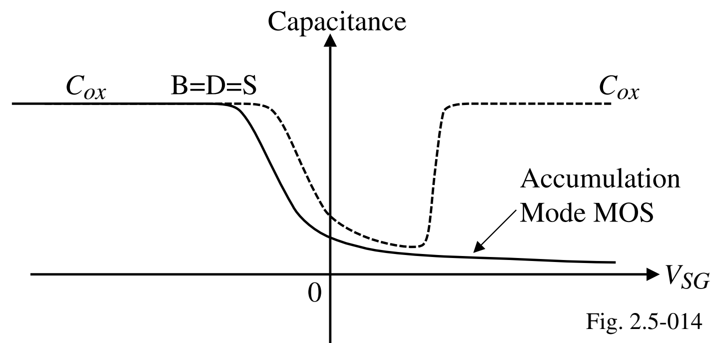


Fig. 2.5-014

Accumulation-Mode Capacitor – More Detail

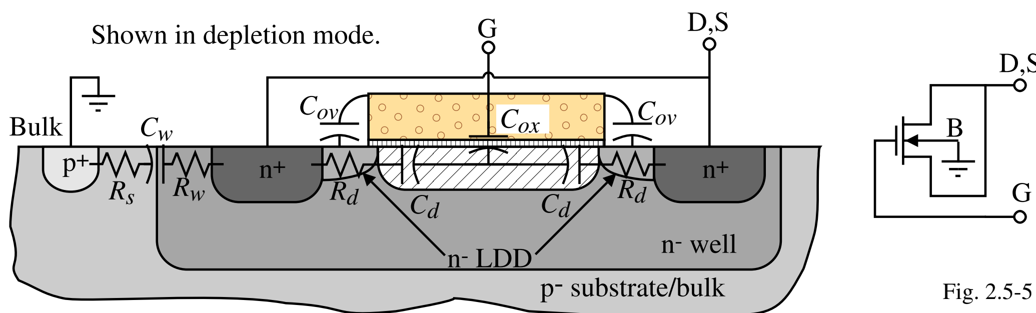


Fig. 2.5-5

Best results are obtained when the drain-source are on ac ground.

Experimental Results (Q at 2GHz, 0.5µm CMOS):

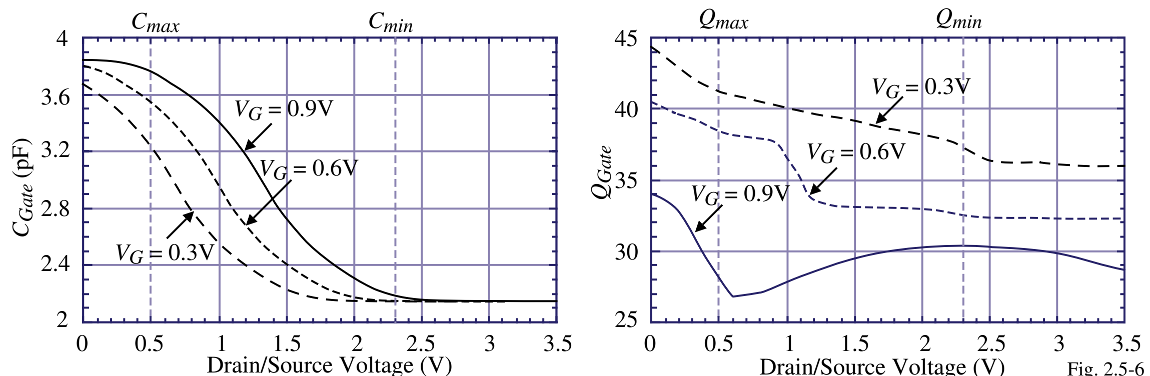
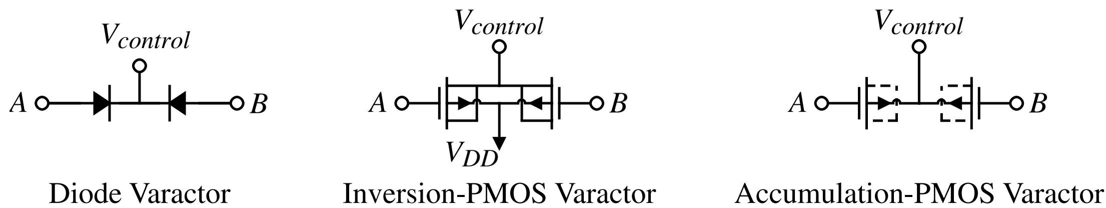


Fig. 2.5-6

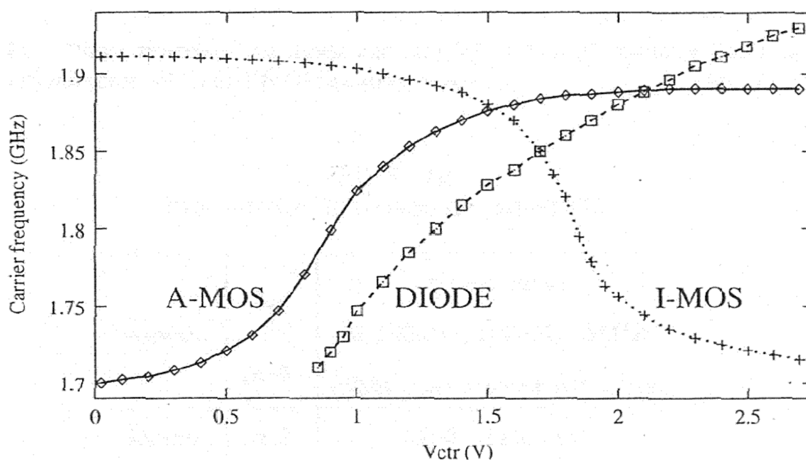
$V_G = 0.6$V: C_{max}/C_{min} ratio = 1.69 (1.61), Q_{max} = 38.3 (15.0), and Q_{min} = 33.2(13.6)

Differential Varactors†



Diode Varactor   Inversion-PMOS Varactor   Accumulation-PMOS Varactor

Fig. 040-01



Varactor	$f_L - f_H$ (GHz)	f_C (GHz)	Tuning Range
Diode	1.73-1.93	1.83	10.9%
I-MOS	1.71-1.91	1.81	11.0%
A-MOS	1.70-1.89	1.80	10.6%

† P. Andreani and S. Mattisson, "On the Use of MOS Varactors in RF VCO's," *IEEE J. of Solid-State Circuits*, Vol. 35, No. 6, June 2000, pp. 905-910.

© P.E. Allen - 2003

Compensated MOS-Capacitors in Depletion with Substrate Biasing†

Substrate biasing keeps the MOS capacitors in a broad depletion region and extends the usable voltage range and achieves a first-order cancellation of the nonlinearity effect.

Principle:

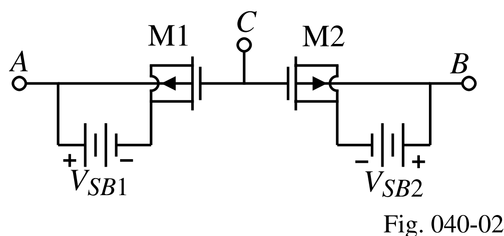
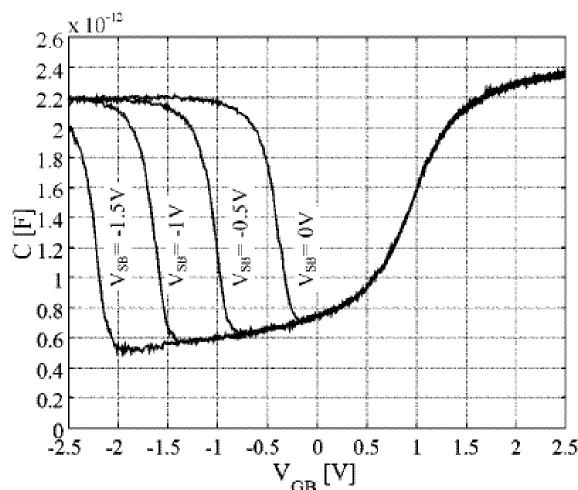


Fig. 040-02

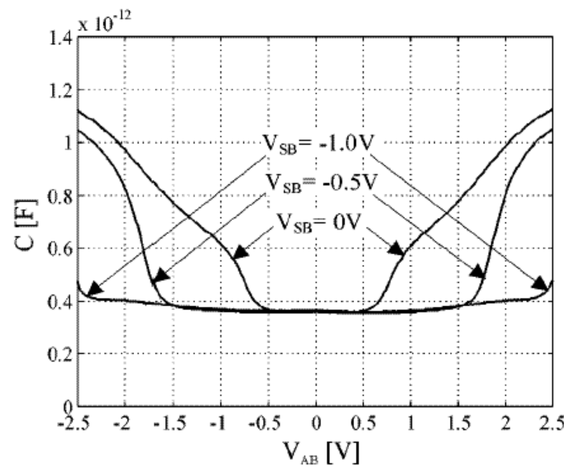


† T. Tille, J. Sauerbrey and D. Schmitt-Landsiedel, "A 1.8V MOSFET-Only ΣΔ Modulator Using Substrate Biased Depletion-Mode MOS Capacitors in Series Compensation," *IEEE J. of Solid-State Circuits*, Vol. 36, No. 7, July 2001, pp. 1041-1047.

© P.E. Allen - 2003

Compensated MOS-Capacitors in Depletion – Continued

Measured CV plot of a series compensated MOS capacitor with different substrate biases (0.25µm CMOS, t_{ox} = 5nm, W_1=W_2=20µm and L_1=L_2=20µm):



Example of a realization of the series compensation without using floating batteries.

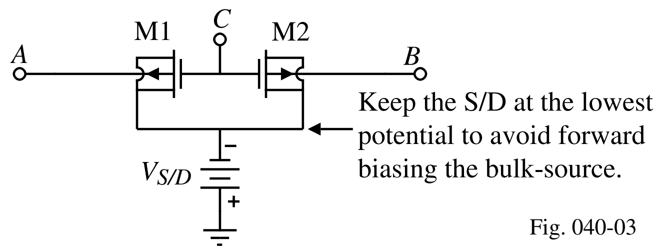
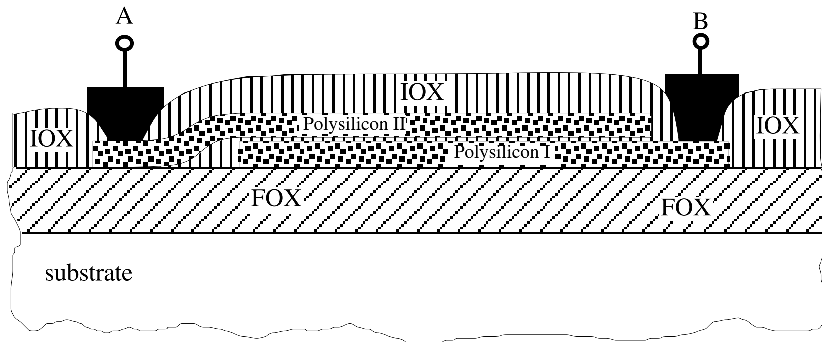


Fig. 040-03

 © P.E. Allen - 2003

MOS Capacitors - Continued

Polysilicon-Oxide-Polysilicon (Poly-Poly):

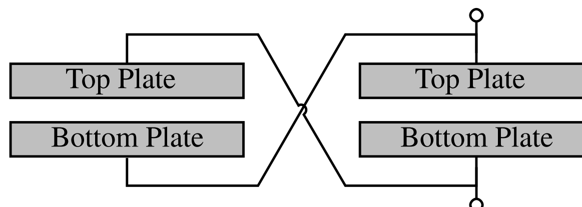


Best possible capacitor for analog circuits

Less parasitics

Voltage independent

Possible approach for increasing the voltage linearity:



 © P.E. Allen - 2003

Implementation of Capacitors using Available Interconnect Layers

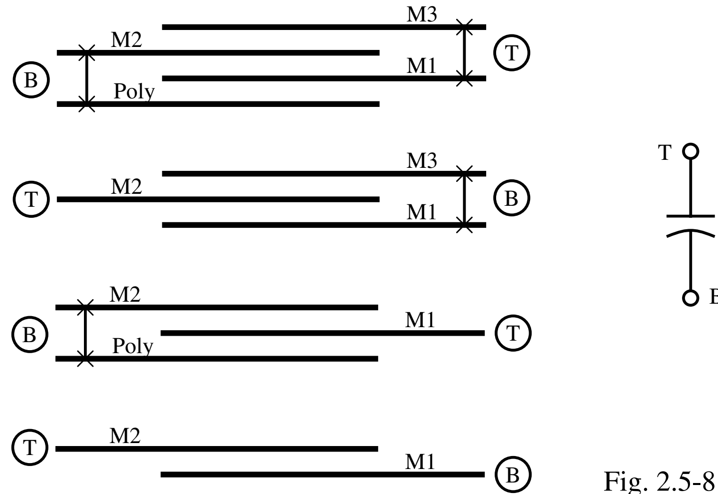


Fig. 2.5-8

Much more information on using metal for capacitance is found in the reference: R. Aparicio and A. Hamimiri, "Capacity Limits and Matching Properties of Integrated Capacitors," *IEEE J. of Solid-State Circuits*, Vol. 37, No. 3, March 2002, pp. 384-393.

Horizontal Metal Capacitors

Capacitance between conductors on the same level and use lateral flux.

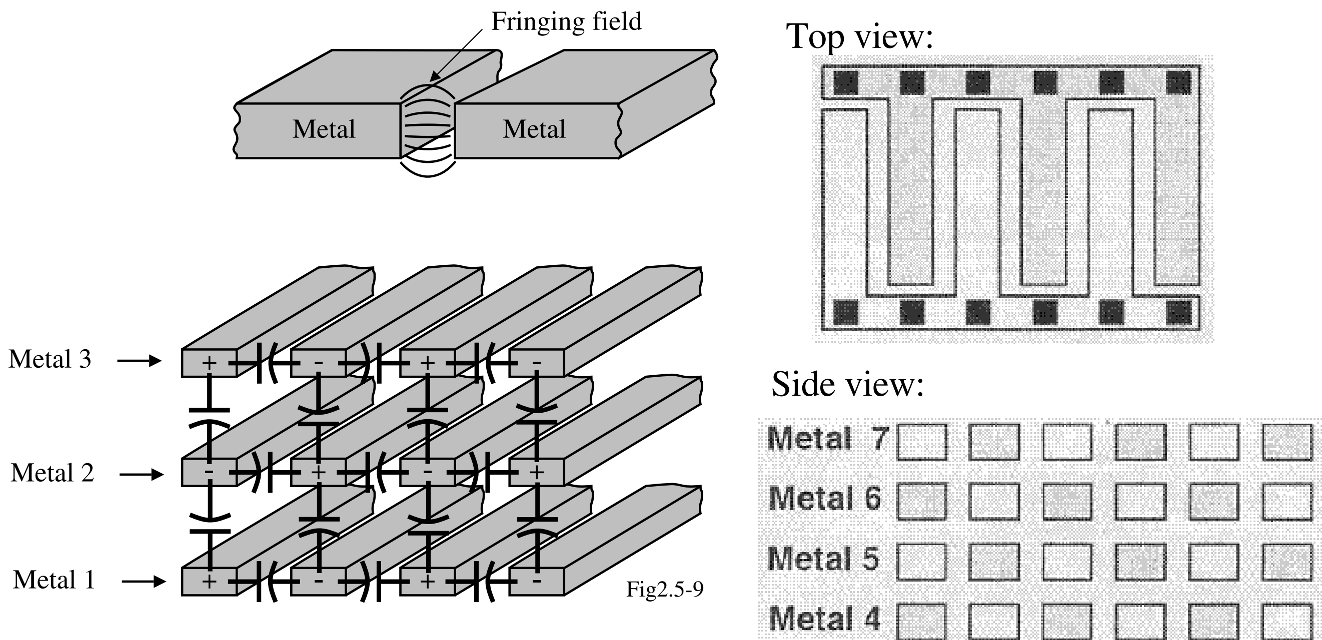


Fig2.5-9

These capacitors are sometimes called fractal capacitors because the fractal patterns are structures that enclose a finite area with an infinite perimeter.

The capacitor/area can be increased by a factor of 10 over vertical flux capacitors.

MOS Passive RC Component Performance Summary

Component Type	Range of Values	Absolute Accuracy	Relative Accuracy	Temperature Coefficient	Voltage Coefficient
Poly-oxide-semi-conductor Capacitor	0.35-0.5 fF/μm²	10%	0.1%	20ppm/°C	±20ppm/V
Poly-Poly Capacitor	0.3-0.4 fF/μm²	20%	0.1%	25ppm/°C	±50ppm/V
Diffused Resistor	10-100 Ω/sq.	35%	2%	1500ppm/°C	200ppm/V
Ion Implanted Resistor	0.5-2 kΩ/sq.	15%	2%	400ppm/°C	800ppm/V
Poly Resistor	30-200 Ω/sq.	30%	2%	1500ppm/°C	100ppm/V
n-well Resistor	1-10 kΩ/sq.	40%	5%	8000ppm/°C	10kppm/V

© P.E. Allen - 2003

INDUCTORS

Inductors

What is the range of values for on-chip inductors?

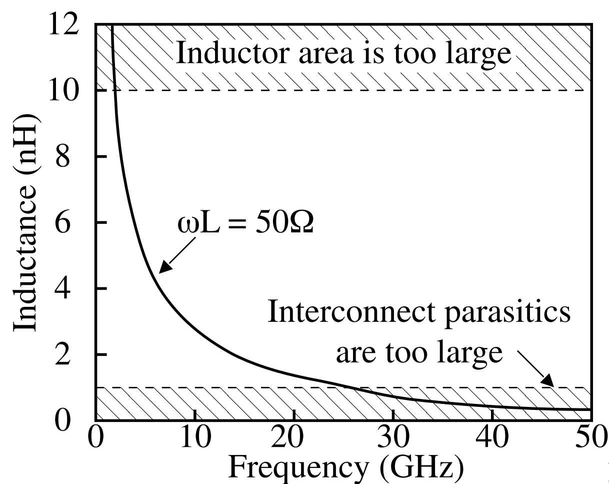


Fig. 6-5

Consider an inductor used to resonate with 5pF at 1000MHz.

$$L = \frac{1}{4\pi^2 f_o^2 C} = \frac{1}{(2\pi\cdot 10^9)^2 \cdot 5\text{x}10^{-12}} = 5\text{nH}$$

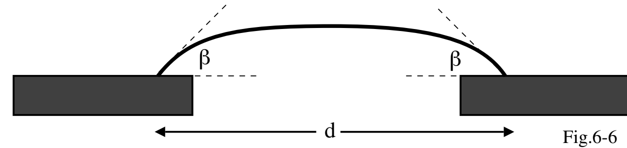
Note: Off-chip connections will result in inductance as well.

© P.E. Allen - 2003

Candidates for inductors in CMOS technology are:

1.) Bond wires
2.) Spiral inductors
3.) Multi-level spiral
4.) Solenoid

Bond wire Inductors:



- Function of the pad distance d and the bond angle β
- Typical value is 1nH/mm which gives 2nH to 5nH in typical packages
- Series loss is 0.2 Ω/mm for 1 mil diameter aluminum wire
- $Q \approx 60$ at 2 GHz

Planar Spiral Inductors

Spiral Inductors on a Lossy Substrate:

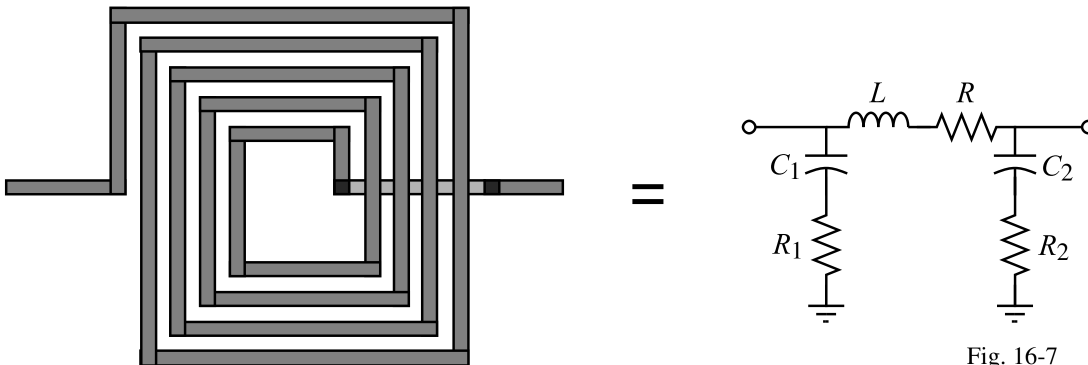


Fig. 16-7

- Design Parameters:

  Inductance, $L = \Sigma(L_{self} + L_{mutual})$

  Quality factor, $Q = \dfrac{\omega L}{R}$

  Self-resonant frequency: $f_{self} = \dfrac{1}{\sqrt{LC}}$

- Trade-off exists between the Q and self-resonant frequency
- Typical values are L = 1-8nH and Q = 3-6 at 2GHz

Planar Spiral Inductors - Continued

Inductor Design

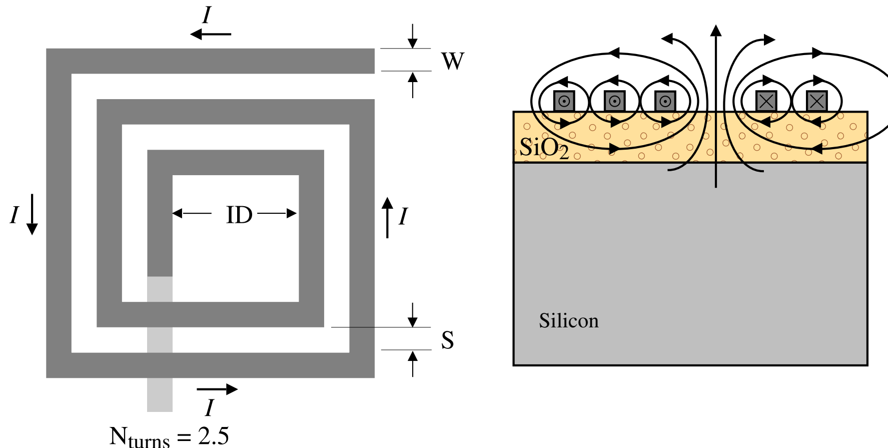


Fig. 6-9

Typically: $3 < N_{turns} < 5$ and $S = S_{min}$ for the given current

Select the OD, N_{turns}, and W so that ID allows sufficient magnetic flux to flow through the center.

Loss Mechanisms:

- Skin effect
- Capacitive substrate losses
- Eddy currents in the silicon

© P.E. Allen - 2003

Planar Spiral Inductors - Continued

Influence of a Lossy Substrate

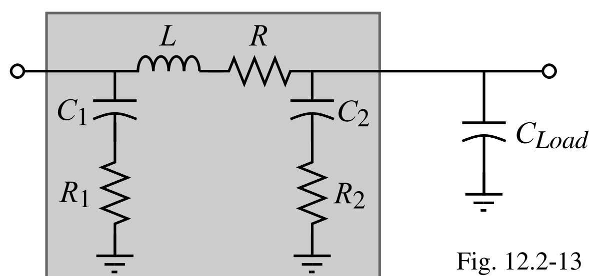


Fig. 12.2-13

where:

L is the desired inductance

R is the series resistance

C_1 and C_2 are the capacitance from the inductor to the ground plane

R_1 and R_2 are the eddy current losses in the silicon

Guidelines for using spiral inductors on chip:

- Lossy substrate degrades Q at frequencies close to f_{self}
- To achieve an inductor, one must select frequencies less than f_{self}
- The Q of the capacitors associated with the inductor should be very high

© P.E. Allen - 2003

Planar Spiral Inductors - Continued

Comments concerning implementation:

1.) Put a metal ground shield between the inductor and the silicon to reduce the capacitance.
    - Should be patterned so flux goes through but electric field is grounded
    - Metal strips should be orthogonal to the spiral to avoid induced loop current
    - The resistance of the shield should be low to terminate the electric field

2.) Avoid contact resistance wherever possible to keep the series resistance low.

3.) Use the metal with the lowest resistance and farthest away from the substrate.

4.) Parallel metal strips if other metal levels are available to reduce the resistance.

Example:

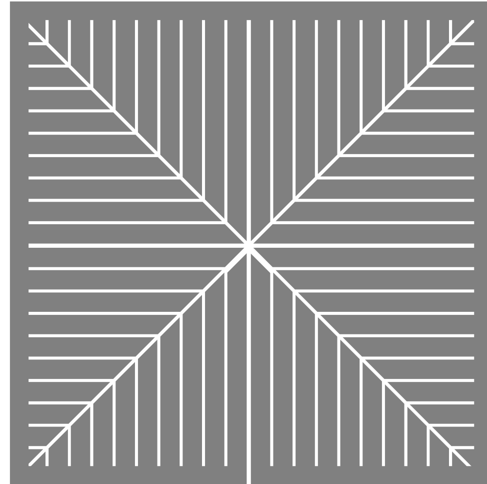


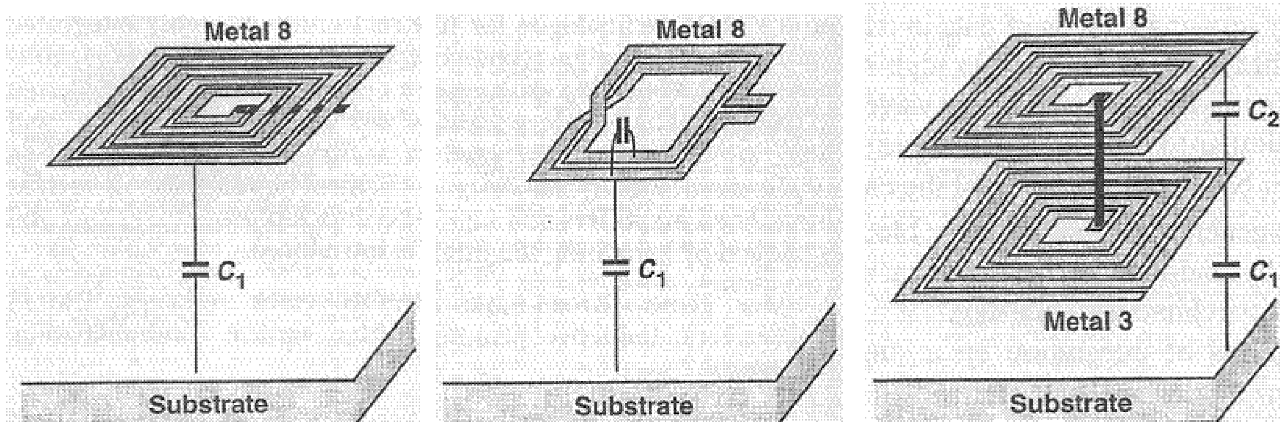
Fig. 2.5-12

© P.E. Allen - 2003

Multi-Level Spiral Inductors

Use of more than one level of metal to make the inductor.

- Can get more inductance per area
- Can increase the interwire capacitance so the different levels are often offset to get minimum overlap.
- Multi-level spiral inductors suffer from contact resistance (must have many parallel contacts to reduce the contact resistance).
- Metal especially designed for inductors is top level approximately 4μm thick.



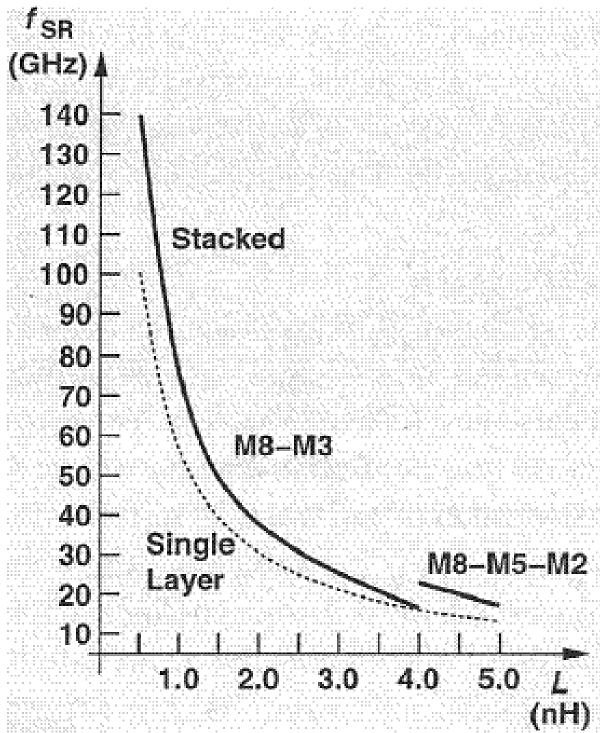
Q = 5-6, f_{SR} = 30-40GHz. Q = 10-11, f_{SR} = 15-30GHz[1]. Good for high L in small area.

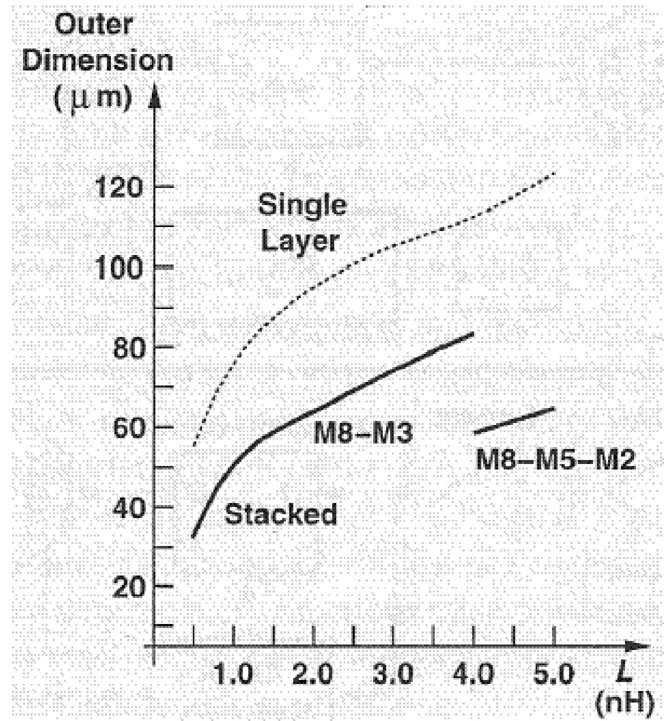
[1] The skin effect and substrate loss appear to be the limiting factor at higher frequencies of self-resonance.

© P.E. Allen - 2003

Inductors - Continued

Self-resonance as a function of inductance. Outer dimension of inductors.





 © P.E. Allen - 2003

Solenoid Inductors

Example:

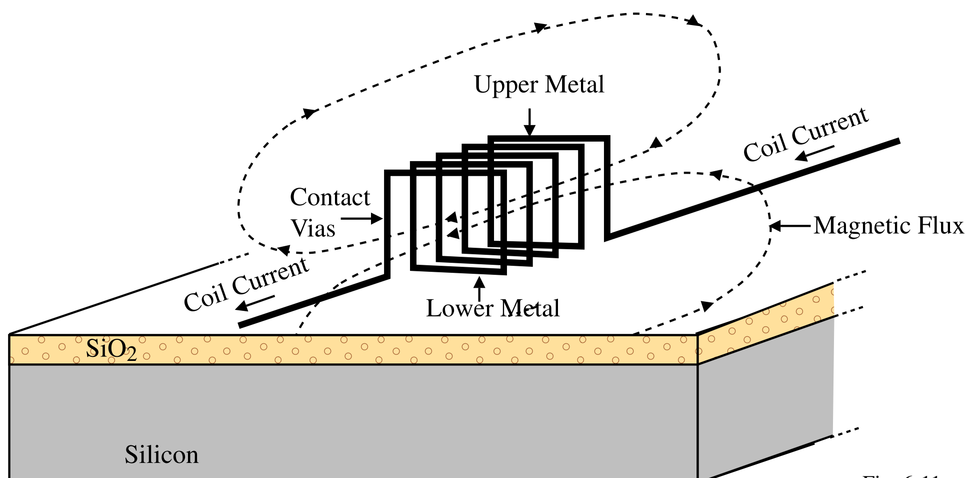


Fig. 6-11

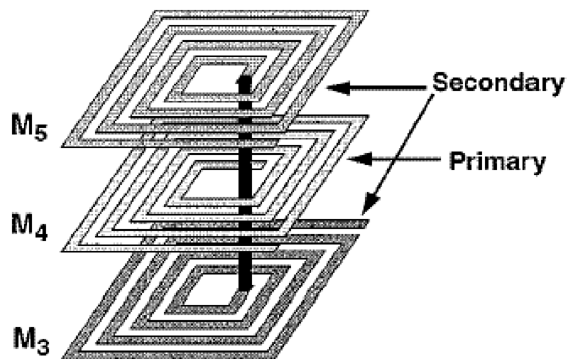
Comments:

- Magnetic flux is small due to planar structure
- Capacitive coupling to substrate is still present
- Potentially best with a ferromagnetic core

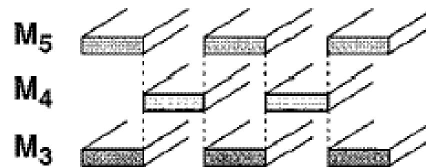
 © P.E. Allen - 2003

Transformers

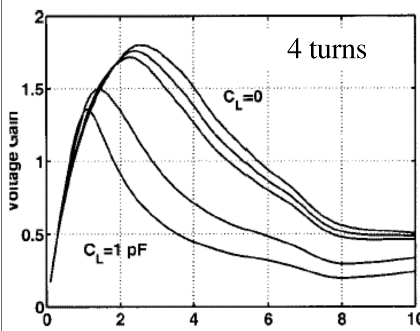
Transformer structures are easily obtained using stacked inductors as shown below for a 1:2 transformer.

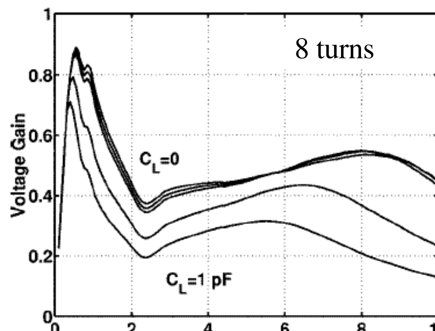


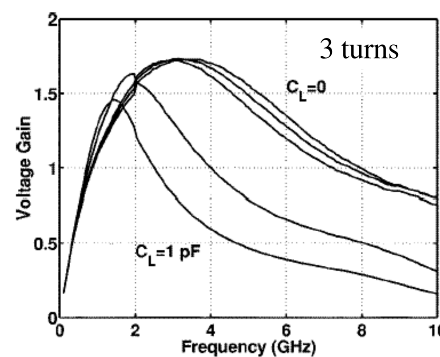
Method of reducing the interwinding capacitances.



Measured 1:2 transformer voltage gains:





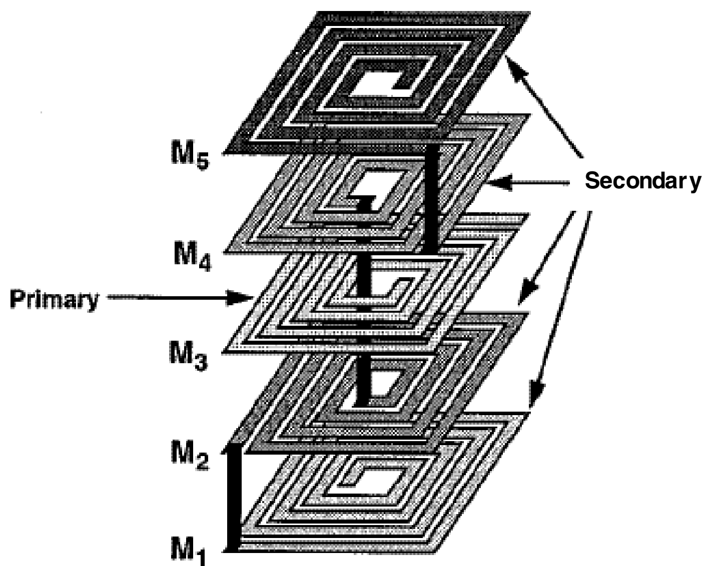


 © P.E. Allen - 2003

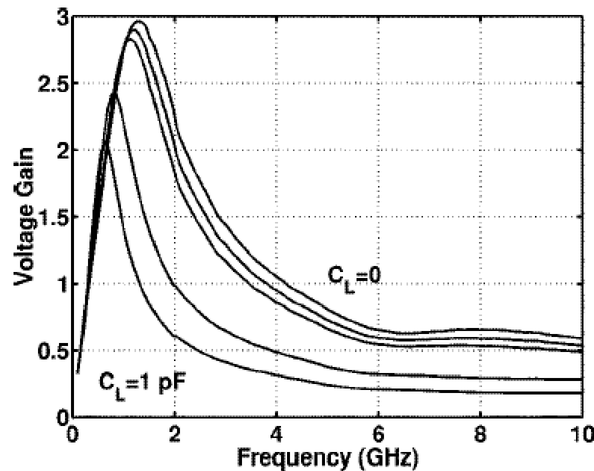
Transformers – Continued

A 1:4 transformer:

Structure-



Measured voltage gain-



(C_L = 0, 50fF, 100fF, 500fF and 1pF. C_L is the capacitive loading on the secondary.)

 © P.E. Allen - 2003

SUMMARY

- This section has presented and characterized passive components suitable for implementation on silicon integrated circuit technologies.
- Resistors
  - Source/drain diffusions, base/emitter diffusions, polysilicon and n-well/collector
- Capacitors
  - pn-junction, MOS capacitors (depletion and accumulation), poly-poly, metal-metal
- Varactors – varied using a voltage and vary from 10% to as much as 100% or more
- Inductors
  - Limited to nanohenrys
  - Very low Q (3-5)
  - Not variable
- Transformers
  - Reasonably easy to build and work using stacked inductors
- Did not cover several important aspects of IC components
  - Errors
  - Matching
  - Physical aspects (layout)

 © P.E. Allen - 2003