LECTURE 070 – DIGITAL PHASE LOCK LOOPS (DPLL)

(Reference [2])

DIGITAL PHASE LOCKED LOOPS (DPLL)

Outline

- Building Blocks of the DPLL
- Dynamic Performance of the DPLL
- Noise Performance of the DPLL
- DPLL Design Procedure
- DPLL System Simulation

BUILDING BLOCKS OF THE DPLL

Block Diagram of the DPLL

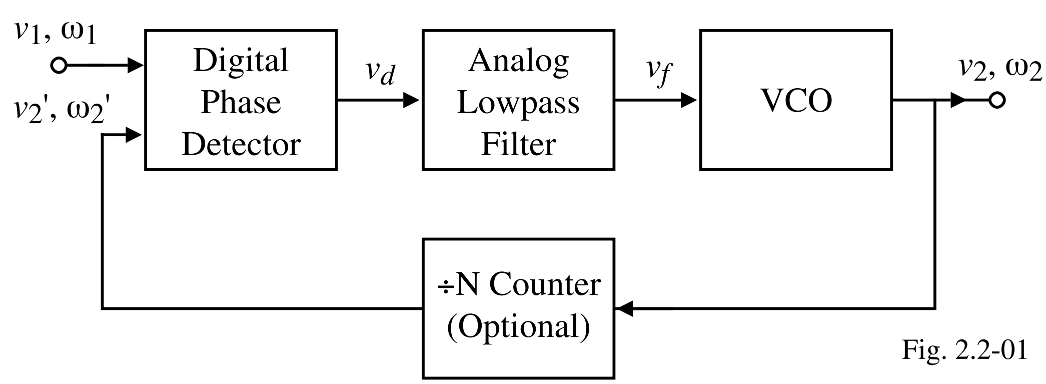


Fig. 2.2-01

- The only digital block is the phase detector and the remaining blocks are similar to the LPLL
- The divide by N counter is used in frequency synthesizer applications.

$$\omega_2' = \omega_1 = \frac{\omega_2}{N} \quad \rightarrow \quad \omega_2 = N\,\omega_1$$

DIGITAL PHASE DETECTORS

Introduction

Key assumption in digital phase detectors: $v_1(t)$ and $v_2(t)$ are square waves. This may require amplification and limiting.

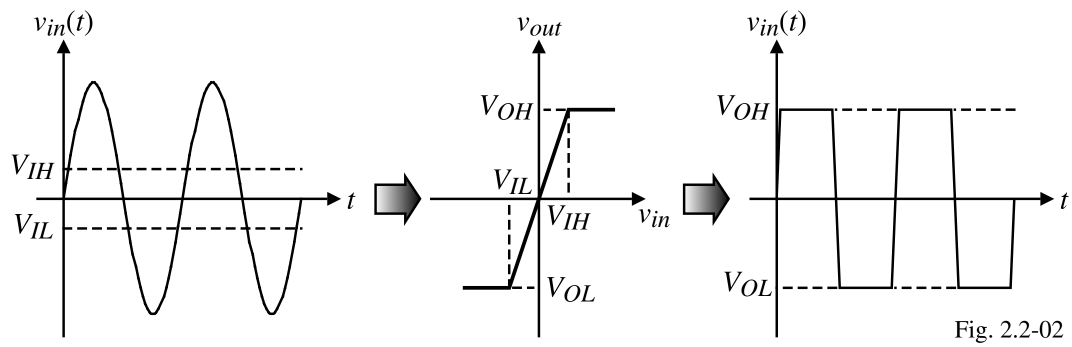


Fig. 2.2-02

Types of digital phase detectors:

1.) EXOR gate

2.) The edge-triggered JK flip-flop

3.) The phase-frequency detector

The EXOR Gate

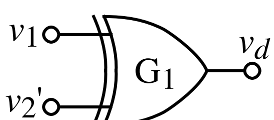


Fig. 2.2-03

v_1	v_2’	v_d
0	0	0
0	1	1
1	0	1
1	1	0

Zero Phase Error:

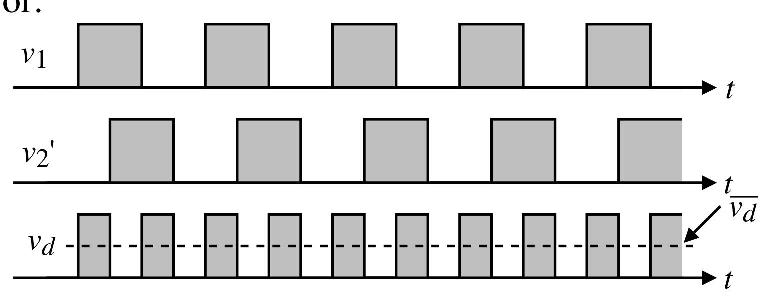


Fig. 2.2-04

Positive Phase Error:

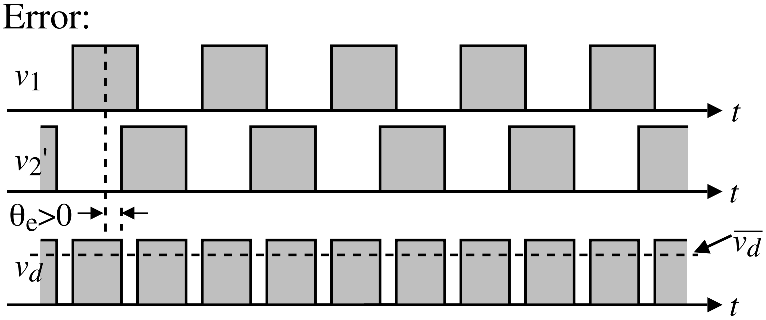
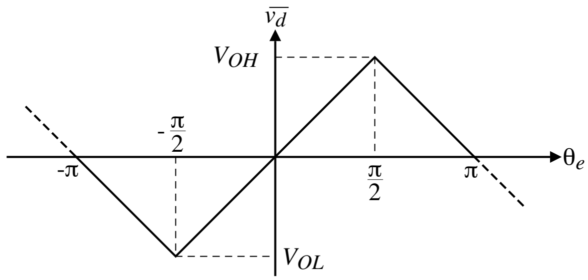


Fig. 2.2-05

EXOR Gate – Continued

Assume that the average value of v_d, is shifted to zero for zero phase error, θ_e. $\overline{v_d}$ can be plotted as,



$$K_d = \frac{V_{OH}-V_{OL}}{\pi}$$

Fig. 2.2-06

If v_1 and v_2' are asymmetrical (have different duty cycles), then $\overline{v_d}$ becomes,

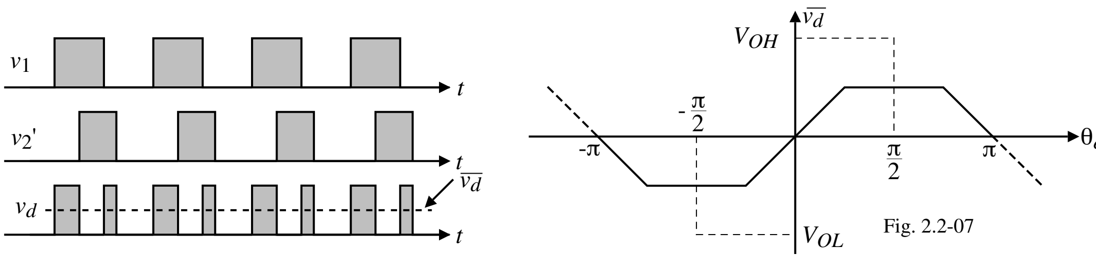


Fig. 2.2-07

The effect of waveform asymmetry is to reduce the loop gain of the DPLL and also results in a smaller lock range, pull-in range, etc.

JK Flip-Flop

The JK Flip-Flop is not sensitive to waveform asymmetry because it is edge-triggered.

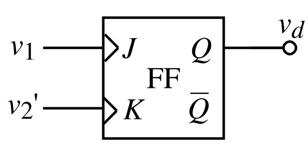


Fig. 2.2-08

v_1	v_2’	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

Zero Phase Error (Assume rising edge triggered):

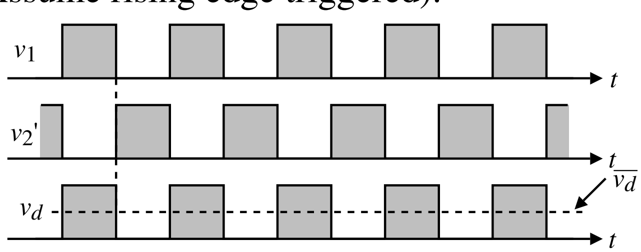


Fig. 2.2-09

Positive Phase Error:

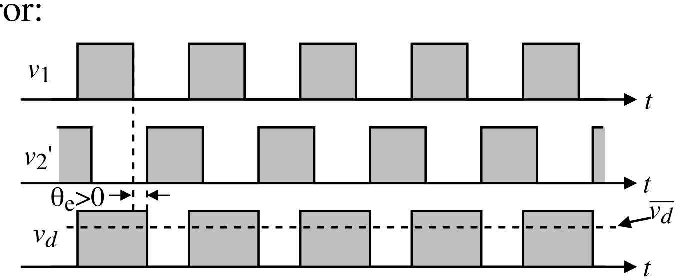
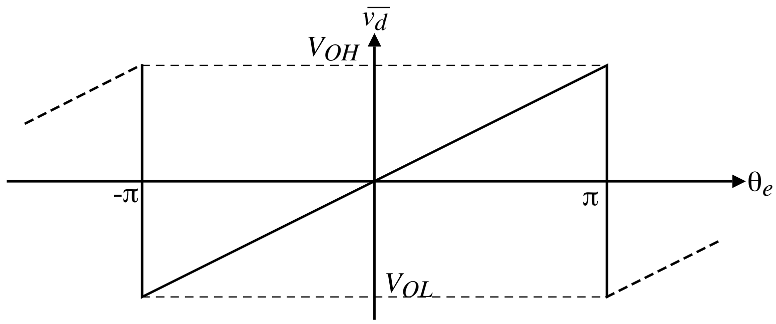


Fig. 2.2-10

JK Flip-Flop Phase Detector – Continued

Input-Output Characteristic:



$$K_d = \frac{V_{OH}\text{-}V_{OL}}{2\pi}$$

Fig. 2.2-11

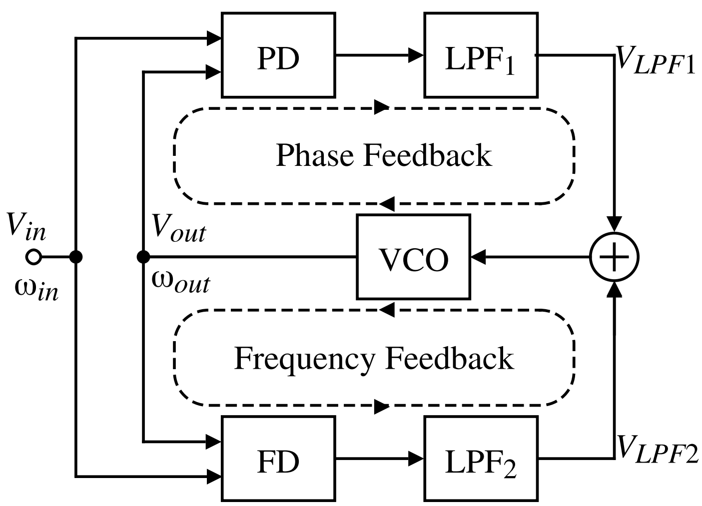
Comments:

- Symmetry of v_1 and v_2' is unimportant
- Both the EXOR and the JK flip-flop have a severely limited pull-in range if the loop filter does not have a pole at zero.

The Phase-Frequency Detector (PFD)

The PFD can detect both the phase and frequency difference between v_1 and v_2'.

Conceptual diagram:



The output signal of the PFD depends on the phase error in the locked state and on the frequency error in the unlocked state.

Consequently, the PFD will lock under any condition, irrespective of the type of loop filter used.

The PFD – Continued

PFD implementation:

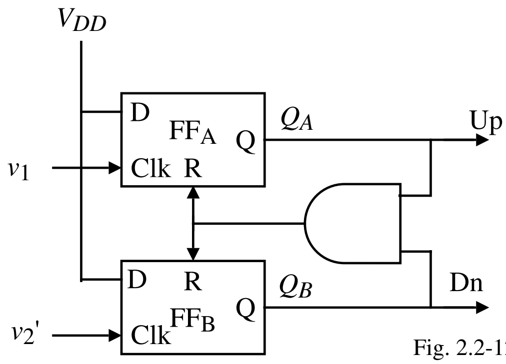


Fig. 2.2-12

No AND Gate

Q_A	Q_B
0	0
1	0
0	1
1	1

With AND Gate

Q_A	Q_B
1	0→State=+1
0	0→State = 0
0	1→State=-1

PFD State Diagram:

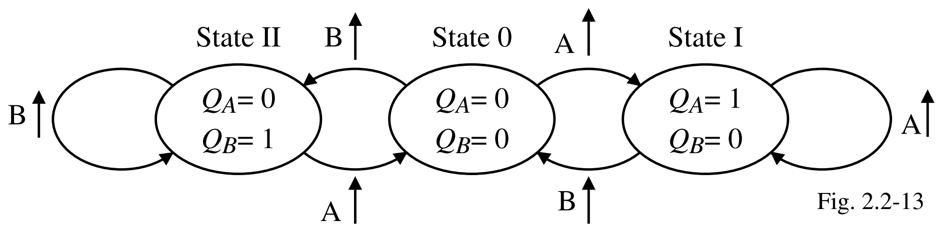


Fig. 2.2-13

Unlike the EXOR gates and the R-S latches, the PFD generates two outputs which are not complementary.

Illustration of a PFD

PFD ($\omega_A = \omega_B$):

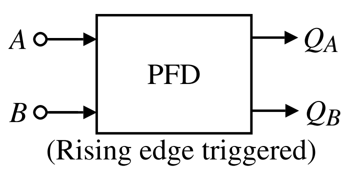


Fig. 2.2-14

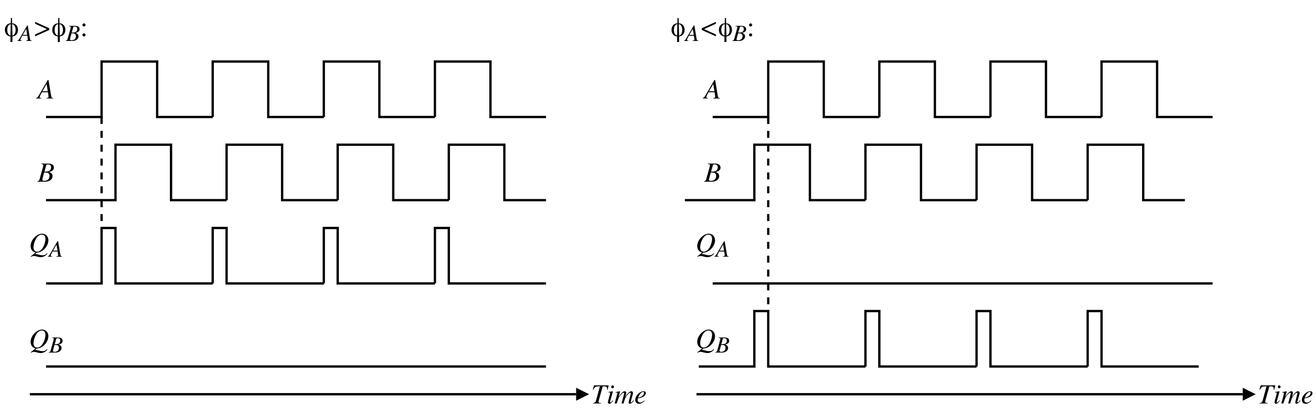


Fig. 2.2-15

Illustration of the PFD- Continued

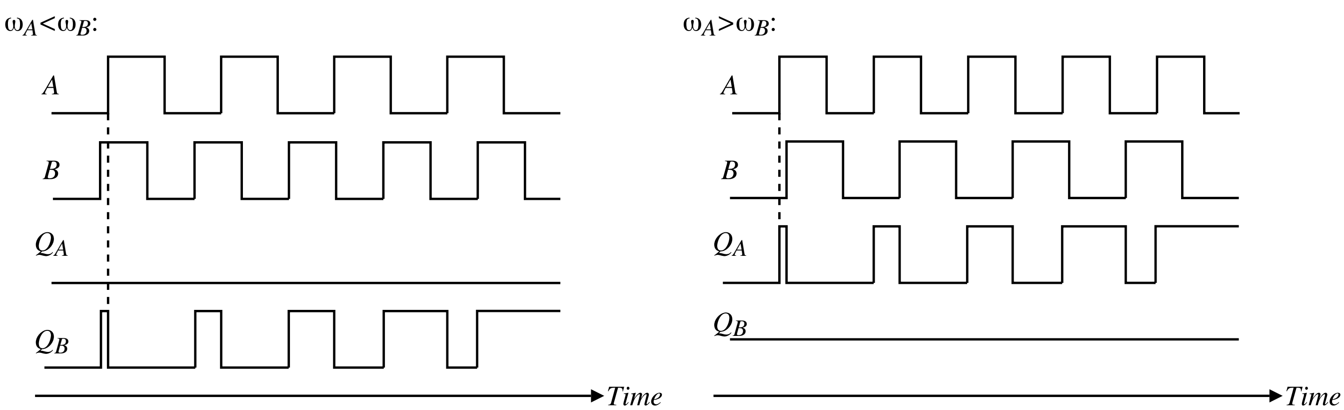


Fig. 2.2-16

PFD – Continued

Plot of the PFD output versus phase error:

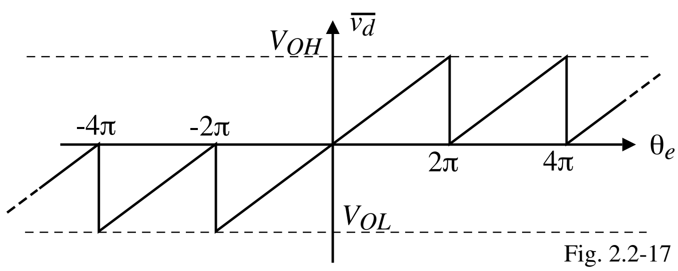


Fig. 2.2-17

When θ_e exceeds $\pm 2\pi$, the PFD behaves as if the phase error recycled at zero.

$$\therefore \quad K_d = \frac{V_{OH}-V_{OL}}{4\pi}$$

A plot of the averaged duty cycle of v_d versus ω_1/ω_2' (ω_A/ω_B) in the unlocked state of the DPLL:

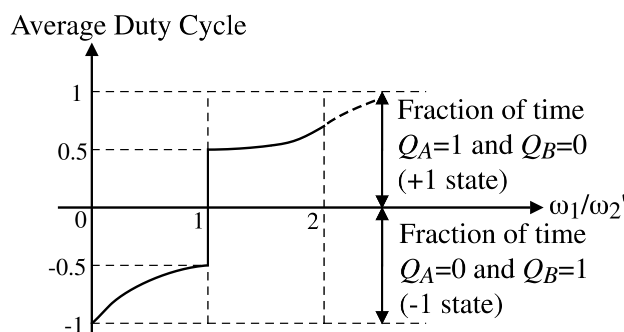


Fig. 2.2-18

CHARGE PUMPS

Charge Pumps

A charge pump consists of two switched current sources controlled by Q_A and Q_B which drive a capacitor or a combination of a resistor and a capacitor to form a filter for the PLL with a pole at the origin.

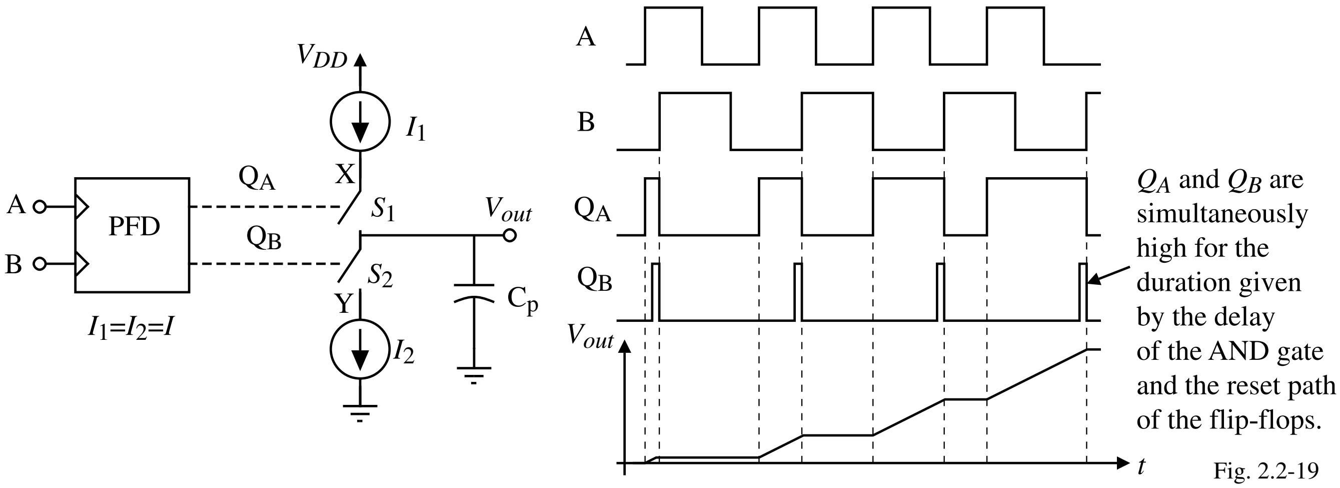


Fig. 2.2-19

$\omega_A > \omega_B$ or $\omega_A = \omega_B$ but $\theta_A > \theta_B$: S_1 is on and V_{out} increases.

$\omega_A < \omega_B$ or $\omega_A = \omega_B$ but $\theta_A < \theta_B$: S_2 is on and V_{out} decreases.

A Charge-Pump PLL

Block diagram:

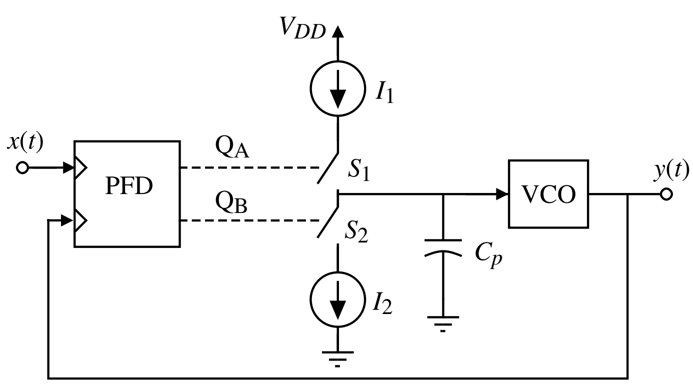


Fig. 2.2-20

The charge pump and capacitor C_p serve as the loop filter for the PLL.

The charge pump can provide infinite gain for a static phase shift.

Step Response of a Charge Pump PLL

Assume that the period of the input is T_1 and the charge pump provides a current of $\pm I_p$ to the capacitor C_p.

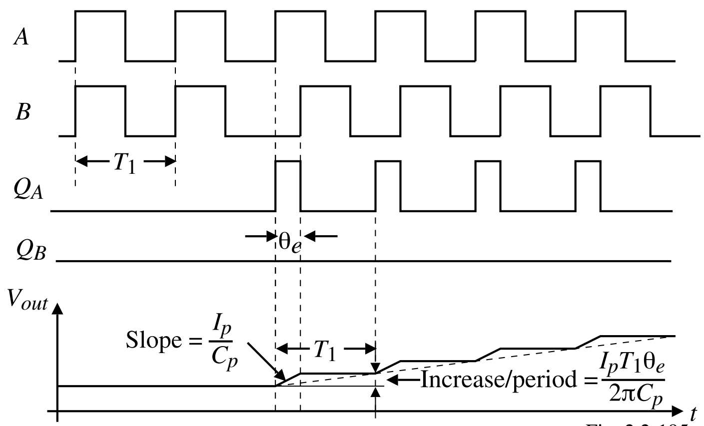


Fig. 2.2-195

Detector gain?

Since the steady-state gain = ∞, it is more meaningful to define K_d as follows,

$$\text{Amount of } v_d(t) \text{ increase per period } (T_1) = \frac{I_p}{C_p} \times \frac{\theta_e}{2\pi/T_1} = \frac{I_p T_1 \theta_e}{2\pi C_p}$$

$$\text{Average slope per period} = \frac{I_p T_1 \theta_e}{2\pi C_p} \times \frac{1}{T_1} = \frac{I_p \theta_e}{2\pi C_p}$$

$$v_d(t) = \text{Average Slope}\cdot\Delta\theta = \frac{I_p}{2\pi C_p}\cdot\theta_e\mu(t)$$

Taking the Laplace transform gives,

$$V_d(s) = \frac{I_p}{2\pi C_p s}\frac{\theta_e}{s} \qquad \rightarrow \qquad K_d = \frac{I_p}{2\pi C_p}\frac{\text{V}}{\text{rads}}$$

A Charge-Pump PLL – Continued

$$\frac{Y(s)}{X(s)} = \frac{V_2(s)}{V_1(s)} = ?$$

$$Y(s) = \frac{K_o}{s}V_d(s) = \frac{K_oK_d}{s^2}[X(s) - Y(s)] \qquad \rightarrow \qquad \frac{Y(s)}{X(s)} = \frac{K_oK_d}{s^2 + K_oK_d}$$

which has poles at $\pm j\sqrt{K_oK_d}$. To avoid instability, a zero must be introduced by the resistor in series with C_p.

$$V_d(s) = \frac{I}{2\pi}\left(R + \frac{1}{sC_p}\right) = \frac{I}{s2\pi C_p}(sRC_p + 1) = \frac{K_d}{s}(s\tau_p + 1)$$

$$\therefore \qquad Y(s) = \frac{K_o}{s}V_d(s) = \frac{K_oK_d}{s^2}(s\tau_p + 1)\,[X(s) - Y(s)]$$

$$Y(s)\left[1 + \frac{K_oK_d}{s^2}(s\tau_p + 1)\right] = \frac{K_oK_d}{s^2}(s\tau_p + 1)X(s)$$

$$\frac{Y(s)}{X(s)} = \frac{K_oK_d(s\tau_p + 1)}{s^2 + K_oK_d\tau_p s + K_oK_d}$$

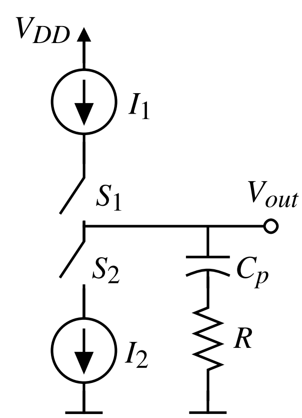


Fig. 2.2-21

Equating to the standard second-order denominator gives,

$$\omega_n = \sqrt{K_oK_d} \text{ and } \zeta = \frac{\omega_n \tau_p}{2}$$

Nonideal Effects of Charge-Pumps

1.) Dead zone.

A dead zone occurs when Q_A or Q_B do not reach their full logic levels. This is due to delay differences in the AND gate and the flip-flops. It is easily removed by proper synchronization of the delays.

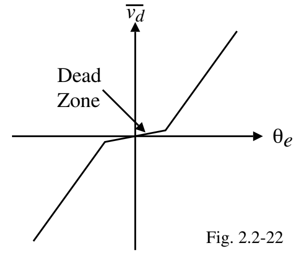


Fig. 2.2-22

2.) Mismatch between I_1 and I_2.

To eliminate the dead zone, Q_A and Q_B can be simultaneously high for a small time. If $I_1 \neq I_2$, the output varies even though $\theta_e = 0$. (Can introduce spurs.)

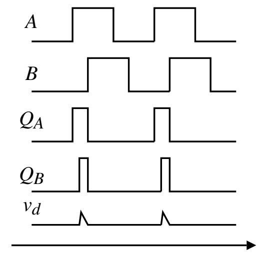


Fig. 2.2-23

3.) Charge injection.

When the S_1 and S_2 switches turn off, they can inject/remove charge from C_p. Changes ω_2.

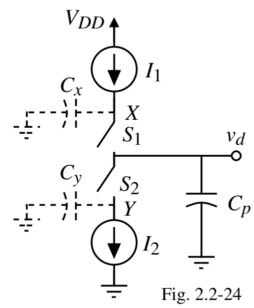


Fig. 2.2-24

4.) Charge sharing.

If $X \rightarrow V_{DD}$ and $Y = 0$ when S_1 and S_2 are off, the VCO will experience a jump when S_1 or S_2 turns on. This periodic effect introduces sidebands (spurs) at the output.

DYNAMIC PERFORMANCE OF THE DPLL

Types of PLLs

Type I – Open-loop transfer function has one pole at the origin.

Type II – Open-loop transfer function has two poles at the origin.

The above transfer functions may also have other roots but not at the origin.

Model for the DPLL

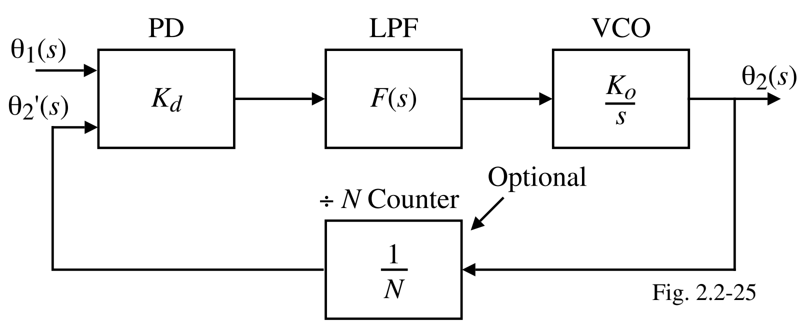


Fig. 2.2-25

Various configurations of the DPLL:

1.) Phase detector – EXOR, J-K flip-flop, or PFD

2.) Filter –

Passive lag with or without a charge pump
Active lag with or without a charge pump
Active PI with or without a charge pump

Loop Filters

1.) Passive lag-

PD $\rightarrow$ $F(s) = \dfrac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)}$

PFD $\rightarrow$ $F(s) \approx \dfrac{1 + s\tau_2}{s(\tau_1 + \tau_2)}$

Experimental results using the PFD with a passive lag filter show that the gain of the passive filter is not constant. As a result, the filter dynamics become nonlinear.

2.) Active lag-

PD $\rightarrow$ $F(s) = K_a\dfrac{1 + s\tau_2}{1 + s\tau_1}$

PFD $\rightarrow$ $F(s) \approx \dfrac{1 + s\tau_2}{s\tau_1}$

3.) Active PI-

PD or PFD $\rightarrow$ $F(s) = \dfrac{1 + s\tau_2}{s\tau_1}$

The Hold Range, $\Delta\omega_H$

The hold range, $\Delta\omega_H$, is the frequency range within which the PLL operation is statically stable. The hold range for various types of DPLLs are:

Type of PD	EXOR	EXOR	EXOR	JK-FF	JK-FF	JK-FF	PFD
Loop Filter	Passive Lag	Active Lag	Active PI	Passive Lag	Active Lag	Active PI	All Filters
$\Delta\omega_H$	$\dfrac{K_oK_d(\pi/2)}{N}$	$\dfrac{K_oK_d(\pi/2)}{N}$	∞	$\dfrac{K_oK_d\pi}{N}$	$\dfrac{K_oK_dK_a\pi}{N}$	∞	∞

The Lock Range, $\Delta\omega_L$

The lock range is the offset between ω_1 and ω_2/N that causes the DPLL to acquire lock with one beat note between ω_1 and $\omega_2' = \omega_2/N$.

1.) PD = EXOR

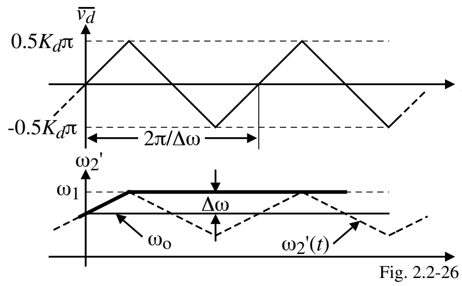


Fig. 2.2-26

Recall that $\Delta\omega_L(\text{LPLL}) = 2\zeta\omega_n$

and $\Delta\omega_L \propto$ Range of $\theta_e = \Delta\theta_e$

But, $\Delta\theta_e(\text{EXOR}) = 0.5\pi\, \Delta\theta_e(\text{LPLL})$

$\therefore\ \Delta\omega_L = 0.5\pi(2\zeta\omega_n) = \pi\zeta\omega_n$

$$\boxed{\Delta\omega_L = \pi\zeta\omega_n}$$

2.) PD =JK-Flip flop

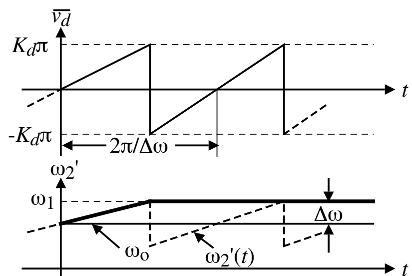


Fig. 2.2-27

$\Delta\theta_e(\text{EXOR}) = \pi\, \Delta\theta_e(\text{LPLL})$

$\therefore\ \Delta\omega_L = \pi(2\zeta\omega_n)$

$$\boxed{\Delta\omega_L = 2\pi\zeta\omega_n}$$

3.) PD = PFD

$\Delta\theta_e(\text{PFD}) = 2\pi\, \Delta\theta_e(\text{LPLL}) \rightarrow \quad \Delta\omega_L = 2\pi(2\zeta\omega_n) \quad \rightarrow \quad \boxed{\Delta\omega_L = 4\pi\zeta\omega_n}$

The lock time for all cases is $T_p \approx 2\pi/\omega_n$.

The Pull-In Range, $\Delta\omega_p$, and the Pull-In Time, T_p

The pull-in range, $\Delta\omega_p$, is the largest $\Delta\omega = |\omega_1 - \omega_2'|$ for which an unlocked loop will lock.

The pull-in time, T_p, is the time required for the loop to lock.

EXOR as the PD:

Waveforms-

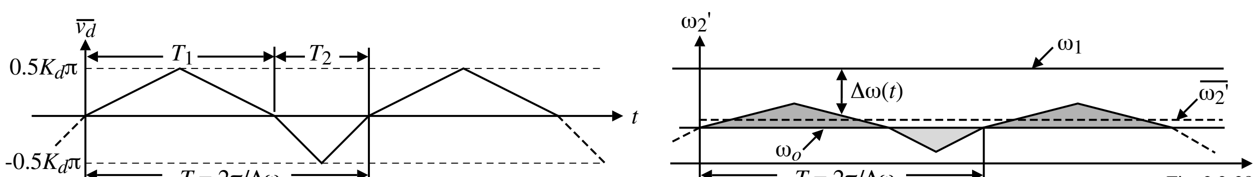


Fig. 2.2-28

$T_1 > T_2$ because $\Delta\omega$ is smaller when $\overline{v_d}$ is positive and larger when $\overline{v_d}$ is negative.

Results-

Type of Filter	$\Delta\omega_p$ (Low loop gains)	$\Delta\omega_p$ (High loop gains)	Pull-in Time, T_p
Passive Lag	$\frac{\pi}{2}\sqrt{2\zeta\omega_n K_o K_d - \omega_n^2}$	$\frac{\pi}{\sqrt{2}}\sqrt{\zeta\omega_n K_o K_d}$	$\frac{4}{\pi^2}\frac{\Delta\omega_o^2}{\zeta\omega_n^3}$
Active Lag	$\frac{\pi}{2}\sqrt{2\zeta\omega_n K_o K_d - \frac{\omega_n^2}{K_a}}$	$\frac{\pi}{\sqrt{2}}\sqrt{\zeta\omega_n K_o K_d}$	$\frac{4}{\pi^2}\frac{\Delta\omega_o^2}{\zeta\omega_n^3}$
Active PI	∞	∞	$\frac{4}{\pi^2}\frac{\Delta\omega_o^2}{\zeta\omega_n^3}$

The Pull-In Range, $\Delta\omega_p$, and the Pull-In Time, T_p-Continued

JK Flip-Flop as the PD:

Waveforms-

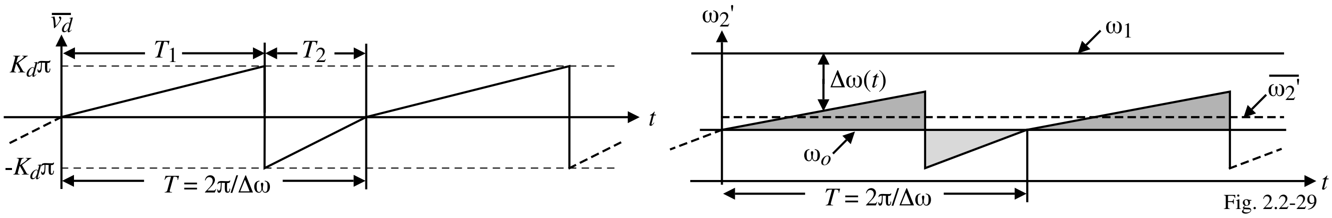


Fig. 2.2-29

$T_1 > T_2$ because $\Delta\omega$ is smaller when $\overline{v_d}$ is positive and larger when $\overline{v_d}$ is negative.

Results-

Type of Filter	$\Delta\omega_p$ (Low loop gains)	$\Delta\omega_p$ (High loop gains)	Pull-in Time, T_p
Passive Lag	$\pi\sqrt{2\zeta\omega_n K_o K_d - \omega_n^2}$	$\pi\sqrt{2}\sqrt{\zeta\omega_n K_o K_d}$	$\frac{1}{\pi^2}\frac{\Delta\omega_o^2}{\zeta\omega_n^2}$
Active Lag	$\pi\sqrt{2\zeta\omega_n K_o K_d - \frac{\omega_n^2}{K_a}}$	$\pi\sqrt{2}\sqrt{\zeta\omega_n K_o K_d}$	$\frac{1}{\pi^2}\frac{\Delta\omega_o^2}{\zeta\omega_n^2}$
Active PI	∞	∞	$\frac{4}{\pi^2}\frac{\Delta\omega_o^2}{\zeta\omega_n^2}$

$\Delta\omega_p$ and T_p for the PFD

Assume that the PFD uses a single power supply of V_{DD}. The various waveforms are,

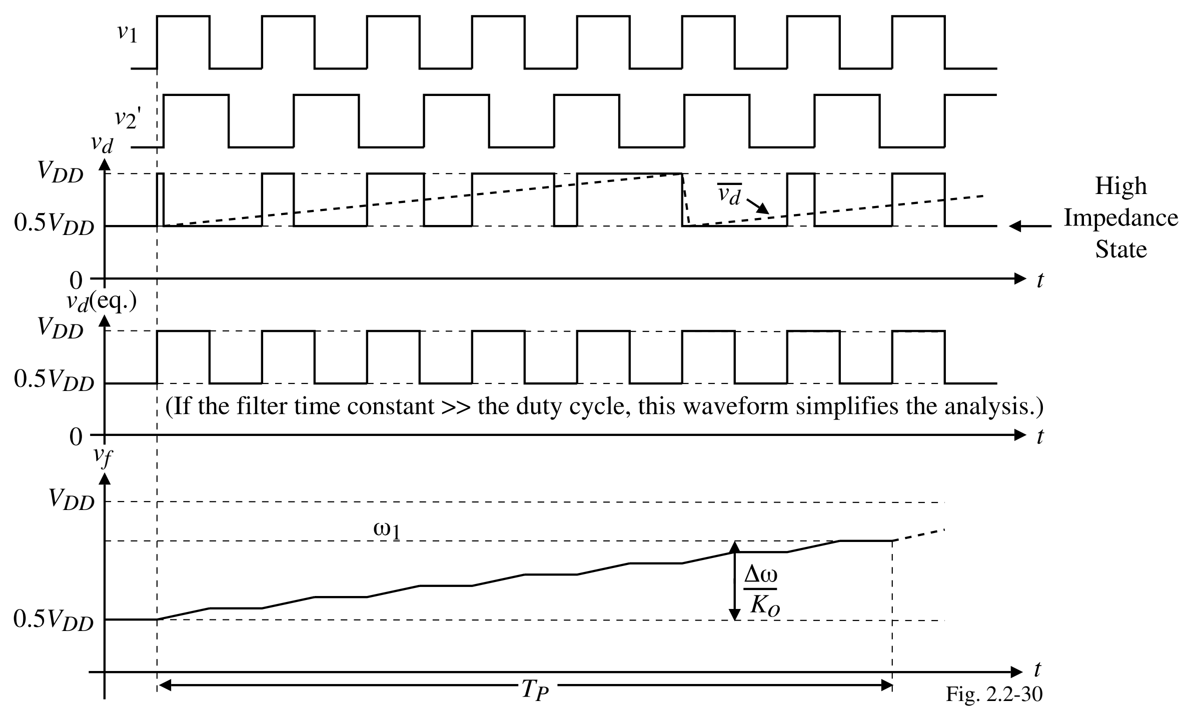


Fig. 2.2-30

v_d(eq.) is a 50% duty cycle model of the PFD to find T_p.

$\Delta\omega_p$ and T_p for the PFD – Continued

Since $\Delta\omega_p = \infty$, let us find T_p using the following model for the passive lag filter:

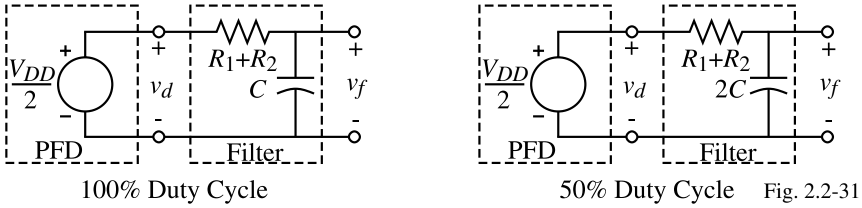


Fig. 2.2-31

Use the 50% duty cycle model, solve for the time necessary to increase v_f by $\Delta\omega/K_o$.

1.) Loop filter = Passive lag

$$T_p = 2(\tau_1+\tau_2)\ ln\left(\frac{K_oV_{DD}/2}{K_oV_{DD}/2 - \Delta\omega_o}\right)$$

2.) Loop filter = Active lag

$$T_p = 2\tau_1\ ln\left(\frac{K_oK_aV_{DD}/2}{K_oK_aV_{DD}/2 - \Delta\omega_o}\right)$$

3.) Loop filter = Active PI

$$T_p = \frac{2\tau_1\Delta\omega_o}{K_oV_{DD}/2}$$

For split power supplies, replace V_{DD} with $(V_{OH}\text{-}V_{OL})$.

The Pull-Out Range, $\Delta\omega_{po}$

The pull-out range is the size of the frequency step applied to the reference input that causes the PLL to lose phase tracking.

1.) EXOR: $\Delta\omega_{po} \approx 2.46\omega_n(\zeta + 0.65)$ for $0.1 < \zeta < 3$

2.) JK Flip-flop:

$$\Delta\omega_{po} = \pi\omega_n \exp\left[\frac{\zeta}{\sqrt{1-\zeta^2}}\tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right)\right],\ \zeta < 1$$

$$\Delta\omega_{po} = \pi\omega_n e,\quad \zeta = 1$$

$$\Delta\omega_{po} = \pi\omega_n \exp\left[\frac{\zeta}{\sqrt{1-\zeta^2}}\tanh^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right)\right],\ \zeta > 1$$

$\Delta\omega_{po} \approx 5.78\omega_n(\zeta + 0.5)$ for all ζ

3.) PFD:

$$\Delta\omega_{po} = 2\pi\omega_n \exp\left[\frac{\zeta}{\sqrt{1-\zeta^2}}\tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right)\right],\ \zeta < 1$$

$$\Delta\omega_{po} = 2\pi\omega_n e,\quad \zeta = 1$$

$$\Delta\omega_{po} = 2\pi\omega_n \exp\left[\frac{\zeta}{\sqrt{1-\zeta^2}}\tanh^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right)\right],\ \zeta > 1$$

$\Delta\omega_{po} \approx 11.55\omega_n(\zeta + 0.5)$ for all ζ

NOISE PERFORMANCE OF THE DPLL

Combination of Noise and Information

In the LPLL, the noise and information signals are added because of the linear multiplier PD.

The noise supression of DPLL's is generally better than LPLL's but no theory of noise exists for the DPLL.

The following pages provide some insight into the noise performance of the DPLL.

Noise Performance of a DPLL with an EXOR PD

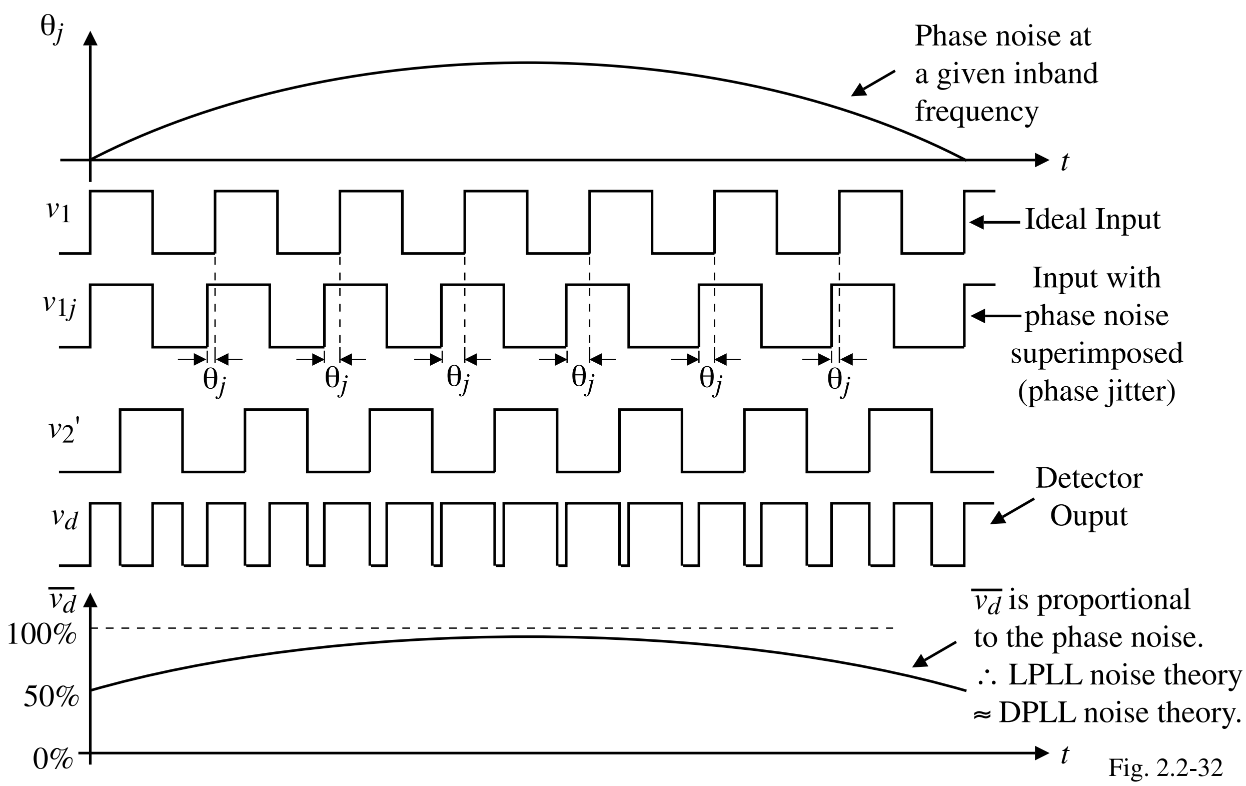


Fig. 2.2-32

Phase Noise in a Communication Signal

Consider the following simple noise model-

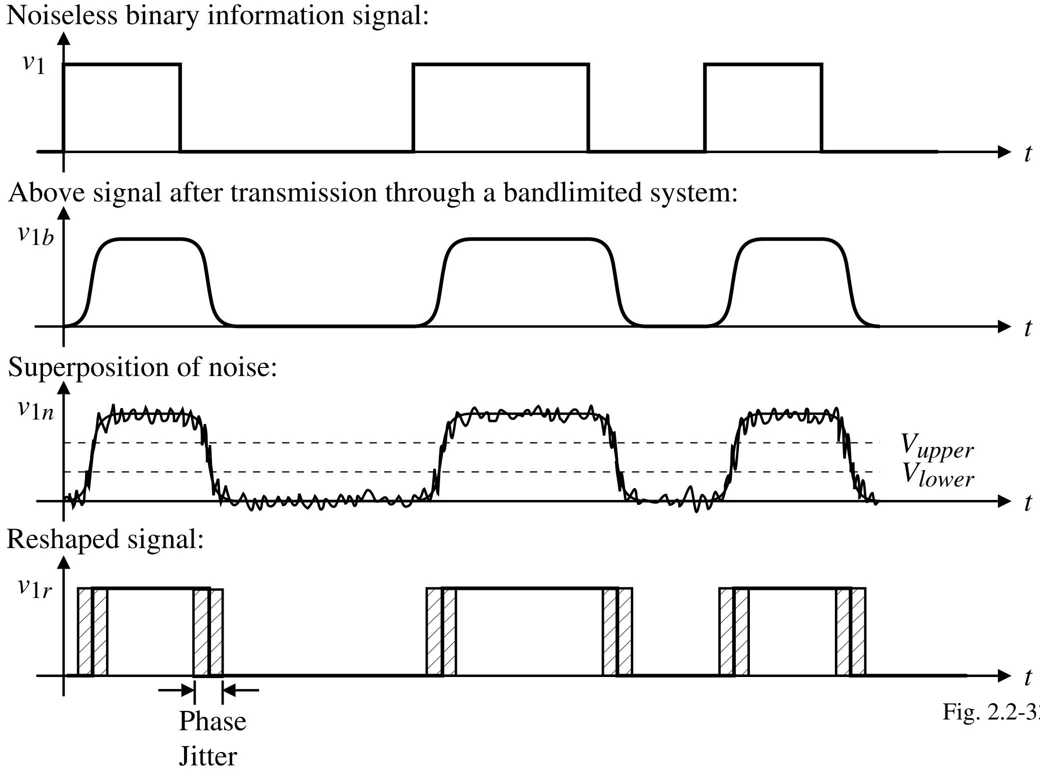


Fig. 2.2-33

Input Signal-to-Noise Ratio

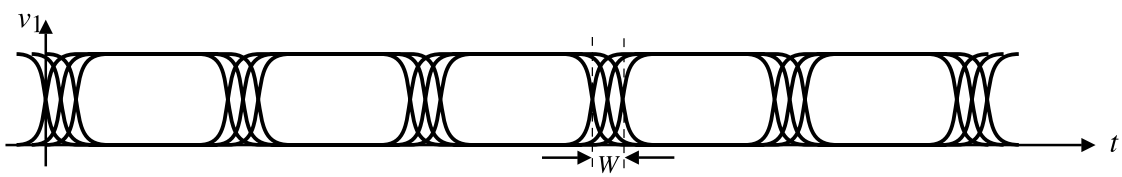
The input signal noise ratio of a pulse with phase jitter is defined as,

$$SNR_i = \frac{1}{2\,\overline{\theta_{n1}^2}}$$

where

$$\overline{\theta_{n1}^2} \approx \frac{W^2}{36}$$

where,



Phase Noise in a DPLL with a JK Flip-Flop and a PFD

The basic difference is that the JK Flip-flop and PFD are edge-triggered.

When the input signal fades ($v_1 \rightarrow 0$), the reshaped signal can stick at a distinct logic level.

Conclusion:

The noise suppression of the DPLL is about the same for all phase detectors as long as none of the edges of the reference get lost by fading. If fading occurs, the EXOR offers better noise performance.

Summary of DPLL Noise Performance:

P_s = input signal power

P_n = input noise power

B_i = input noise bandwidth

B_L = noise bandwidth $\approx \dfrac{\omega_n}{2}\left(\zeta + \dfrac{1}{4\zeta}\right)$

SNR_i = SNR of the input signal = $\dfrac{P_s}{P_n}$

SNR_L = SNR of the loop = $SNR_i \dfrac{B_i}{2B_L}$

DPLL DESIGN PROCEDURE

Design Procedure

Objective: Design K_o, K_d, ζ, and $F(s)$

Given: Phase detector and VCO

Steps:

1.) Specify $f_1(min)$, $f_1(max)$, $f_2(min)$, and $f_2(max)$.

2.) Design N unless otherwise specified.

Given: $\omega_n(min) < \omega_n < \omega_n(max)$ and $\zeta_{min} < \zeta < \zeta_{max}$

For these ranges we get approximately,

$$\frac{\omega_n(max)}{\omega_n(min)} = \sqrt{\frac{N_{max}}{N_{min}}} \quad \text{and} \quad \frac{\zeta_{max}}{\zeta_{min}} = \sqrt{\frac{N_{max}}{N_{min}}} \rightarrow N = N_{mean} = \sqrt{N_{max}N_{min}}$$

3.) Determine ζ. Typically, $\zeta \approx 0.7$.

4.) If noise is of concern, continue with the next step, otherwise go to step 12.

5.) If there are missing edges in the input signal (fading), go to step 6, otherwise go to step 7.

6.) Choose an EXOR phase detector. Continue with step 8.

$$K_d = \frac{V_{OH}\text{-}V_{OL}}{\pi}$$

Design Procedure – Continued

7.) Choose the JK Flip-flop or PFD as the phase detector.

$$K_d = \frac{V_{OH}\text{-}V_{OL}}{2\pi} \quad \text{(JK flip-flop)}$$

$$K_d = \frac{V_{OH}\text{-}V_{OL}}{4\pi} \quad \text{(PFD)}$$

8.) Specify B_L.

B_L should be chosen so that $SNR_i \frac{B_i}{2B_L} \geq 4$

$\overline{\theta_{n1}{}^2} \rightarrow SNR_i$ and $B_i \Rightarrow B_L$

- If N changes, this can create a problem because

$$B_L = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right)$$

and both ω_n and ζ vary with N.

- Need to check that $B_L(min)$ is large enough.
- If B_L is too small, then N should be increased.

Design Procedure – Continued

9.) Find K_o.

$$K_o = \frac{\omega_2(max)\text{-}\omega_2(min)}{v_f(max)\text{-}v_f(min)}$$

10.) Find ω_n given B_L and ζ.

$$\omega_n = \frac{8B_L\zeta}{1+4\zeta}$$

If N is variable, use B_L and ζ correspondingly to $N = N_{mean}$.

11.) Specify the loop filter.

Given ω_n, ζ, K_o, K_d, and N find τ_1, τ_2, and K_a (K_a>1).

Go to step 19.

12.) Continued from step 4.

Choose the PFD $\rightarrow$ $K_d = \frac{V_{OH}\text{-}V_{OL}}{4\pi}$

13.) Find K_o.

$$K_o = \frac{\omega_2(max)\text{-}\omega_2(min)}{v_f(max)\text{-}v_f(min)}$$

Design Procedure – Continued

14.) Specify the type of loop filter. Use the passive lag filter as the others offer no benefits.

15.) Determine ω_n.

a.) Fast switching (T_p). Go to step 16.

b.) DPLL does not lock out when switching from $N_o f_{ref}$ to $(N_o+1) f_{ref}$. $\therefore$ $\Delta\omega_{po} < f_{ref}$. Go to step 20.

c.) Neither the pull-in time nor the pull-out range are critical. Go to step 21.

16.) Given the maximum T_p allowed for the largest frequency step, solve for τ_1 or $\tau_1+\tau_2$.

17.) Find ω_n.

Loop filter is passive: $$\omega_n = \sqrt{\frac{K_o K_d}{N(\tau_1+\tau_2)}}$$

Active lag filter: $$\omega_n = \sqrt{\frac{K_o K_d K_a}{N\tau_1}}$$

Active PI filter: $$\omega_n = \sqrt{\frac{K_o K_d}{N\tau_1}}$$

Design Procedure – Continued

18.) Given ω_n and ζ, find τ_2.

$$\tau_2 = \frac{2\zeta}{\omega_n}$$

If the system cannot be realized (negative values of τ_1 or τ_2), modify ω_n and ζ appropriately.

19.) Given τ_1 and τ_2 (and K_a), determine the filter components.

20.) Given $\Delta\omega_{po}$ and ζ, find ω_n.

$$\omega_n \approx \frac{\Delta\omega_{po}}{11.55(\zeta+0.5)}$$

21.) Given T_L, find ω_n from $\omega_n \approx 2\pi/T_L$.

22.) Given ω_n, find τ_1 and $\tau_1+\tau_2$.

Passive lag filter: $$\tau_1+\tau_2 = \frac{K_o K_d}{N\omega_n^2}$$

Active lag filter: $$\tau_1 = \frac{K_o K_d K_a}{N\omega_n^2}$$

Active PI filter: $$\tau_1 = \frac{K_o K_d}{N\omega_n^2}$$

Go to step 18.).

Flowchart of the DPLL Design Procedure

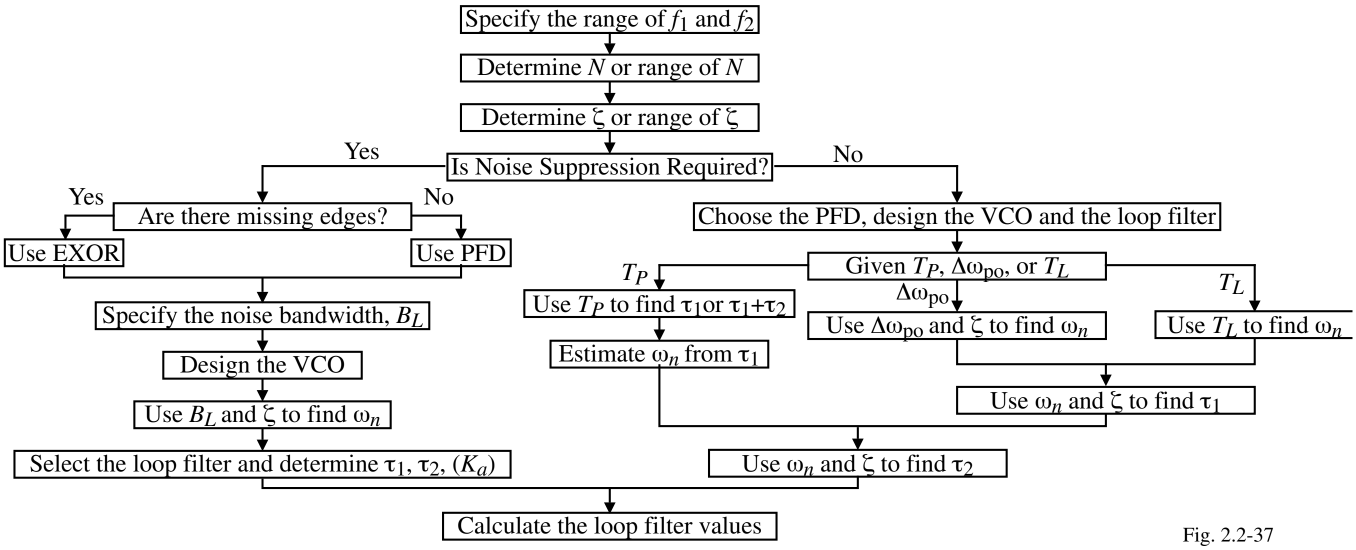


Fig. 2.2-37

Design Example – A Frequency Synthesizer Using the 74HC/HCT4076

Design a DPLL frequency synthesizer using the CMOS 74HC/HCT4076 PLL. The frequency sythesizer should be able to produce a set of frequencies in the range of 1MHz to 2MHz with a channel spacing of 10kHz. Use a PFD and a passive lag-lead filter.

Design:

1.) Determine the ranges of the input and output frequencies.

f_1 is constant at 10kHz. $f_2(min)$ = 1MHz and $f_2(max)$ = 2MHz

2.) Choose N.

$$N_{max} = \frac{2\text{MHz}}{10\text{kHz}} = 200 \quad \text{and} \quad N_{min} = \frac{1\text{MHz}}{10\text{kHz}} = 100$$

$$\therefore \quad N_{mean} = \sqrt{N_{max} \cdot N_{min}} = 141$$

3.) Find ζ. Start by choosing $\zeta = 0.7$ and find ζ_{max} and ζ_{min}.

$$\frac{\zeta_{max}}{\zeta_{max}} = \sqrt{\frac{N_{max}}{N_{min}}} = \sqrt{2} \quad \text{and} \quad \zeta = \sqrt{\zeta_{max} \cdot \zeta_{min}} = 0.7$$

$$\therefore \quad \zeta_{min}^2\sqrt{2} = 0.49 \quad \rightarrow \quad \zeta_{min} = 0.59 \quad \text{and} \quad \zeta_{max} = 0.59\sqrt{2} = 0.83$$

$\therefore$ $0.59 < \zeta < 0.83$ which is consistent with our choice of ζ.

4.) Select the PFD as the phase detector. For the 74HC/HCT4076, V_{OH} = 5V and V_{OL}=0V. This gives a $K_d = 5\text{V}/4\pi = 0.4$ V/rad.

Design Example – Continued

5.) According to the data sheet of the 74HC4046A, the VCO operates linearly in the voltage range of v_f = 1.1V to 3.9V as shown.

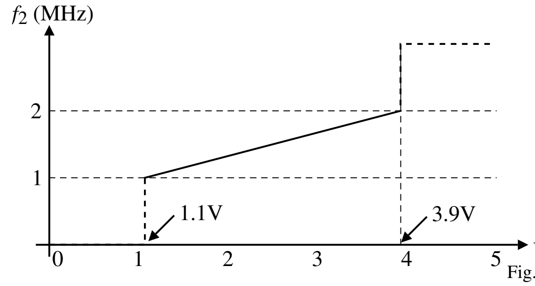


Fig. 2.2-35

$$\therefore \quad K_o = \frac{2\text{x}10^6\text{x}2\pi}{3.9-1.1} = 2.2\text{x}10^6 \text{ rads/V}\cdot\text{sec}$$

The data sheet also requires calculation of two resistors, R_1 and R_2, and a capacitor, C_1. Using the graphs from the data sheet gives,

R_1 = 47kΩ, R_2 = 130kΩ, and C_1 = 100pF.

6.) Assume the loop should lock with 1ms.

$$\therefore \quad T_L = 1\text{ms} \quad \rightarrow \quad \omega_n = 2\pi/T_L = 6280 \text{ rads/sec.}$$

7.) Using a passive loop filter we get,

$$\tau_1+\tau_2 = \frac{K_oK_d}{N\omega_n^2} = \frac{2.2\text{x}10^6\cdot 0.4}{141\cdot 6280^2} = 161\mu\text{s}$$

8.) $\tau_2 = \frac{2\zeta}{\omega_n} = \frac{2\cdot 0.7}{6280} = 223\mu\text{s}$!!! (The problem is that $\tau_1+\tau_2$ is too small)

Go back and choose T_L = 2ms → $\omega_n = 2\pi/T_L$ = 3140 rads/sec.

$$\tau_1+\tau_2 = \frac{K_oK_d}{N\omega_n^2} = \frac{2.2\text{x}10^6\cdot 0.4}{141\cdot 3140^2} = 633\mu\text{s} \text{ and } \tau_2 = \frac{2\zeta}{\omega_n} = \frac{2\cdot 0.7}{3140} = 446\mu\text{s} \rightarrow \tau_1 = 187\mu\text{s}$$

Design Problem – Continued

9.) Design the loop filter.

For optimum sideband supression, C should be large. Choose C = 0.33μF.

$$\therefore \quad R_1 = \frac{\tau_1}{C} = \frac{187\text{x}10^{-6}}{0.33\text{x}10^{-6}} = 567\Omega \quad \text{and} \quad R_2 = \frac{\tau_2}{C} = \frac{446\text{x}10^{-6}}{0.33\text{x}10^{-6}} = 1.351\Omega$$

The data sheet requires that $R_1+R_2 \geq 470\Omega$ which is satisfied.

Block diagram of the DPLL frequency synthesizer design of this example:

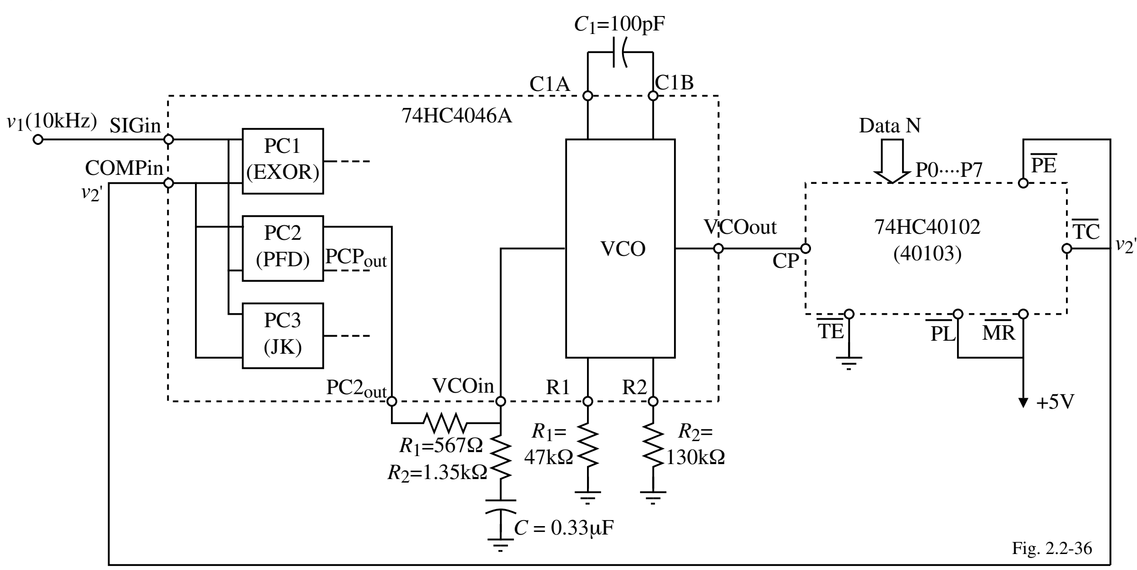


Fig. 2.2-36

Simulation of the DPLL Example

The block diagram of this example is shown below.

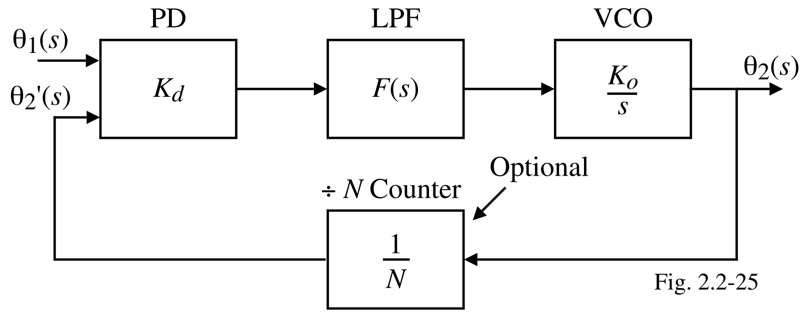


Fig. 2.2-25

The PFD-charge pump combination can be approximated as†

$$\text{“}K_dF(s)\text{”} = \frac{K_d(1+s\tau_2)}{s(\tau_1+\tau_2)}$$

Therefore, the loop gain becames

$$LG(s) = \frac{K_oK_d(1+s\tau_2)}{s^2(\tau_1+\tau_2)} = \frac{K_v\,(1+s\tau_2)}{(s+\varepsilon)^2(\tau_1+\tau_2)}$$ (the factor ε is used for simulation purposes)

For this problem,

$K_d = 0.4$V/rad., $K_o = 2.2\text{x}10^6$, $\tau_2 = 446\mu$s, and $\tau_2+\tau_2 = 633\mu$s. Also choose $\varepsilon = 0.01$.

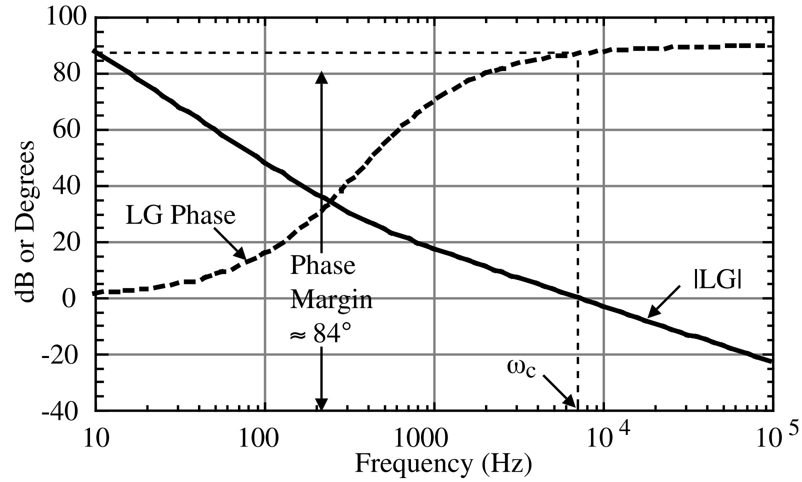
† R.E. Best, “Phase-Locked Loops – Design, Simulation, and Applications,” 4th Ed., McGraw-Hill, NY, p. 103

Simulation of the DPLL Example – Continued

PSPICE Input File

```
DPLL Design Problem-Open Loop Response - Best
VS 1 0 AC 1.0
R1 1 0 10K
* Loop bandwidth = Kv =8.8x10E5 sec.-1   Tau1=187E-6  Tau2=446E-6 N=141
ELPLL 2 0 LAPLACE {V(1)}= {8.8E+6/(S+0.01)/141*(0.446E-3*S+1)/(S+0.01)/0.633E-3}
R2 2 0 10K
*Steady state AC analysis
.AC DEC 20 10 100K
.PRINT AC VDB(2) VP(2)
.PROBE
.END
```

Simulation Results:



Note that the phase is very close to 0° and |LG|>>1 at low frequencies which is typical of type II systems.

DPLL SYSTEM SIMULATION

Examples of Case Studies using the Best Software†

PLL Parameters-

Supply voltages:

Positive supply = 5V Negative supply = -5V

Phase detector:

$V_{sat}^{+} = 4.5\text{V}$ $V_{sat}^{-} = 0.5\text{V}$

Loop filter:

$\tau_1 = 500\mu\text{s}$ $\tau_2 = 50\mu\text{s}$

Oscillator:

$K_o = 130{,}000$ rads/V·sec $V_{sat}^{+} = 4.5\text{V}$ $V_{sat}^{-} = 0.5\text{V}$

The simulation program will be used to verify the following calculated values:

$\omega_n = 17{,}347$ rads/sec.

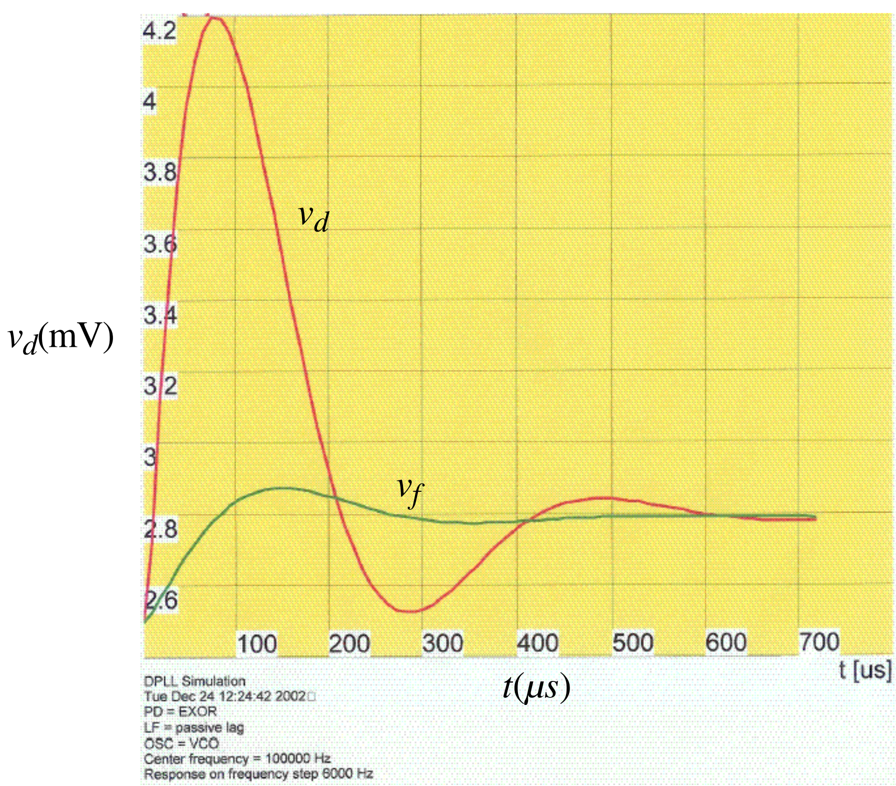
$\zeta = 0.486$

$\Delta f_{po} = 7719$ Hz

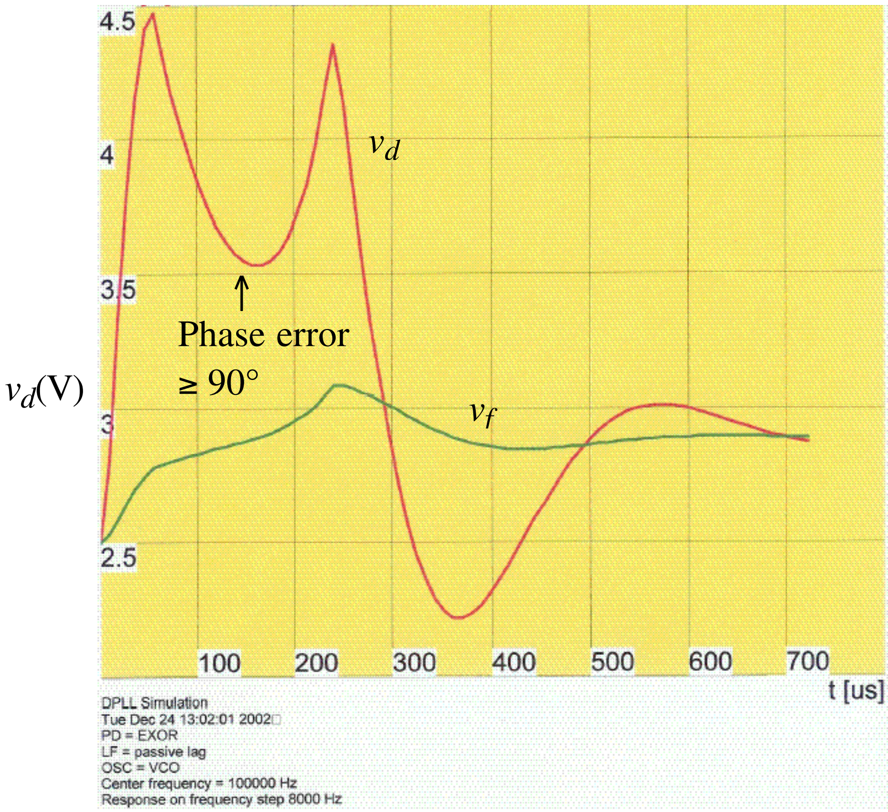
$\Delta f_p = 13{,}192$ Hz

† Roland E. Best, Phase-Locked Loops – Design, Simulation, and Applications, 4th ed., McGraw-Hill Book Co., 1999, New York, NY

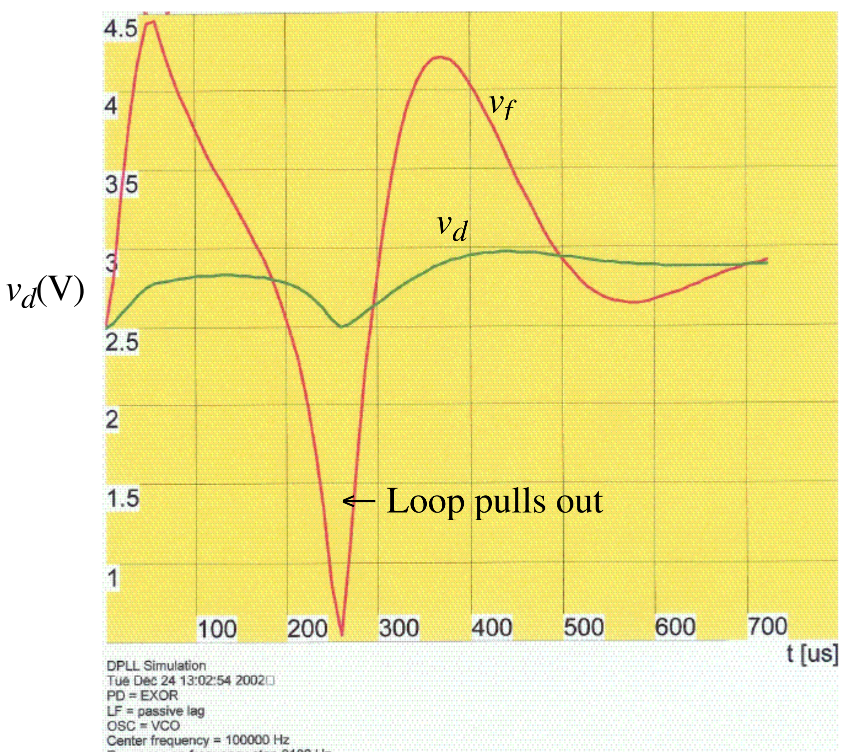
Case 1 – System Benchmark



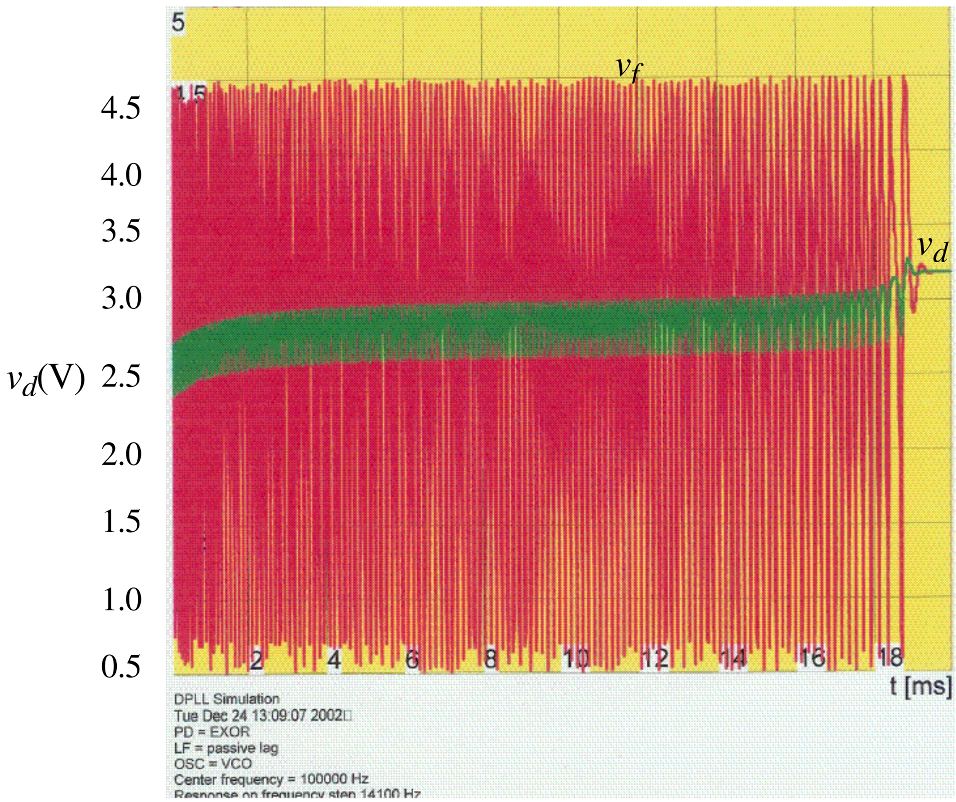
Case 2 - Δf = 8000Hz



Case 3 – Loop Just Locks Out



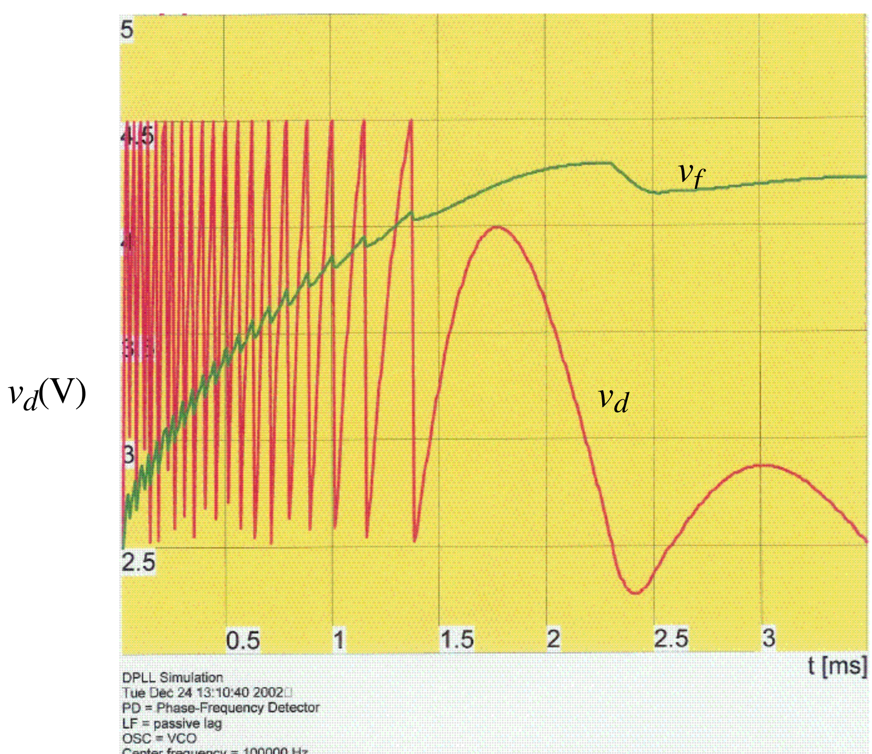
Case 4 – Pull-In Range Verification



Loop will not pull back in for df > 14,200 Hz

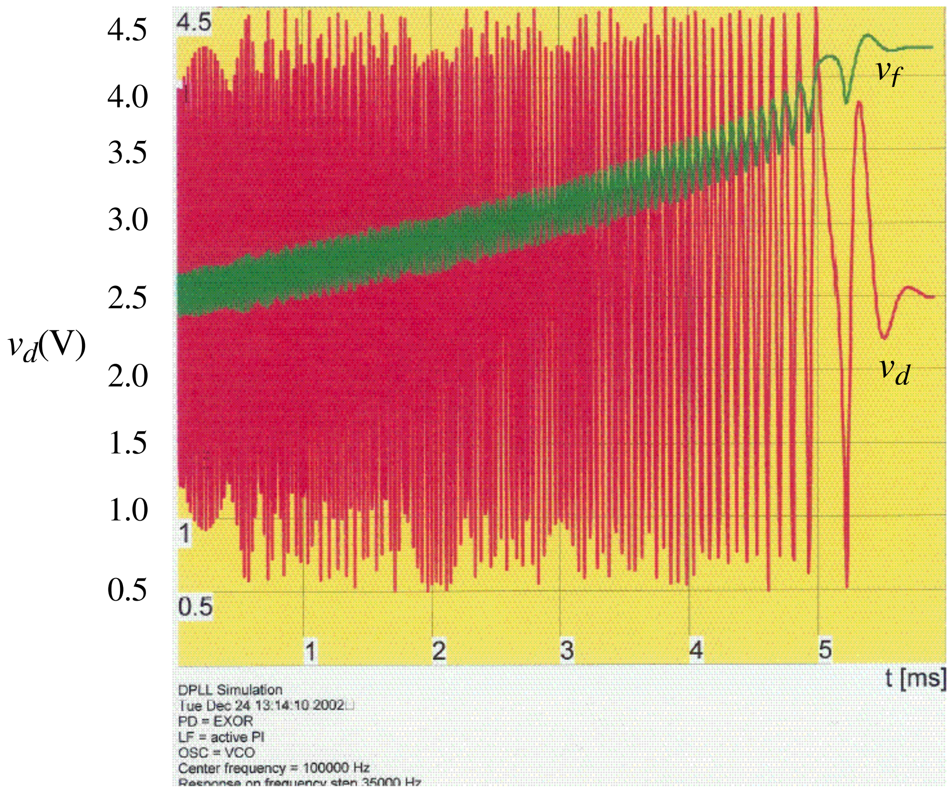
Case 5 – PFD and Illustration of a Virtually Infinite Pull-In Range

$\Delta f_p = \pm 40$kHz Δf = 35 kHz to avoid clipping of v_f.



$T_p \approx 1.5$ms

Case 6 – EXOR with Active PI Filter



$T_p \approx 5\text{ms}$

SUMMARY

- The DPLL has a digital phase detector and the remainder of the blocks are analog
- Digital phase detectors
  - EXOR Gate
  - JK Flip-Flop
  - Phase-Frequency Detector
- Charge pump – a filter implementation using currents sources and a capacitor that works with the PFD
- Charge pumps implement a pole at the origin to result in zero phase error
- The DPLL is much more compatible with IC technology and is the primary form of PLL used for frequency synthesizers