LECTURE 150 – PHASE NOISE - I

(References [4,6,9])

Objective

The objective of this presentation is to understand and model phase noise found in PLLs

Outline

- Jitter and Phase Noise in PLLs
- Spurious Sidebands in PLLs
- Linear Time Invarient Models of VCO Phase Noise
- Linear Time Varying Model of VCO Phase Noise
- Phase Noise in Differential LC Oscillators
- Jitter and Phase Noise in Ring Oscillators
- Finding the Impulse Sensitivity Function
- Amplitude Noise
- Summary

JITTER AND PHASE NOISE IN PLLs

Phase Noise in Oscillators

Causes of spectral purity degradation (phase noise):

1.) Random noise in the reference input, the PFD, loop filter and VCO (also dividers if the PLL is a frequency synthesizer)

2.) Spurious sidebands – high energy sidebands with no harmonic relationship to the generated output signal. It is systematic in origin.

Why is spectral purity important?

Phase noise can degrade the sensitivity of a receiver due to reciprocal mixing.

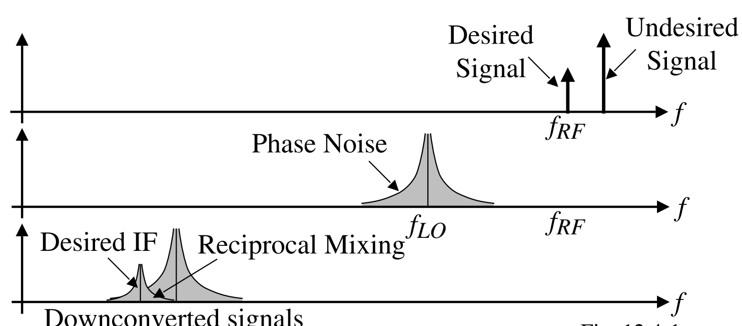

Fig. 12.4-1

Phase noise produces adjacent channel interference in the transmitter.

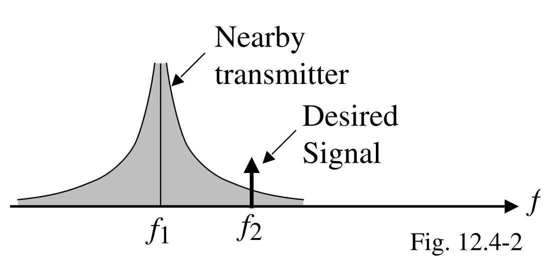

Fig. 12.4-2

Single Sideband Noise Spectral Density

An oscillator's short term instabilities can be characterized in the frequency domain in terms of the single sideband noise spectral density.

This single sideband noise spectral density is given by,

$$\mathcal{L}(\Delta\omega) = 10log\left[\frac{P_{sideband}(\omega_o+\Delta\omega,1\text{Hz})}{P_{carrier}}\right]$$

where

$P_{sideband}(\omega_o+\Delta\omega,1\text{Hz})$ = the single sideband power at a frequency offset of $\Delta\omega$ from the carrier in a measurement bandwidth of 1Hz.

$P_{carrier}$ = total power under the power spectrum.

Advantage of $\mathcal{L}(\Delta\omega)$ is its ease of measurement.

Disadvantage of $\mathcal{L}(\Delta\omega)$ is that is shows the sum of both amplitude and phase variations. It is often important to know both the amplitude and phase noise separately because they behave differently in a circuit.

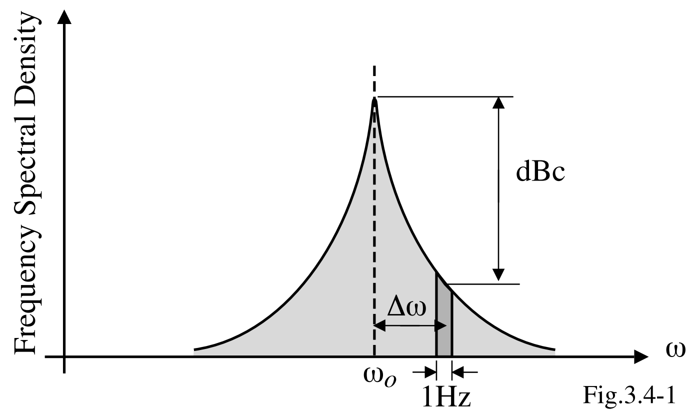

Fig.3.4-1

Signal-to-Noise Ratio (SNR) and Phase Noise

The previous definition can be used to estimate the phase noise required to achieve a desired signal-to-noise ratio.

The in-band noise relative to the carrier is found as,

$$P_{noise} = \int_{\Delta f_{min}}^{\Delta f_{max}} \mathcal{L}(\Delta f)d(\Delta f)$$

where Δf_{min} and Δf_{max} are the offsets from the center of the channel to the edges of the adjacent channel.

Assuming that the phase noise has a $1/f^2$ slope ($\mathcal{L}(\Delta f) = k/\Delta f^2$) gives

$$P_{noise} = \int_{\Delta f_{min}}^{\Delta f_{max}} \frac{k}{\Delta f^2}d(\Delta f) = \frac{k(\Delta f_{max}-\Delta f_{min})}{(\sqrt{\Delta f_{min}\Delta f_{max}})^2}$$

$$= \mathcal{L}(\sqrt{\Delta f_{min}\Delta f_{max}})\ (\Delta f_{max}-\Delta f_{min})$$

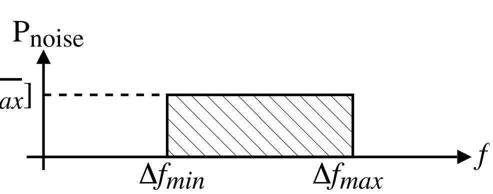

Fig. 3.4-015

This result implies that the phase noise is equivalent to a constant phase noise of

$\mathcal{L}(\sqrt{\Delta f_{min}\Delta f_{max}})$ between Δf_{min} and Δf_{max}.

The minimum *SNR* is given as

$$10log(SNR_{min}) = 10log(P_{signal})-10log(P_{interferer})-10log(P_{noise})-10log\ (\Delta f_{max}-\Delta f_{min})$$

Example

Find the maximum allowable phase noise at a 100kHz offset for a channel spacing of 200kHz and Δf_{min} = 100kHz and Δf_{max} = 300kHz if an adjacent interferer is 40dB stronger than the desired signal and for a minimum *SNR* of 20dB.

Solution

The maximum allowable phase noise can be calculated using the previous relationship as,

$$10log(P_{noise}) = -20\text{dB} - 40\text{dB} - 10\log(200\text{kHz}) = -113\text{dBc}$$

This phase noise corresponds to a frequency offset of $\sqrt{\Delta f_{min}\Delta f_{max}}$ = 173kHz

The equivalent phase noise at an offset of 100kHz assuming a $1/f^2$ slope is –108dBc.

The frequency shift from 173kHz to 100kHz is accomplished by,

$$P(f_1) = P(f_2) + 20\log_{10}(f_2/f_1) \rightarrow P(f_1) = P(f_2) + 20\log_{10}(1.73) = P(f_2) + 4.76\text{dB}$$

$$\therefore\ P(100\text{kHz}) = P(173\text{kHz}) + 4.76\text{dB} = -113\text{dBc} + 4.76\text{dB} = -108.24\text{dBc}$$

Phase Noise in VCOs

In most oscillators, $\mathcal{L}_{total}(\Delta\omega)$ is dominated by the phase noise, $\mathcal{L}_{phase}(\Delta\omega)$ which will be denoted as simply $\mathcal{L}(\Delta\omega)$.

Typical phase noise plot for a free running oscillator:

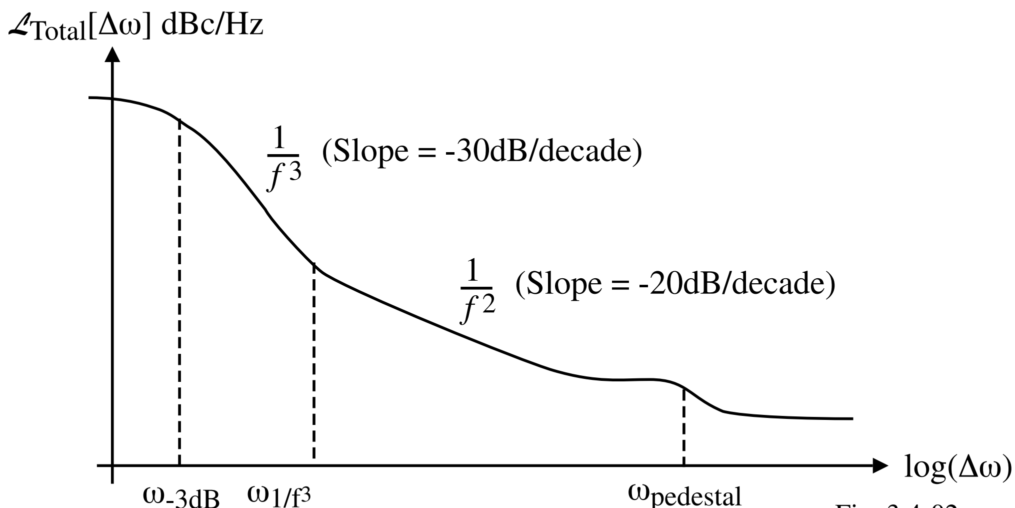

Fig. 3.4-02

The mechanisms responsible for the various regions will be discussed in the material that follows.

VCO Noise

Assume that the phase noise of the VCO is dominated by its phase noise in the $1/f^2$ region.

An equivalent model for the VCO is:

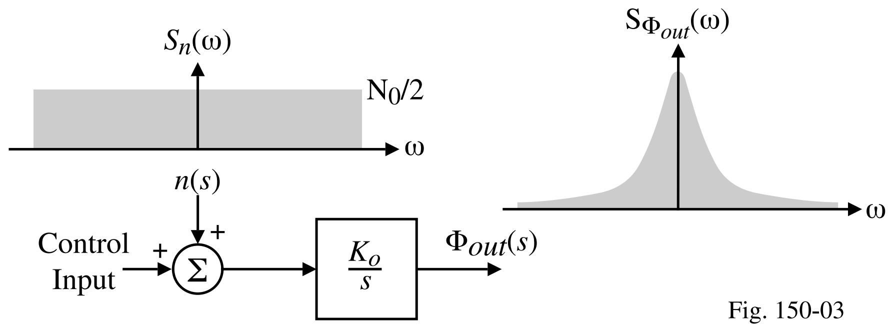

Fig. 150-03

where $n(s)$ is a white noise source with the double sideband power spectral density of $N_0/2$.

Since the VCO acts as an ideal integrator, the output power spectrum can expressed as,

$$S_{\Phi out}(\omega) = \left|\frac{K_v}{j\omega}\right|^2 S_n(\omega) = \frac{K_v{}^2 N_0/2}{\omega^2}$$

Note that $N_0/2$ is chosen in such a way that $S_{\Phi out}(\omega)$ corresponds to the phase noise of the VCO in the $1/f^2$ region.

Phase Noise in PLLs

Assuming the PLL is a linear time-invarient system, we can model the noise sources in a PLL as,

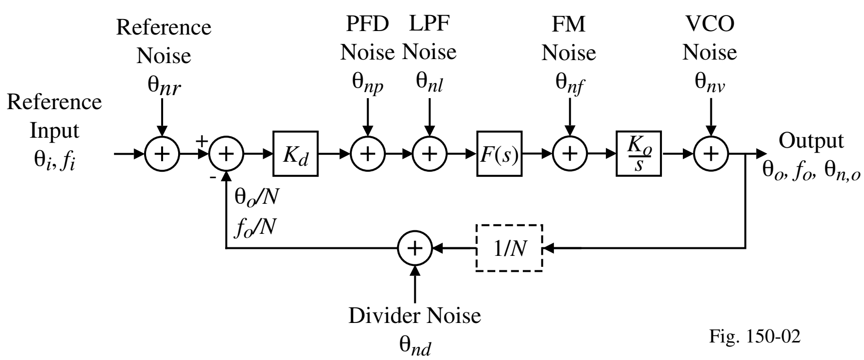

Fig. 150-02

The various transfer functions from each noise source to the output can be found as,

$$T_1(s) = \frac{\theta_{no}(s)}{\theta_{nr}(s)} = \frac{\dfrac{K_dK_oF(s)}{s}}{1 + \dfrac{K_dK_oF(s)}{Ns}} = \frac{NO(s)}{1+O(s)}$$

$$T_2(s) = \frac{\theta_{no}(s)}{\theta_{np}(s)} = \frac{\theta_{no}(s)}{\theta_{nl}(s)} = \frac{\dfrac{K_oF(s)}{s}}{1 + \dfrac{K_dK_oF(s)}{Ns}} = \frac{N}{K_d}\,\frac{O(s)}{1+O(s)}$$

Phase Noise in PLLs – Continued

$$T_3(s) = \frac{\theta_{no}(s)}{\theta_{nf}(s)} = \frac{\frac{K_o}{s}}{1+\frac{K_dK_oF(s)}{Ns}} = \frac{N}{K_dF(s)}\frac{O(s)}{1+O(s)}$$

$$T_4(s) = \frac{\theta_{no}(s)}{\theta_{nd}(s)} = \frac{\frac{K_dK_oF(s)}{s}}{1+\frac{K_dK_oF(s)}{Ns}} = \frac{NO(s)}{1+O(s)} \qquad T_5(s) = \frac{\theta_{no}(s)}{\theta_{nv}(s)} = \frac{1}{1+\frac{K_dK_oF(s)}{Ns}} = \frac{1}{1+O(s)}$$

where $O(s)$ is the open-loop gain given by $O(s) = \frac{K_dK_oF(s)}{Ns} = \frac{K_vF(s)}{Ns}$

The total output phase noise contributed by each source can be written as,

$$\theta_{no}^2 = N^2(\theta_{nr}^2+\theta_{n,eq}^2)\left(\frac{O(s)}{1+O(s)}\right)^2 + \theta_{nv}^2\left(\frac{1}{1+O(s)}\right)^2$$

where $\theta_{n,eq}^2 = \frac{1}{K_d^2}(\theta_{np}^2+\theta_{nl}^2) = \frac{1}{K_d^2F(s)^2}\theta_{nf}^2 + \theta_{nd}^2$

Note that, $\frac{O(s)}{1+O(s)} = \frac{\frac{K_dK_oF(s)}{N}}{s+\frac{K_dK_oF(s)}{N}}$ and $\frac{1}{1+O(s)} = \frac{s}{s+\frac{K_dK_oF(s)}{N}}$

Phase Noise in PLLs – Continued

Interpretation of the above results:

1.) Since $F(s)$ is either unity or low pass, the PLL functions as a low pass filter for phase noise arising in the reference signal, PFD, low-pass filter and frequency divider.

2.) However, the PLL functions as a high-pass filter for phase noise generated in the VCO.

Therefore:

1.) To minimize the output noise due to the VCO, the loop bandwidth must be as large as possible.

2.) To achieve minimum phase noise within the loop bandwidth, the in-band noise contributed by the other loop components should be kept to a minimum.

3.) However, the loop bandwidth must be less than the input reference frequency to keep the loop stable and suppress the spurs at the output due to the reference leakage signal.

Phase Noise and Jitter in First Order Loops

Use the following equivalent first order PLL model with only VCO noise:

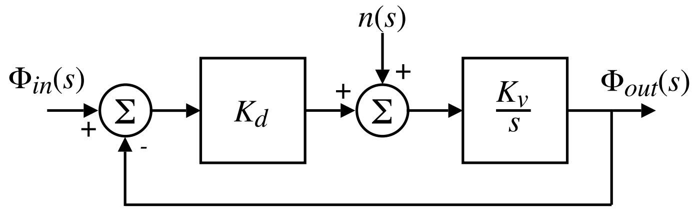

Fig. 3.4-05

In this model, the noise sources $\Phi_{in}(s)$ and $n(s)$, are the only noise sources that influence the phase noise of the output, $\Phi_{out}(s)$. $n(s)$ is white noise to model the VCO noise.

Assuming that these noise sources are uncorrelated (a reasonably good assumption) the phase noise power spectrum at the output can be calculated using superposition.

I.e.,

Total $S_{\Phi_{out}}(\omega) = S_{\Phi_{out}}(\omega)$ due to VCO + $S_{\Phi_{out}}(\omega)$ due to the Input

Output Phase Noise Spectrum with a Noiseless Input

$$\frac{\Phi_{out}(s)}{n(s)} = \frac{sK_o}{s + K_oK_d} \quad \rightarrow \quad S_{\Phi_{out}}(\omega) = \frac{N_o}{2}\,\frac{K_o^2}{\omega^2 + (K_dK_o)^2} = \frac{N_o}{2}\,\frac{K_o^2}{\omega^2 + K_v^2}$$

Illustration:

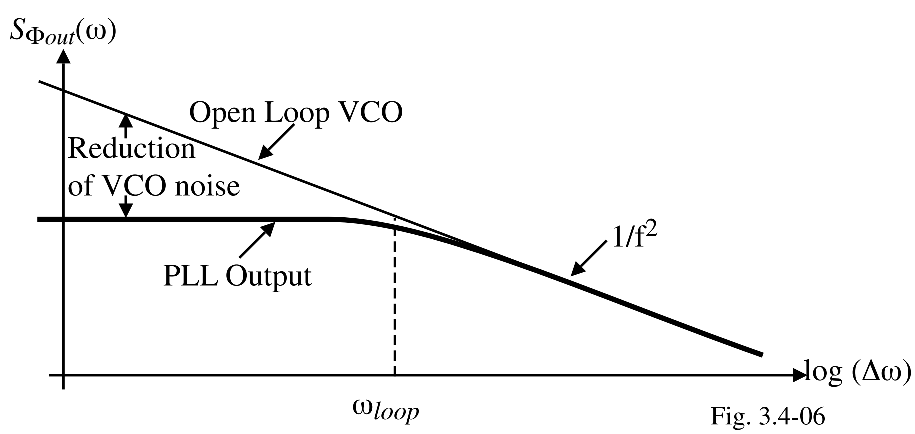

Fig. 3.4-06

For offset frequencies below ω_{loop}, the PLL can react to the noise variation of the VCO and compensate for slow random variations less than ω_{loop}. For offset frequencies above ω_{loop}, the PLL is unable to react fast enough to fast random changes in the VCO output and they appear directly on the output.

Jitter in Oscillators

Illustration of jitter:

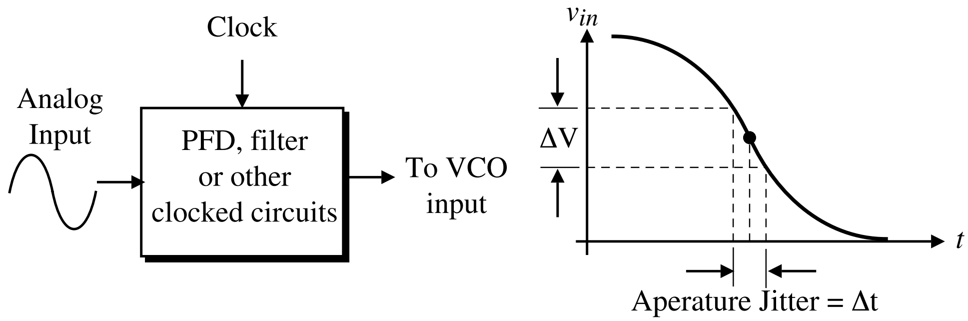

Fig.12.4-2A

If we assume that $v_{in}(t) = V_p sin\omega t$, then the maximum slope is equal to ωV_p.

Therefore, the value of ΔV is given as

$$\Delta V = \left|\frac{dv_{in}}{dt}\right| \Delta t = \omega V_p \Delta t \ .$$

The rms value of this noise is given as

$$\Delta V(\text{rms}) = \left|\frac{dv_{in}}{dt}\right| \Delta t = \frac{\omega V_p \Delta t}{2\sqrt{2}} \ .$$

This ΔV(rms) will lead to an uncertainty in the output frequency when applied on top of the VCO input.

Jitter in Oscillators - Continued

Comparator Noise:

Noise of a comparator is modeled as if the comparator were biased in the transition region.

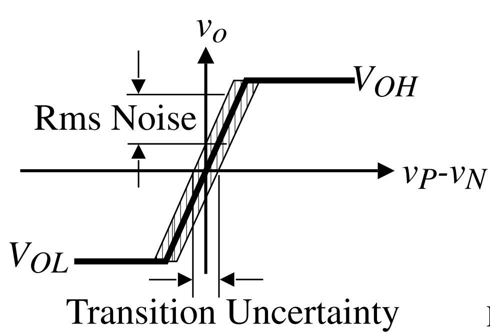

Fig. 8.1-8

Noise leads to an uncertainty in the transition region that causes jitter or phase noise.

Timing Jitter

Clock jitter increases with the time delay between the reference and the observed transition as shown below.

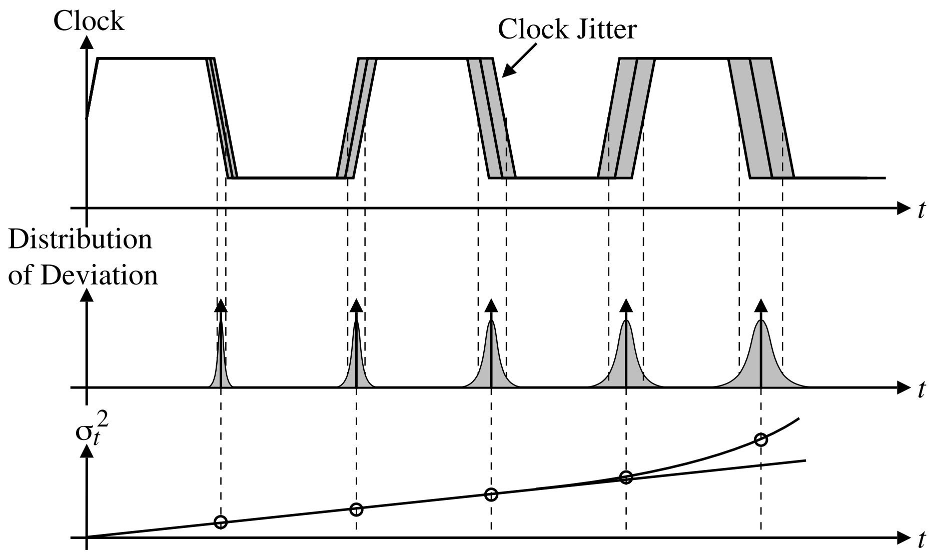

Fig. 3.4-07

Note that the variance, σ_t^2 , will increase as the time between reference and the observed transition increases. This is called “jitter accumulation”.

Jitter Accumulation

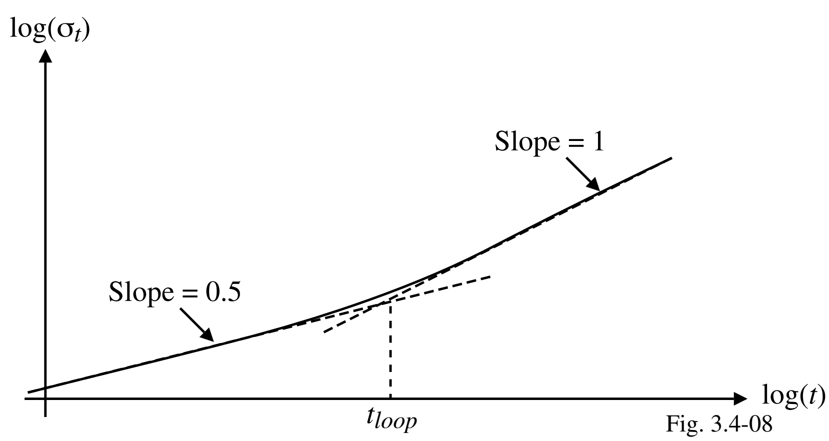

Fig. 3.4-08

Various regions of behavior:

1.) Short time-

$$\sigma_t \propto \sqrt{t}$$

2.) Long time-

$$\sigma_t \propto t$$

Relationship between Jitter and Phase Noise

Start by observing that jitter is the standard deviation of the timing uncertainty,

$$\sigma_\tau^2 = \frac{1}{\omega_o^2} E\{[\phi(t+\tau) - \phi(t)]^2\} = \frac{E[\phi(t)^2]}{\omega_o^2} + \frac{E[\phi(t+\tau)]^2}{\omega_o^2} - \frac{2E[\phi(t)\phi(t+\tau)]^2}{\omega_o^2}$$

where $E\{x\}$ is the expected value of x.

Next, the autocorrelation function of $\phi(t)$ is expressed as

$$R_\phi(\tau) = E\{\phi(t)\phi(t+\tau)\} \quad \rightarrow \quad \sigma_\tau^2 = \frac{2}{\omega_o^2}[R_\phi(0) - R_\phi(\tau)]$$

Using Khinchin's theorem†,

$$R_\phi(\tau) = \frac{1}{2\pi}\int_{-\infty}^{\infty} S_\phi(\omega)e^{j\omega\tau}d\omega \quad \rightarrow \quad \sigma_\tau^2 = \frac{2}{\omega_o^2}\left[\frac{1}{2\pi}\int_{-\infty}^{\infty} S_\phi(\omega)d\omega - \frac{1}{2\pi}\int_{-\infty}^{\infty} S_\phi(\omega)e^{j\omega\tau}d\omega\right]$$

$$\therefore \quad \sigma_\tau^2 = \frac{1}{\pi\omega_o^2}\int_{-\infty}^{\infty} S_\phi(\omega)[1-e^{j\omega\tau}]d\omega = \frac{1}{\pi\omega_o^2}\int_{-\infty}^{\infty} S_\phi(\omega)\sin^2\left(\frac{\omega\tau}{2}\right)d\omega$$

Therefore, knowing the phase noise, $S_\phi(\omega)$, one can find the jitter noise, σ_τ^2.

† W.A. Gardner, *Introduction to Random Processes*, McGraw-Hill Book Co., New York, 1990.

Jitter in First Order Loops with a Noiseless Input

In general, for a first-order PLL with a loop bandwidth of ω_{loop}, we can use the previous relationship to find the timing jitter as,

$$\sigma_t^2 = \frac{2\pi^2 NK_o^2}{\omega_o^2}\frac{1}{\omega_{loop}}(1 - e^{-\omega_{loop}t})$$

where ω_o is center frequency of the VCO. If $t < t_{loop}$, then

$$\sigma_t^2 \approx \frac{2\pi^2 NK_o^2}{\omega_o^2} t$$

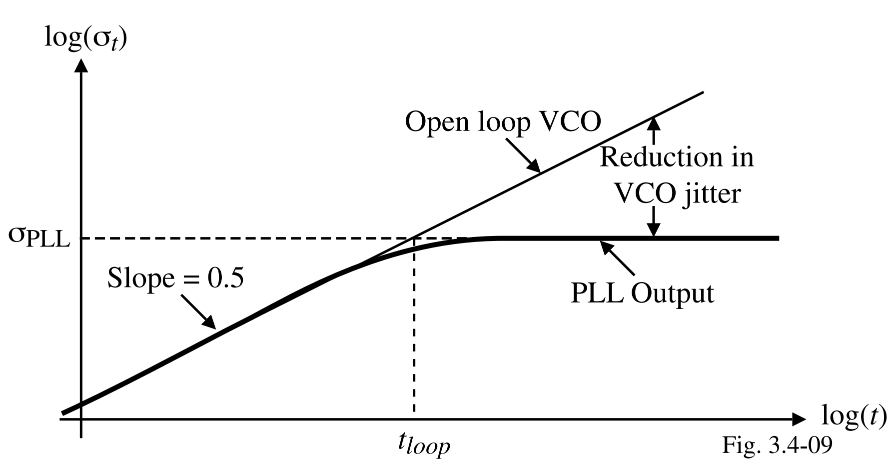

Fig. 3.4-09

Output Phase Noise Spectrum with a Noiseless VCO

In this case, the noise will be due to phase variations in the input reference frequency. The transfer function from the input to output based on the simple first-order PLL model is

$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{K_oK_d}{s + K_oK_d}$$

Assuming input oscillator phase noise in the $1/f^2$ region, we can express its power spectrum as,

$$S_{\Phi in}(\omega) = \frac{\alpha}{\omega^2} \quad \rightarrow \quad S_{\Phi out}(\omega) = \frac{\alpha}{\omega^2}\frac{(K_oK_d)^2}{\omega^2 + (K_dK_o)^2} = \frac{\alpha}{\omega^2}\frac{K_v{}^2}{\omega^2 + K_v{}^2}$$

Illustration:

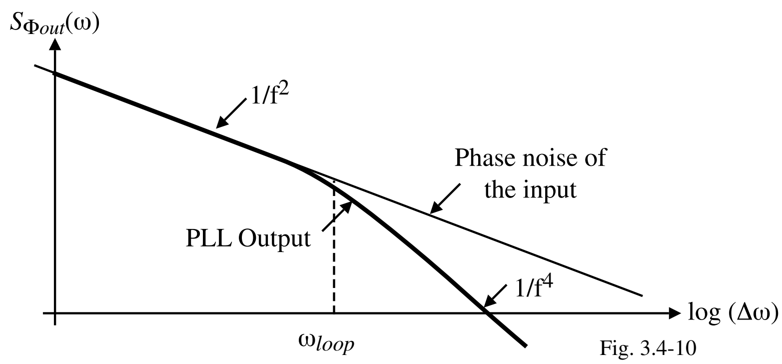

Fig. 3.4-10

Output Timing Jitter with a Noiseless VCO

Corresponding time domain behavior.

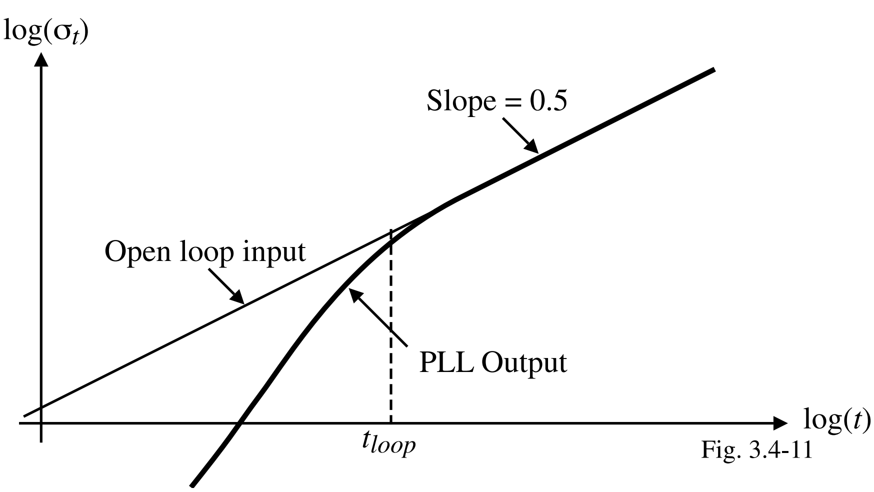

Fig. 3.4-11

Output Phase Noise Spectrum with a Low Noise Input

This circumstance is typical of a microprocessor clock distribution scheme or frequency synthesis.

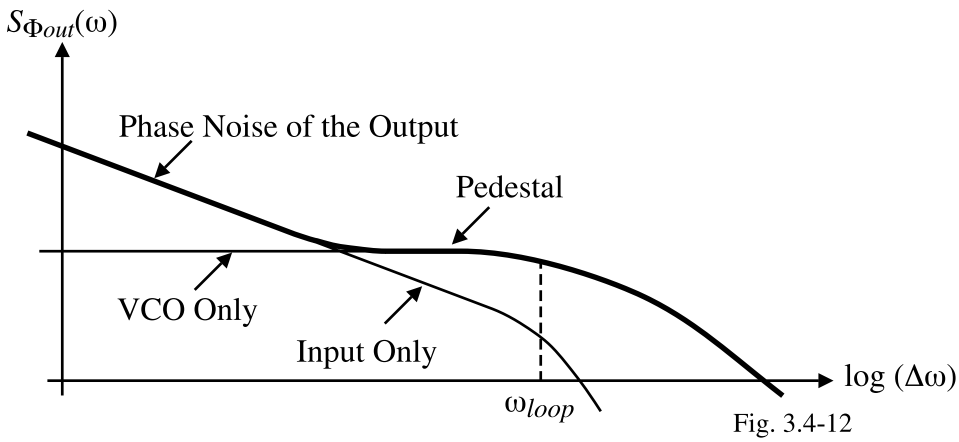

Fig. 3.4-12

The phase noise is dominated by the input phase noise for small offset frequencies and by the VCO noise for large offset frequencies.

The phase noise pedestal shown is common in frequency synthesizers.

Output Timing Jitter with a Low Noise Input

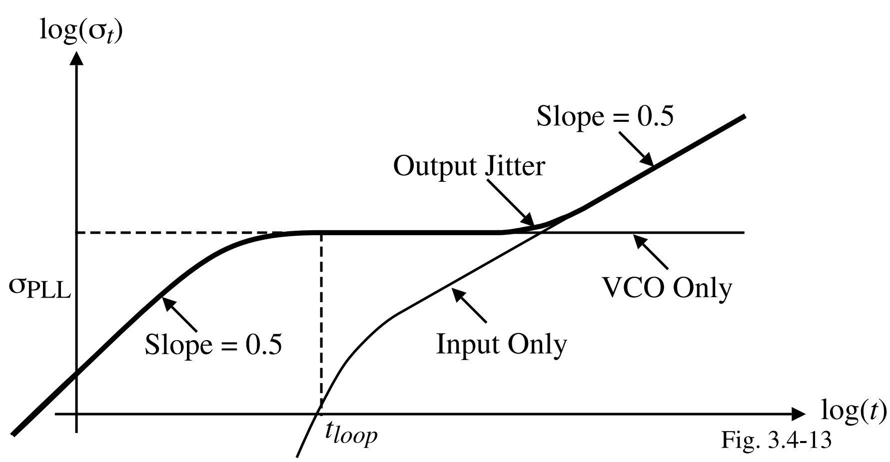

Fig. 3.4-13

Note that if the input signal has better frequency stability compared to the internal time base used in the phase noise/jitter measurement system, phase noise at low offsets (jitter at large delay times) will be dominated by the phase noise (jitter) of the measurement system.

Output Phase Noise Spectrum with a Input Noiser than the VCO

This is typical of clock recovery applications.

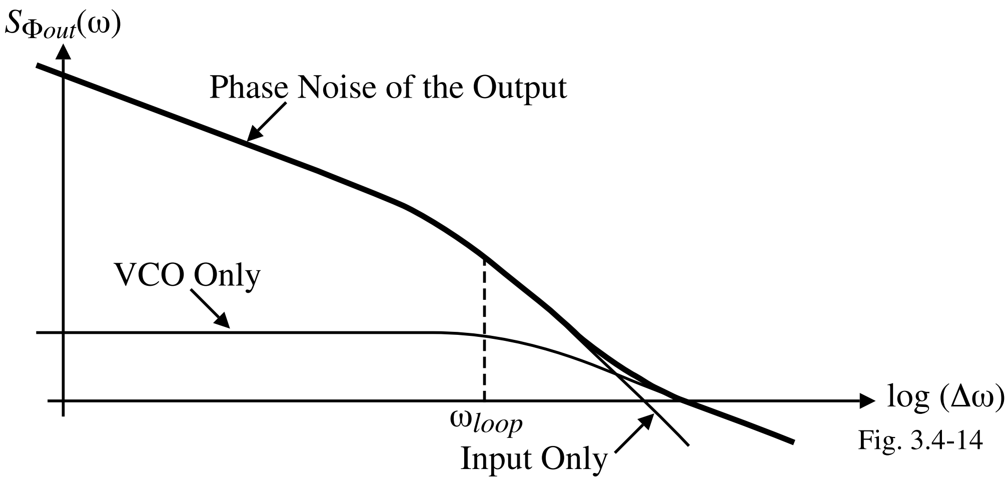

Fig. 3.4-14

Output Timing Jitter with a Input Noiser than the VCO

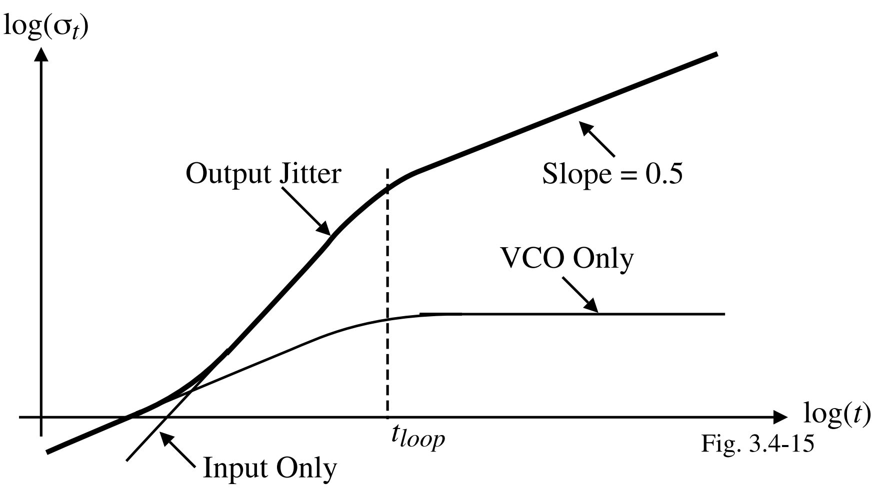

Fig. 3.4-15

Second-Order Charge Pump PLLs

Typical charge pump PFD:

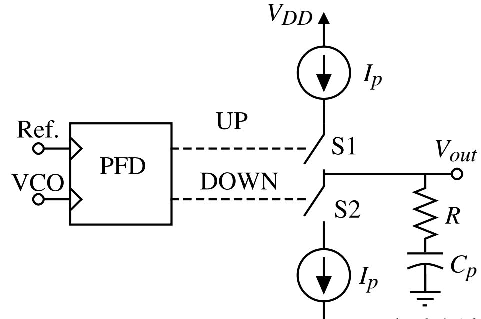

Fig. 3.4-16

The filter transfer function that corresponds to the charge pump PFD using a compensation zero is,

$$K_dF(s) = \frac{I_p}{2\pi C_p}\frac{s\tau_z + 1}{s}$$

Putting this into,

$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{K_dF(s)K_o}{s + K_dF(s)K_o} \quad \rightarrow \quad \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{s\tau_z + 1}{\dfrac{s^2}{\left(\dfrac{K_oI_p}{2\pi C_p}\right)} + s\tau_z + 1}$$

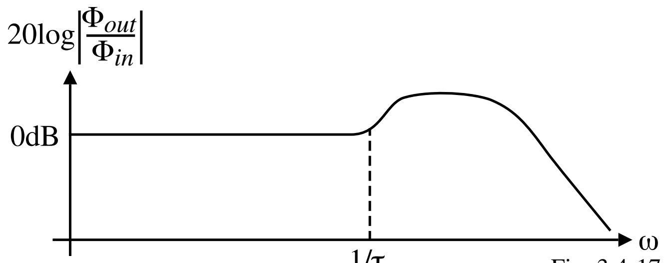

Fig. 3.4-17

Note the zero steady state error typical of charge pumps.

Output Phase Noise of a Charge Pump PLL with a Low Noise Input

Consider the case of a charge pump with a compensation zero that is described by the phase function,

$$\frac{\Phi_{out}(s)}{n(s)} = \frac{2\pi C_p}{I_p}\frac{s}{\dfrac{s^2}{\left(\dfrac{K_oI_p}{2\pi C_p}\right)} + s\tau_z + 1} \quad \rightarrow \quad S_{\Phi out}(\omega) = \frac{N_o}{2}\frac{\omega^2}{\left[1 + \left(\dfrac{\omega^2}{\dfrac{K_oI_p}{2\pi C_p}}\right)^2\right]^2 + (\tau_z\omega)^2}$$

Output phase noise:

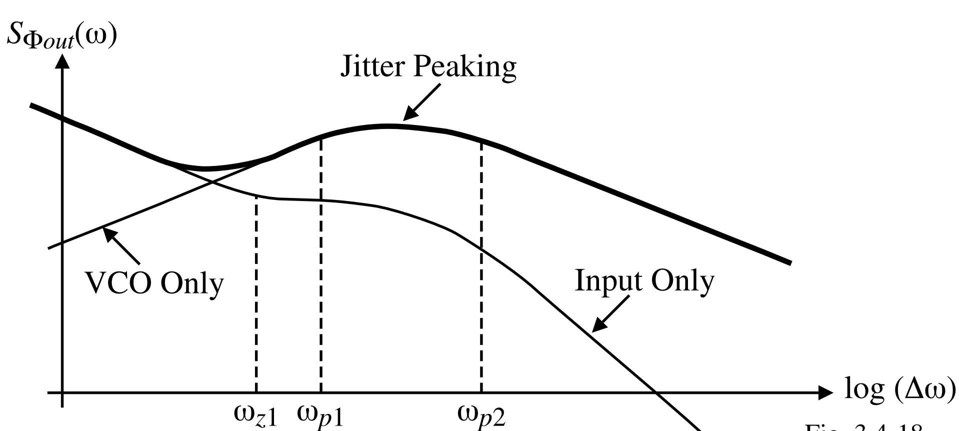

Fig. 3.4-18

A PLL with A Frequency Divider in the Feedback Path

Block diagram:

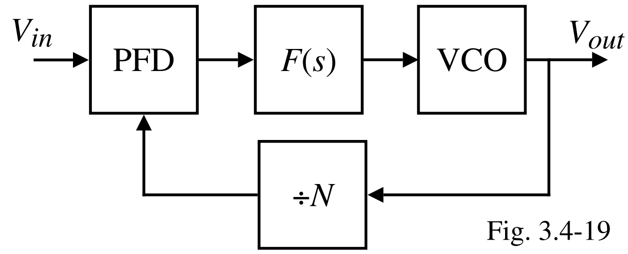

Fig. 3.4-19

The closed-loop transfer function for a charge pump PLL with a divide by N in the feedback path is found to be,

$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{s\tau_z + 1}{\frac{s^2}{K} + \frac{s\tau_z + 1}{N}}$$

Note, when $s \rightarrow 0$, the transfer function reduces to N whereas the transfer function without the divider reduces to 1. Thus the low frequency input phase variations get multiplied by N. For $s \rightarrow \infty$, both transfer functions reduce to $K\tau_z/s$.

Output phase noise →

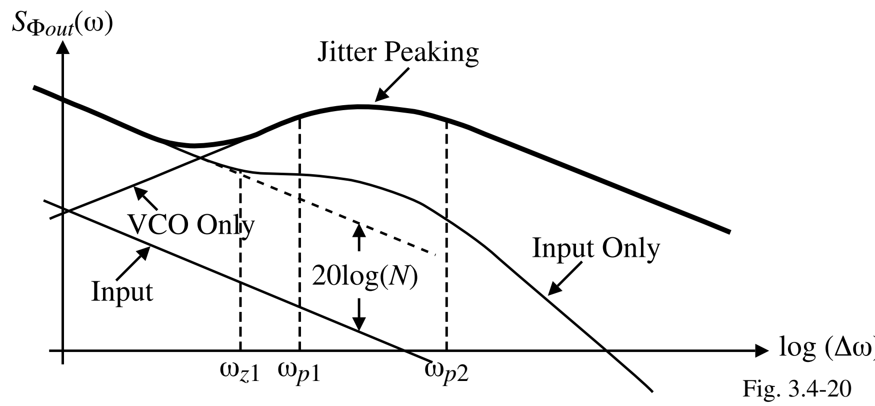

Fig. 3.4-20

SPURIOUS SIDEBANDS IN PLLs

Spurious Sidebands In Oscillators

Spurious sidebands are the undesired systematic variation of the oscillator frequency as a function of time.

These spurious sidebands appear as unwanted sidebands close to the carrier signal and are significantly higher than the noise floor.

The major source spurious sidebands is the reference input frequency and its harmonics that couple through the phase/frequency detector (recall that the phase/frequency detectors are highly nonlinear).

The amplitude of the output spurs can be calculated using the theory of FM modulation:

$$\text{Output amplitude of spurs} = 20\log\left(\frac{\Delta f_{rms}}{f_m\sqrt{2}}\right)$$

where

$\Delta f_{rms} = K_v V_{rms}$

K_v = PLL bandwidth

V_{rms} = amplitude level of the harmonics of the reference frequency

f_m = frequency deviation from the carrier and modulating frequency.

To reduce the spurious sidebands, a higher-order loop filter can be used to suppress the reference frequency allowing a much smaller loop bandwidth to be used.

Spurs From the Phase Detector

We have seen that one source of spurs comes from the modulation (AM, PM or FM) of the VCO. The phase detector can also generate spurious responses.

How does the phase detector generate spurs?

Answer - The spurs from the PD pass through the filter and if they are strong enough, they will phase modulate the VCO and generate undesired sidetones.

Consider the following phase detector:

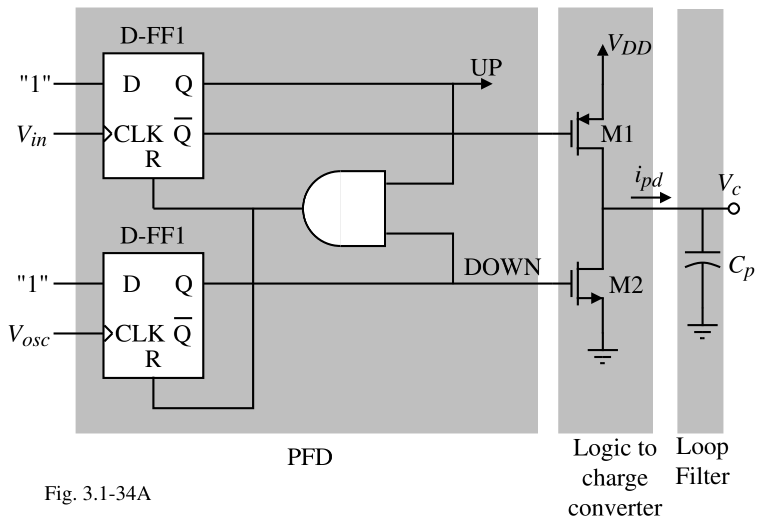

Fig. 3.1-34A

Spurs due to PDs – Continued

Assume the steady-state phase error, θ_e, is positive and fixed which means that V_{in} is always on for a fixed period of time before V_{osc} is on. The duty cycle is

$$d = \frac{\theta_e}{2\pi}T \approx 0.1\%$$

for typical technology and transistor sizes where $T = 1/f_{in}$.

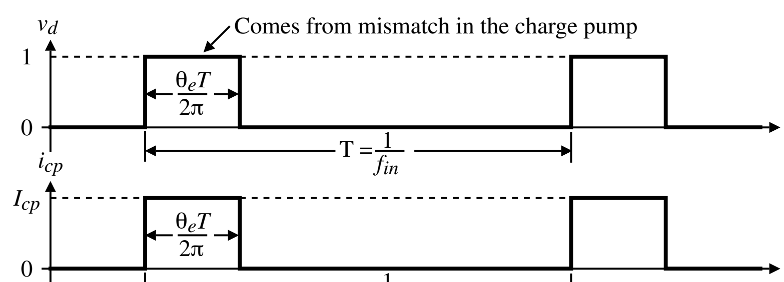

Fig. 3.1-35A

The Fourier series expansion of $i_{cp}(t)$ is given as,

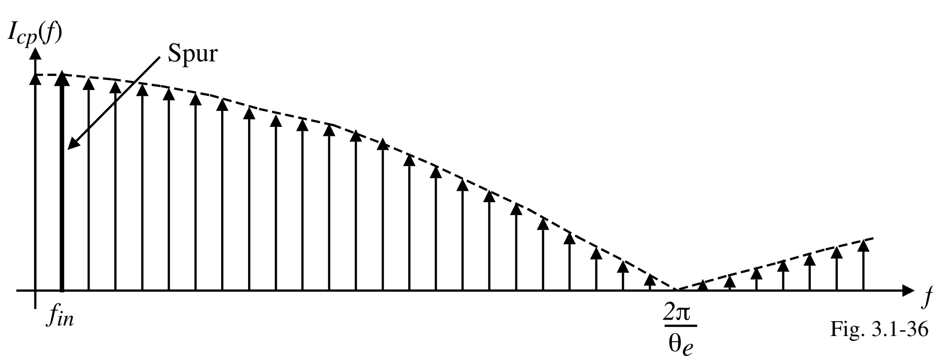

Fig. 3.1-36

The frequency component closest to the origin is the most damaging.

$$\therefore \quad i_{spur} \approx \overline{i_{cp}} \sin\omega_{in}t = (\theta_e/2\pi)I_{cp} \sin\omega_{in}t = d\, I_{cp} \sin\omega_{in}t$$

Spurs due to PDs – Continued

The spur can be expressed in the phase domain as

$$\theta_{spur}(t) = d(2\pi)\sin\omega_{in}t$$

Now,

$$\frac{i_{spur}}{\theta_{spur}} = \frac{d\, I_{cp} \sin\omega_{in}t}{d(2\pi)\sin\omega_{in}t} = \frac{I_{cp}}{2\pi}$$

but,

$$I_{cp} = 2\pi\, K_d \quad \Rightarrow \quad \frac{i_{spur}}{\theta_{spur}} = K_d$$

The sinusoidal phase change at the output of the VCO, θ_o, can be expressed as

$$\theta_o = H \frac{i_{spur}}{K_d}$$

where H is the transfer function from the phase detector to the VCO output.

If the VCO output is assumed to be $v_o(t) = 0.5A_c \sin\omega_o t$, then if the phase modulation of θ_o is narrowband modulation (which is the case when θ_{spur} and i_{spur} are small), then the VCO output will consist of the original frequency at f_o and two new sidetones at $f_o \pm f_{in}$.

$$\therefore \quad v_o(t) = 0.5A_c \sin\omega_o t + 0.5\theta_o A_c \sin(\omega_o+\omega_{in})t + 0.5\theta_o A_c \sin(\omega_o-\omega_{in})t$$

Thus, $$\frac{\text{Spur Amplitude}}{\text{Carrier Amplitude}} = \theta_o = H \frac{i_{spur}}{K_d}$$

Example

Suppose the PLL is given as shown. H can be found as,

$$H(s) = \frac{K_v F(s)}{1 + \dfrac{K_v F(s)}{sN}} \quad \text{where } K_v = K_d K_o$$

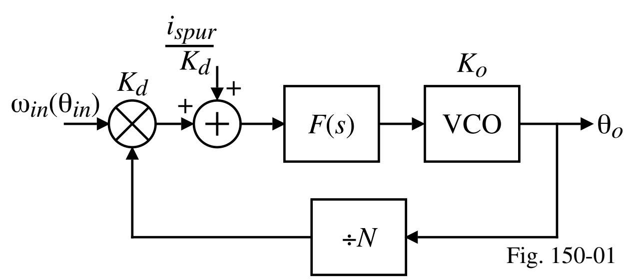

Fig. 150-01

From the previous slide, we can write,

$$\text{Spur (dBc)} = 10\log_{10}\left(\frac{\text{Spur Power}}{\text{Carrier Power}}\right) = 10\log_{10}\theta_o^2 = 20\log_{10}\theta_o = 20\log_{10}\left(H \frac{i_{spur}}{K_d}\right)$$

If $F(s) = \dfrac{s+z_1}{s(s+p_3)}$, then at low frequencies (spur offsets) $|H| \approx \dfrac{NK_v p_3}{\omega_{spur}^2}$.

Thus,

$$\text{Spur (dBc)} = 20\log_{10}\left(\left|\frac{NK_v p_3}{\omega_{spur}^2}\times\frac{\text{Amplitude of } i_{spur}}{K_d}\right|\right) = 20\log_{10}\left(\left|\frac{NK_v p_3}{\omega_{spur}^2}\times\frac{d\cdot I_{cp}}{I_{cp}/2\pi}\right|\right)$$

$$\text{Spur (dBc)} = 20\log_{10}\left(\left|\frac{NK_v p_3 2\pi d}{\omega_{spur}^2}\right|\right)$$

If $N = 1099$, $p_3 = 972$Krads/s, $K_v = 324$ Krads/s, $d = 0.001$, and $f_{spur} = f_{in} = 1.728$MHz,

$$\text{Spur (dBc)} = 20\log_{10}\left(\left|\frac{1099\cdot 324\text{K}\cdot 972\text{K}}{2\pi(1.728\text{M})^2}\,0.001\right|\right) = -34.7 \text{ dBc}$$

Methods of Reducing Spurious Sidebands

- Use a higher order loop filter to suppress the reference frequency with the loop bandwidth smaller than the reference frequency
- Reduce the leakage current that occurs due to the charge pump, loop filter components, varactor diodes and other components
- Use a fully differential configuration
- Use a higher reference frequency (as done in fractional-N synthesis techniques)

(To be continued)

