LECTURE 180 –FREQUENCY SYNTHESIZERS – GSM EXAMPLE

(References [3,11])

Specifications

Frequency range: 890-960MHz Switching time: ≤ 800μs Close-in rms noise: ≤ 2°

Phase noise @ 200kHz: -110dBc Reference spurs: < -71dBc P_{diss}: ≤ 50mW

Block Diagram of the Design:

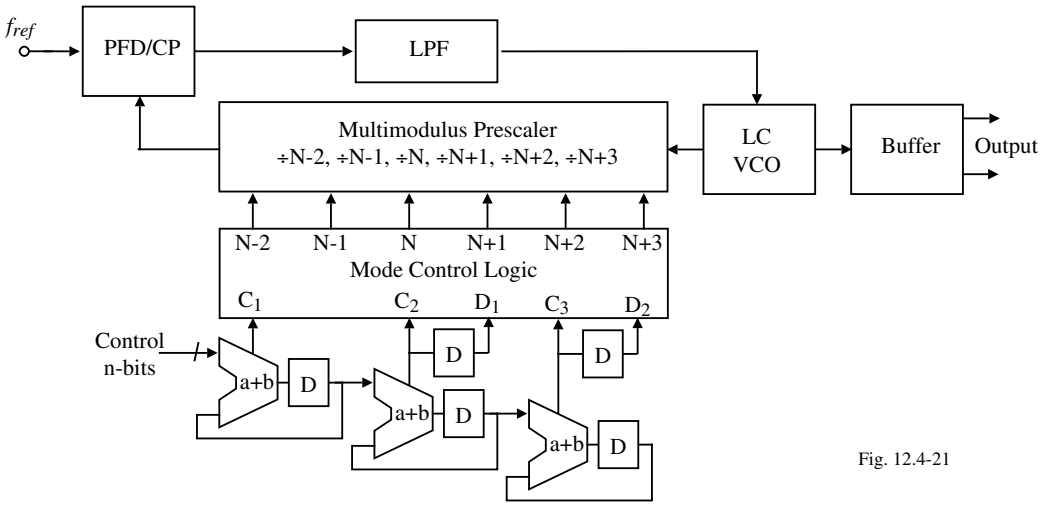


Fig. 12.4-21

Technology used is 0.5μm CMOS with 3 metal layers.

Design of the PFD

Illustration of (a.) symbol, (b.) state-diagram:

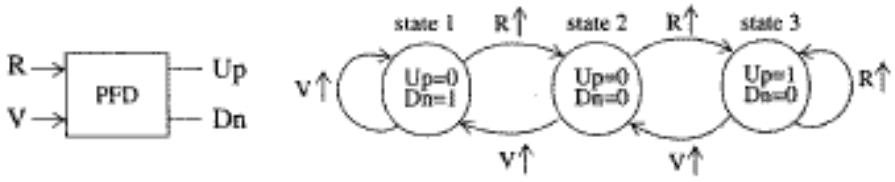
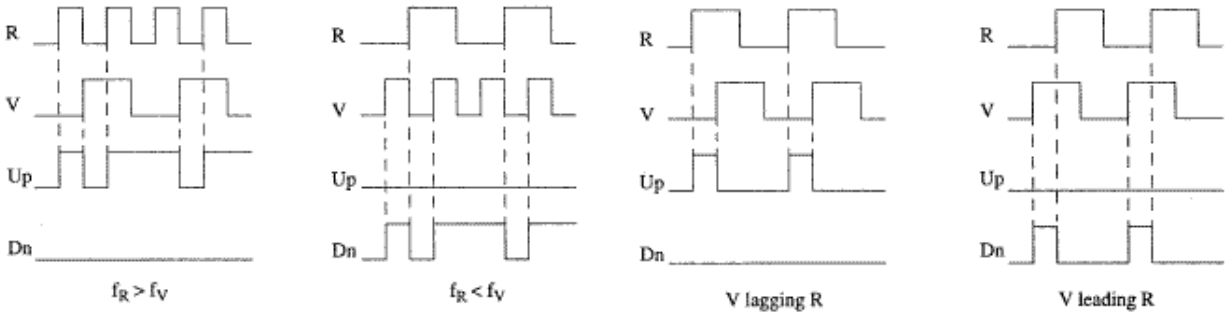
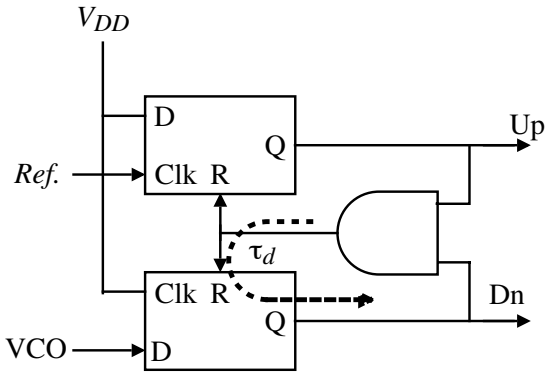


Illustration of the response with $f_r > f_o$, $f_r < f_o$, V lagging R, and R lagging V.

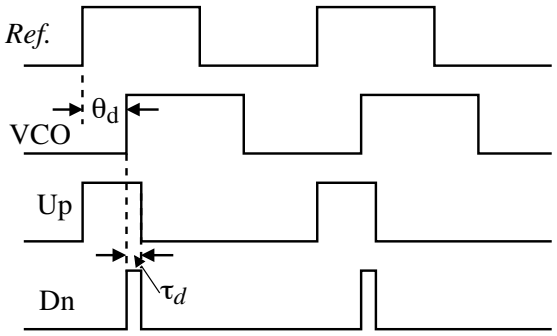


PFD Implementation and Response

PFD consists of two edge-triggered, resettable D flipflops with their D inputs connected to logical 1.



PFD Implementation



PFD Response Fig. 4.3-31

Note that the outputs Up and Dn are simultaneously high for a duration of τ_d equal to the total delay through the AND gate and the reset path of the D flipflop.

A dead zone exists when the phase error is nearly zero. Neither the Up or Dn signal reaches the logic 1 and the charge pump is disconnected from the capacitor. In this case, the high impedance node of the charge pump will leak off until the phase difference of the inputs is large enough for the PFD to exit the dead zone and turn on the charge pump to correct this error.

A PFD without a Dead Zone

Concept:

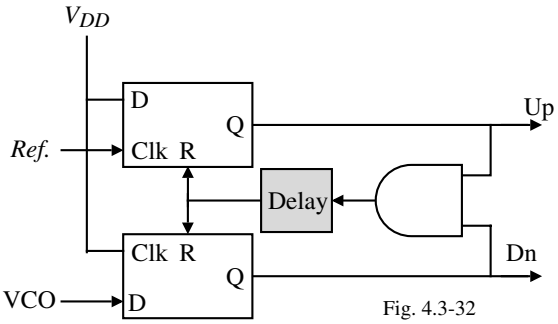


Fig. 4.3-32

Modified D flipflop:

- Number of transistors in the signal path has been reduced.
- Extra gates have been added to increase the reset delay.

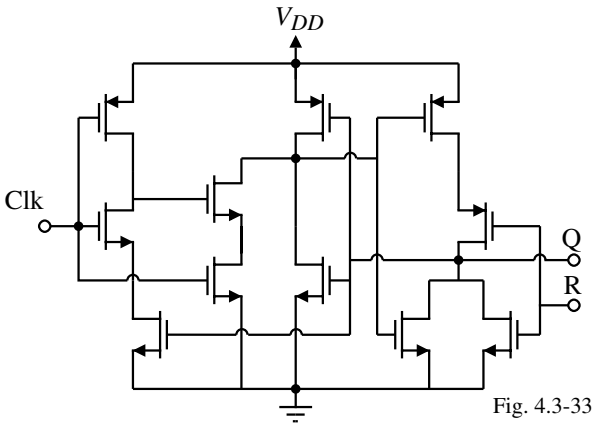
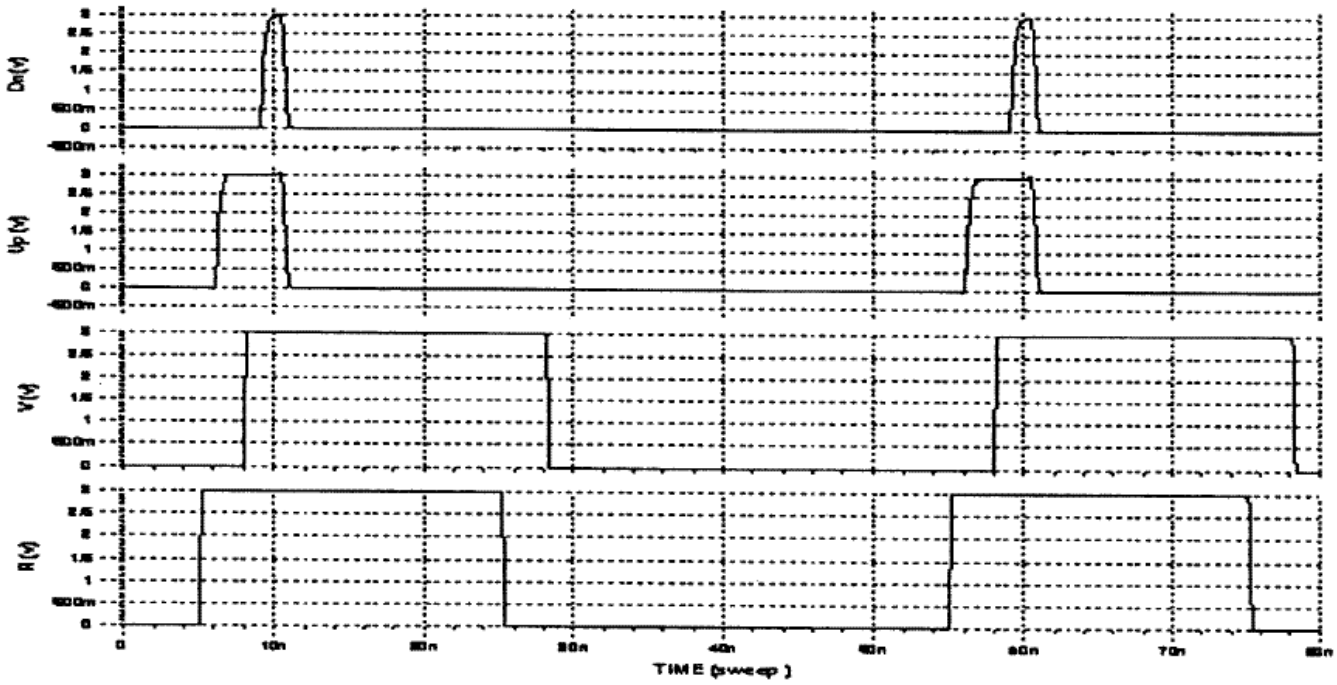


Fig. 4.3-33

Simulated PFD Waveforms

The input R leads the input V by 3ns at $f = 20$ MHz.



Charge Pump

One possible differential charge pump.

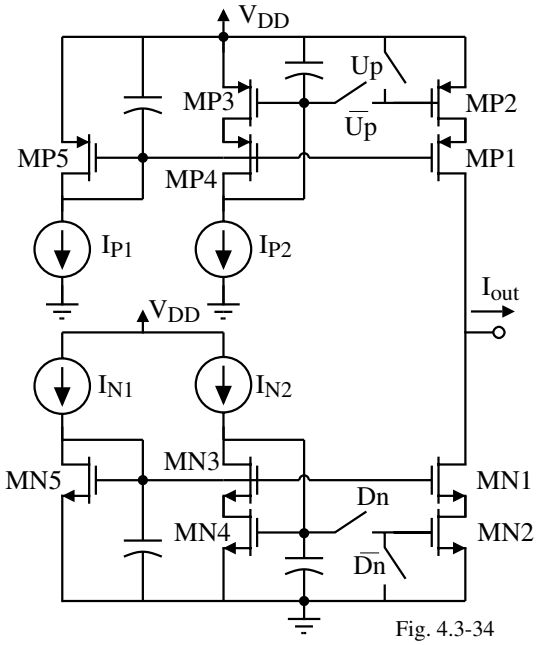


Fig. 4.3-34

Comments:

- Large transistors are needed for the Up and $\overline{\text{Up}}$ and Dn and $\overline{\text{Dn}}$
- Larger switches introduce more parasitic capacitance decreasing the response speed and introducing a dead zone.

Thus, tradeoffs between response speed and matching are needed.

A Second Charge-Pump

Uses current steering in the source-coupled pairs, MN1-MN2 and MP1 and MP2.

Current sinks and sources are 300μA.

This charge pump does not produce current spikes resulting from charge sharing which in turn minimizes the spurs in the synthesized RF signal.

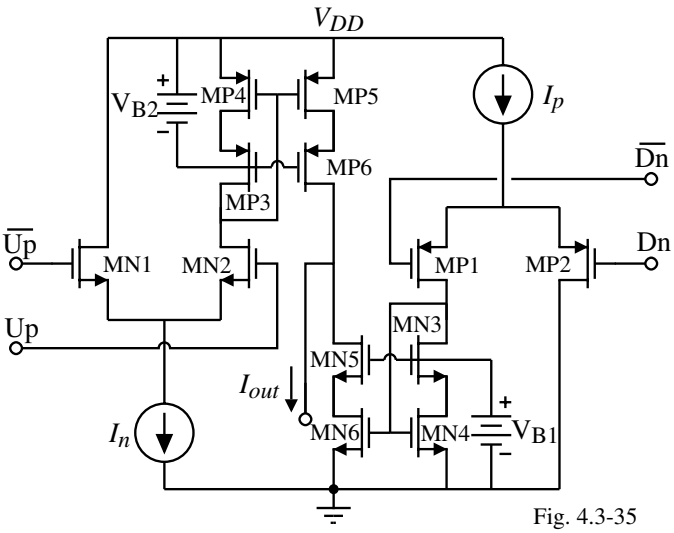
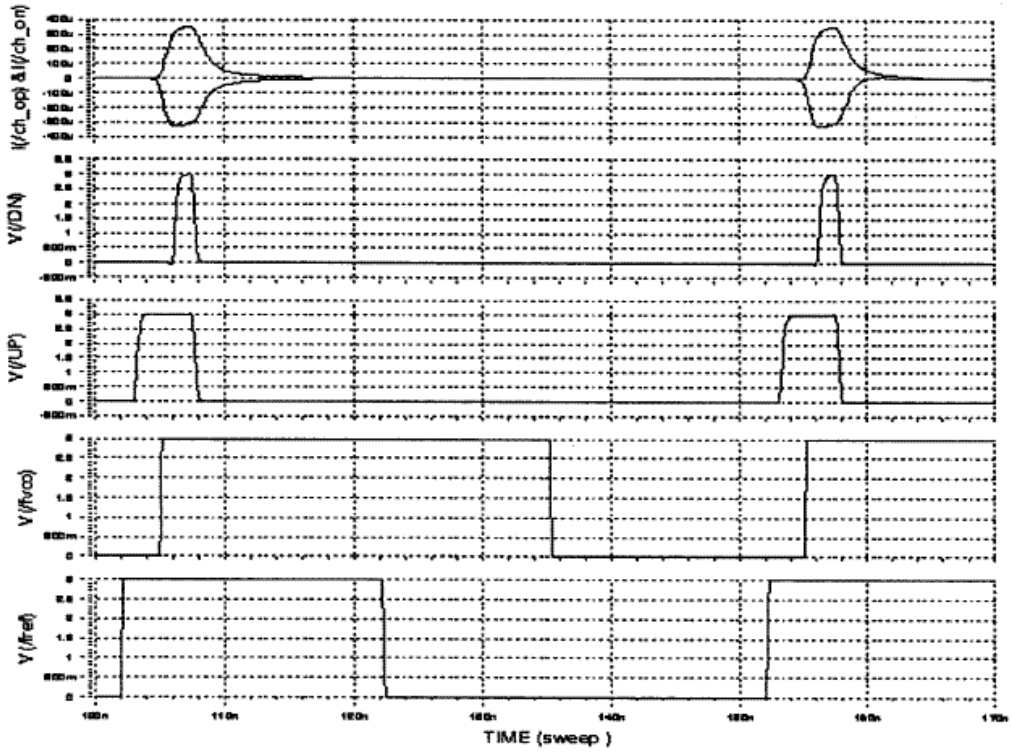


Fig. 4.3-35

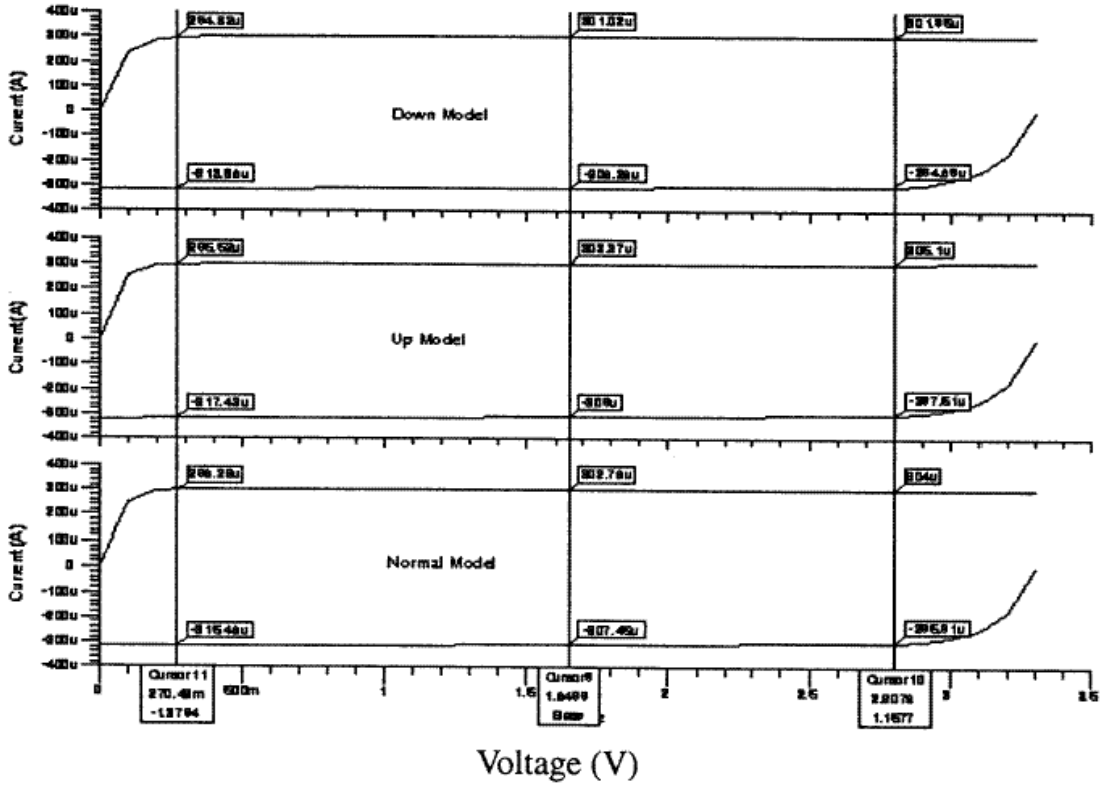
Simulated Charge-Pump Waveforms

The reference signal, f_{ref}, leads the feedback VCO signal, f_{vco}, by 3ns. The frequency of f_{ref} and f_{vco} is 20 MHz.



Simulated Charge-Pump Current Waveforms

The charge pump has been simulated over a $\pm 3\sigma$ process variation at $V_{DD} = 3.3$V.



Loop Filter Design

In order to supress the high-frequency noise introduced by the third-order, delta-sigma modulator, it will be necessary to select a higher order loop filter.

A third-order filter is chosen for this work and is shown below.

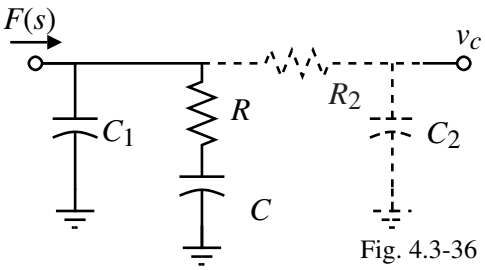


Fig. 4.3-36

The transfer function is

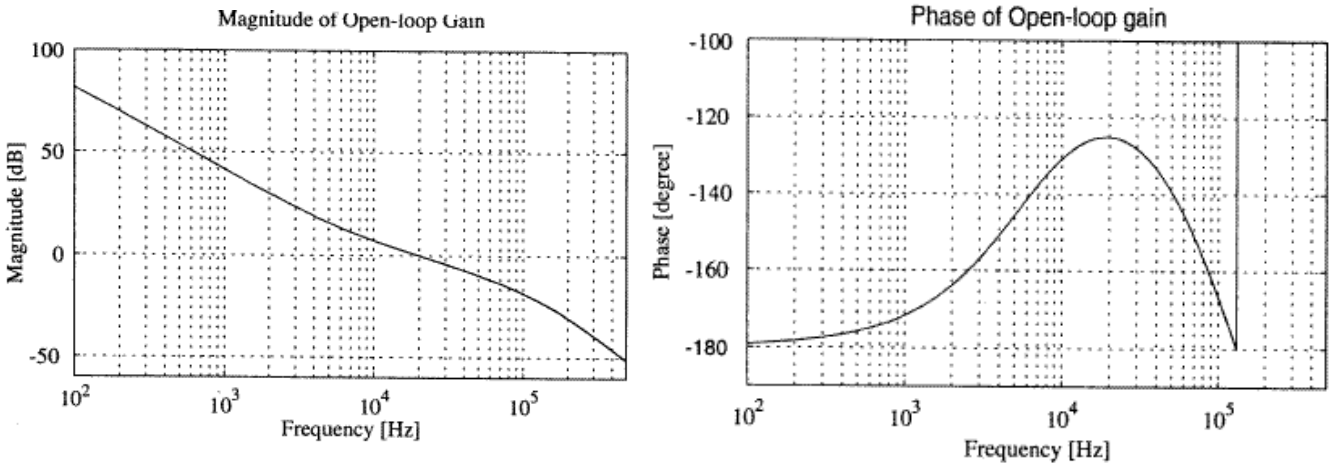
$$F(s) = \frac{1+sCR}{s^2RCC_1 + sC + sC_1} = \frac{1+s\tau_2}{s(C+C_1)(1+s\tau_1)}$$

where

$$\tau_1 = \frac{CC_1}{C+C_1}R \qquad \text{and} \qquad \tau_2 = RC$$

Actually, more supression is needed and R_2 and C_2 above are added prior to the VCO making the PLL a type-II, fourth-order.

The Third-Order Filter Response



Realization of the Loop Filter

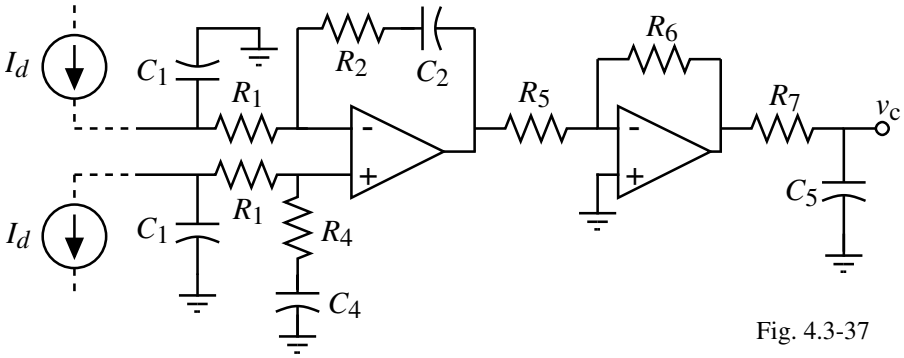


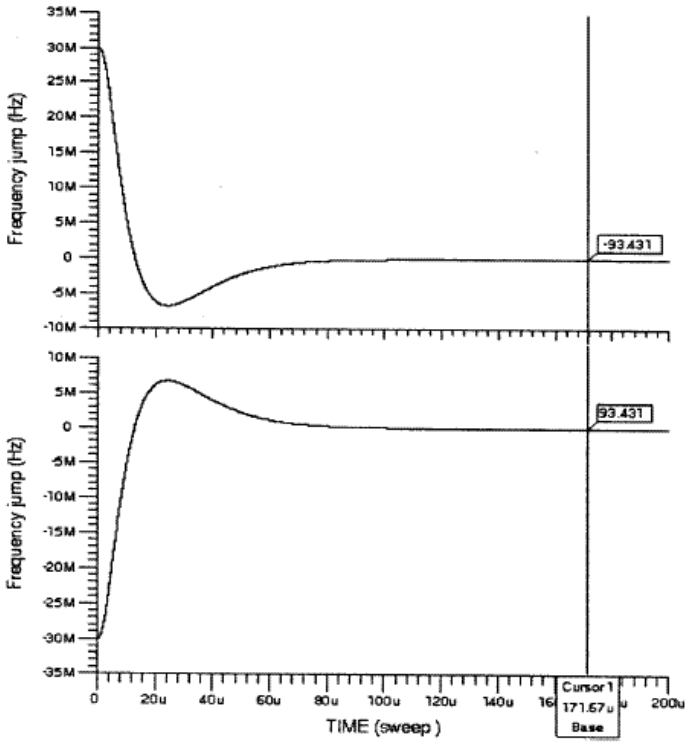
Fig. 4.3-37

The transfer function of this filter is given as,

$$F_a(s) = \frac{V_c}{I_d} = \frac{2}{sC_2}\frac{R_6}{R_5}\frac{1+sC_2R_2}{1+sC_1R_1}\frac{1}{1+sC_5R_7}$$

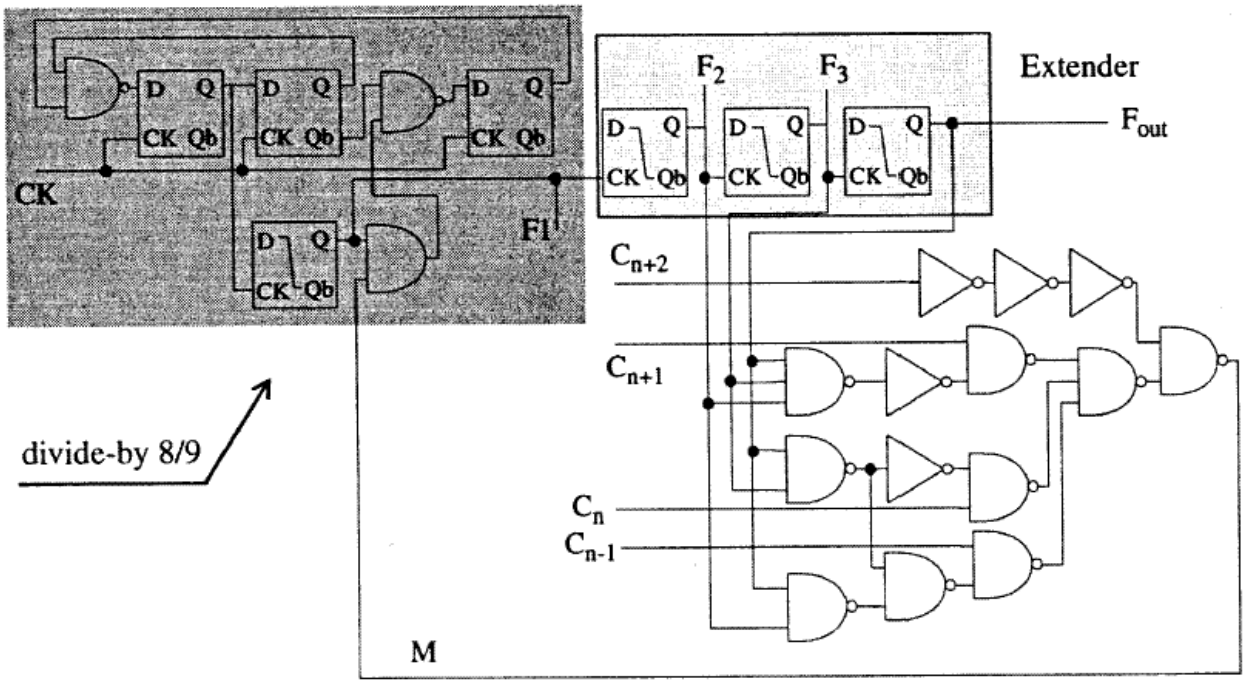
Simulated Settling Time

Simulated results for 30MHz frequency steps using behavioral modeling:



Settles to within ±100Hz at about 172μs.

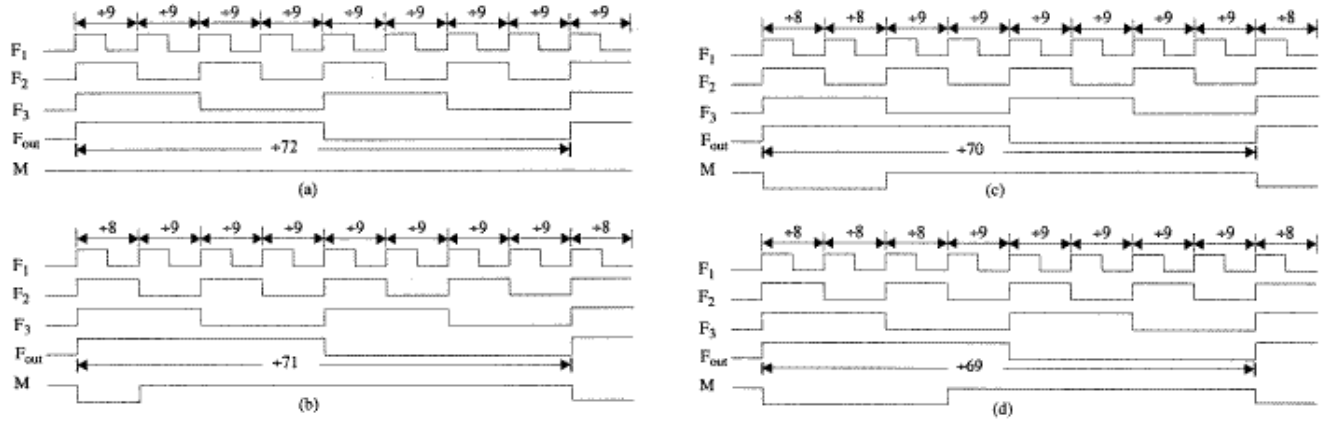
Frequency Divider



A multimodulus prescaler with four different divide ratios:

Consists of a divide-by-8/9 prescaler, composed of a synchronous divide-by-4/5 and a toggle flipflop, a three-stage extender, and control logic gates.

Timing Diagrams of the Four-Modulus Prescaler



a.) Divide-by 72: The prescaler divides by 9 for eight F_1 cycles.

b.) Divide-by 71: The prescaler divides by 8 for one F_1 cycle and 9 for seven F_2 cycles.

c.) Divide-by 70: The prescaler divides by 8 for two F_1 cycle and 9 for six F_2 cycles.

d.) Divide-by 69: The prescaler divides by 8 for three F_1 cycle and 9 for five F_2 cycles.

Eight-Modulus Prescaler:

The following multi-modulus prescaler is based on a dual-modulus prescaler.

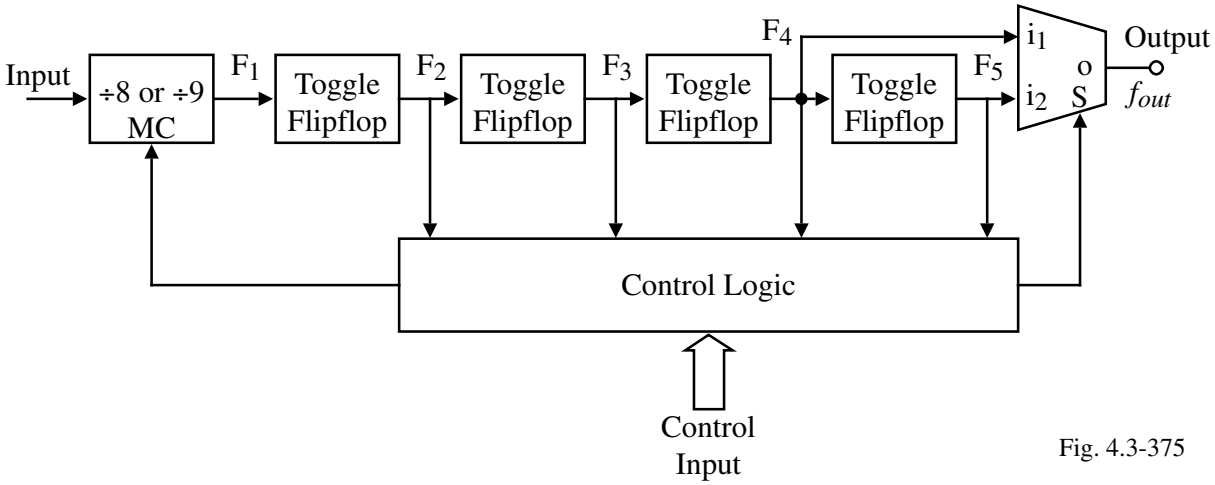


Fig. 4.3-375

The multi-modulus prescaler can achieve a divide ratio of 64 to 144.
For this work, the divide ratio is set to N-3 to N+4 where N = 70.

I.e. 67, 68, 69, 70, 71, 72, 73, and 74

Circuit Design for the Multimodulus Prescaler

To avoid switching noise generation and reduce the coupling noise from the supply line and substrate, a folded source-coupled logic and ECL-like logic were chosen.

Differential Inverter/Buffer:

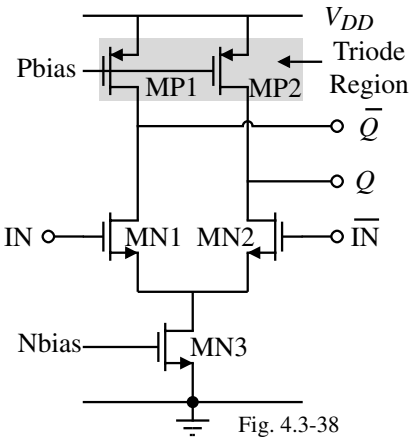


Fig. 4.3-38

Temperature and Supply Independent Biasing:

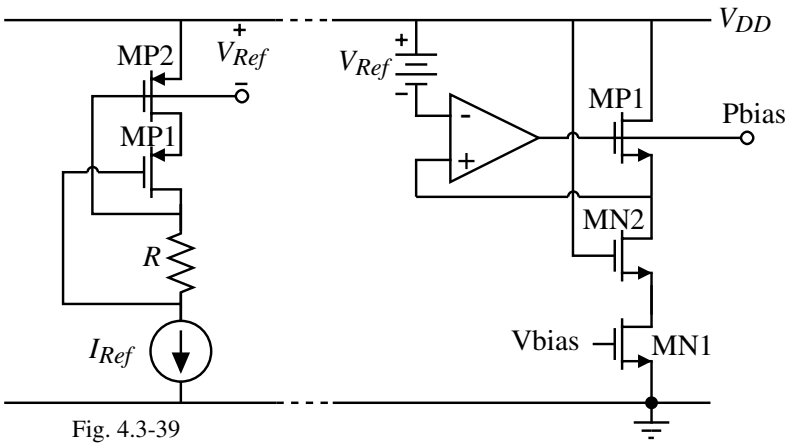


Fig. 4.3-39

$V_{ref} = I_{ref}R = 0.5\text{V}$

R is the same type of resistance used in the bandgap

Implementation of the D Flipflop with an Embedded NAND Gate

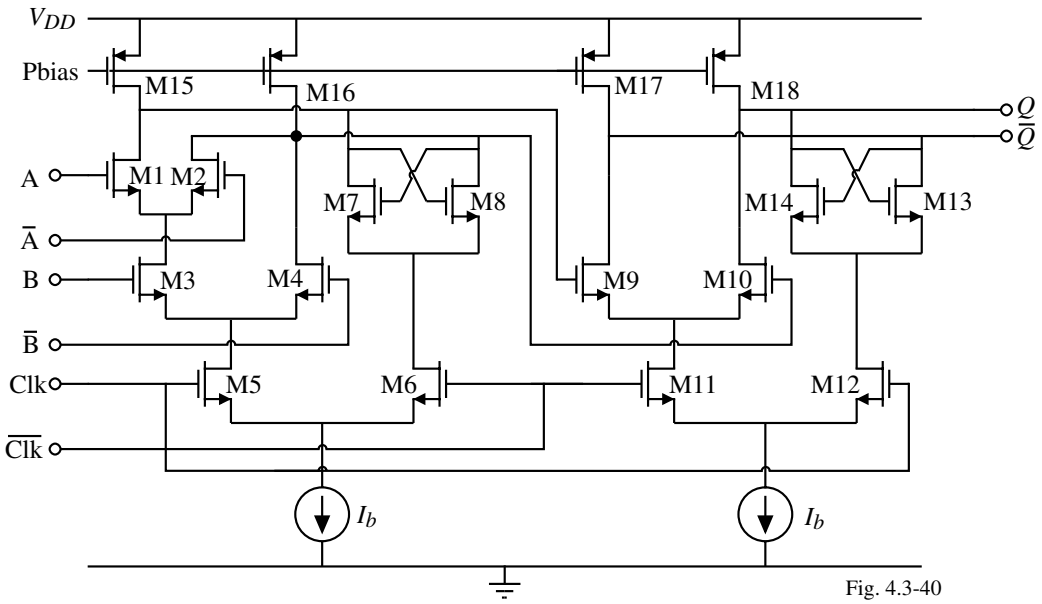


Fig. 4.3-40

Positive Edge-Triggered Toggle Flipflop

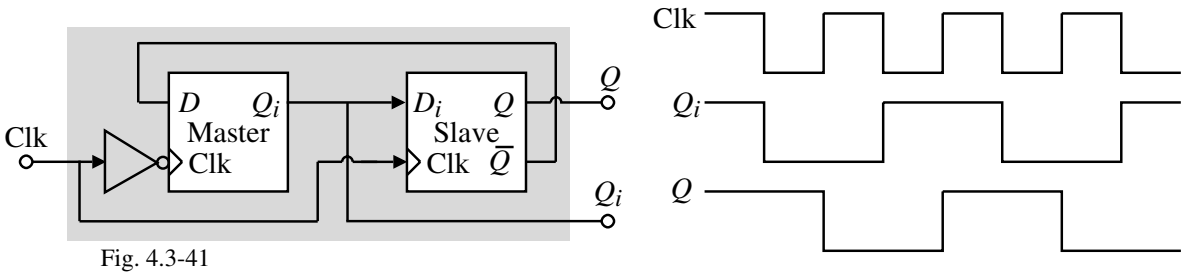
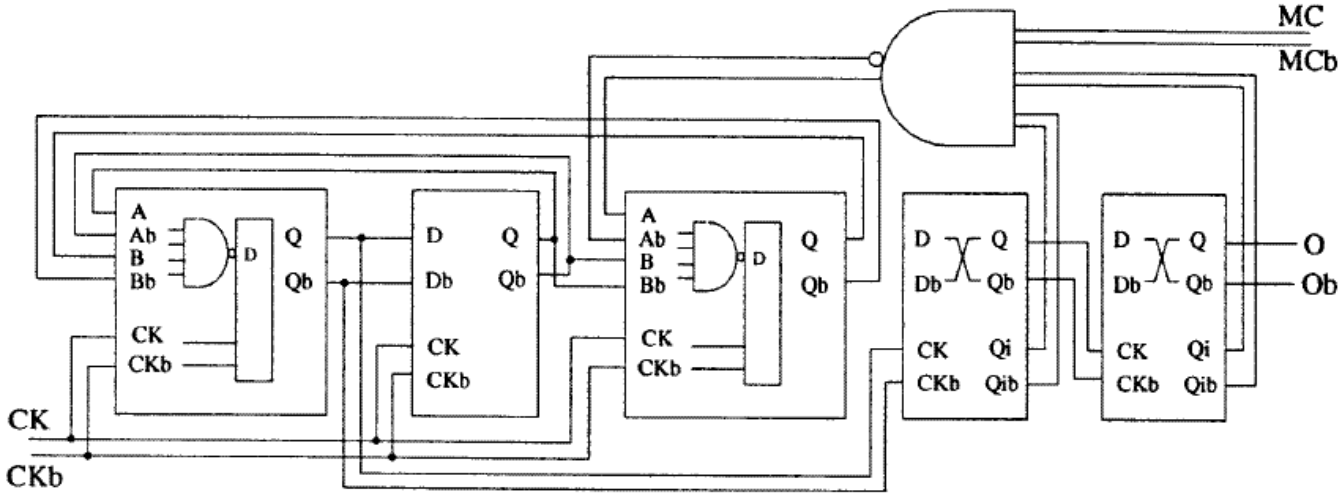


Fig. 4.3-41

Note that the master output, Q_i, always leads the slave output, Q, by 90°.

If the master output is used as the inputs to the control logic gates to generate the appropriate control signals for the prescaler, the delay requirement in a critical path of the prescaler loop is relaxed which causes reduction in power consumption.

Implementation of a 16/17 Dual Modulus Prescaler using Above Concepts



Uses the master outputs instead of the slave outputs to generate the control signals. When MC is high, the divide ratio is 17 and when MC is low, the divide ratio is 16.

Accumulator

A three-stage modulated fractional divider controller.

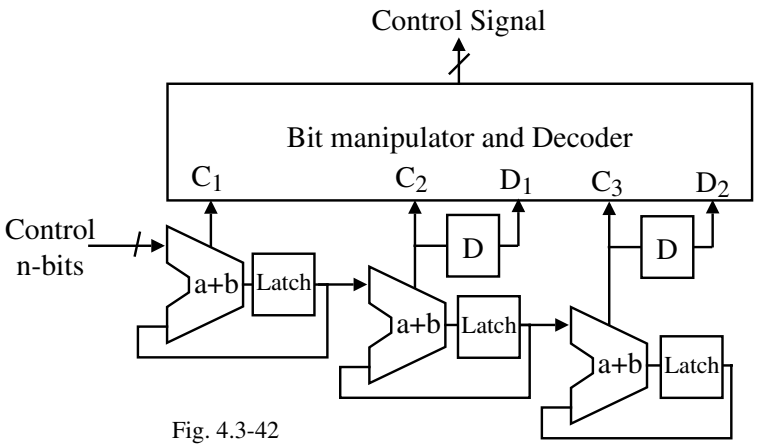


Fig. 4.3-42

This circuit generates the modulus control signals for the multi-modulus prescaler.

Bias Circuitry

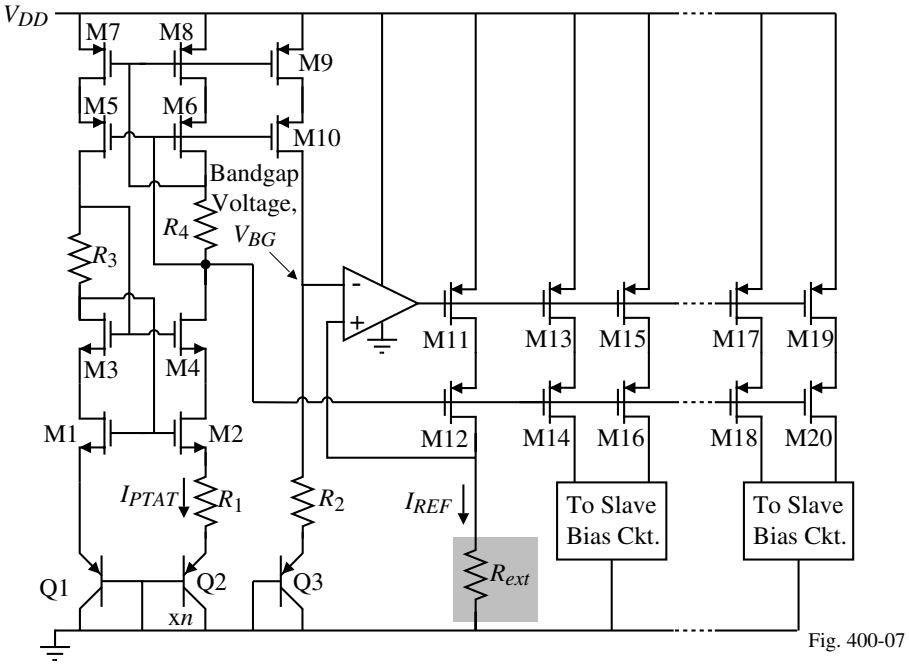


Fig. 400-07

Constant current:

$$I_{REF} = \frac{V_{BG}}{R_{ext}} \quad \text{where} \quad V_{BG} = V_{BE3} + I_{PTAT}R_2 = V_{BE3} + \frac{V_T}{R_1} ln(n) \cdot R_2$$

Bias Circuitry-Continued

Distribution of the current avoids change in bias voltage due to *IR* drop in bias lines.

Slave bias circuit:

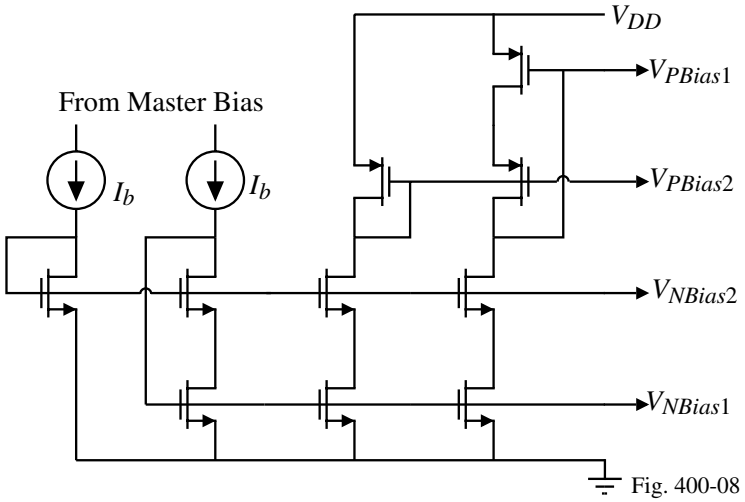


Fig. 400-08

Synthesizer Block Diagram

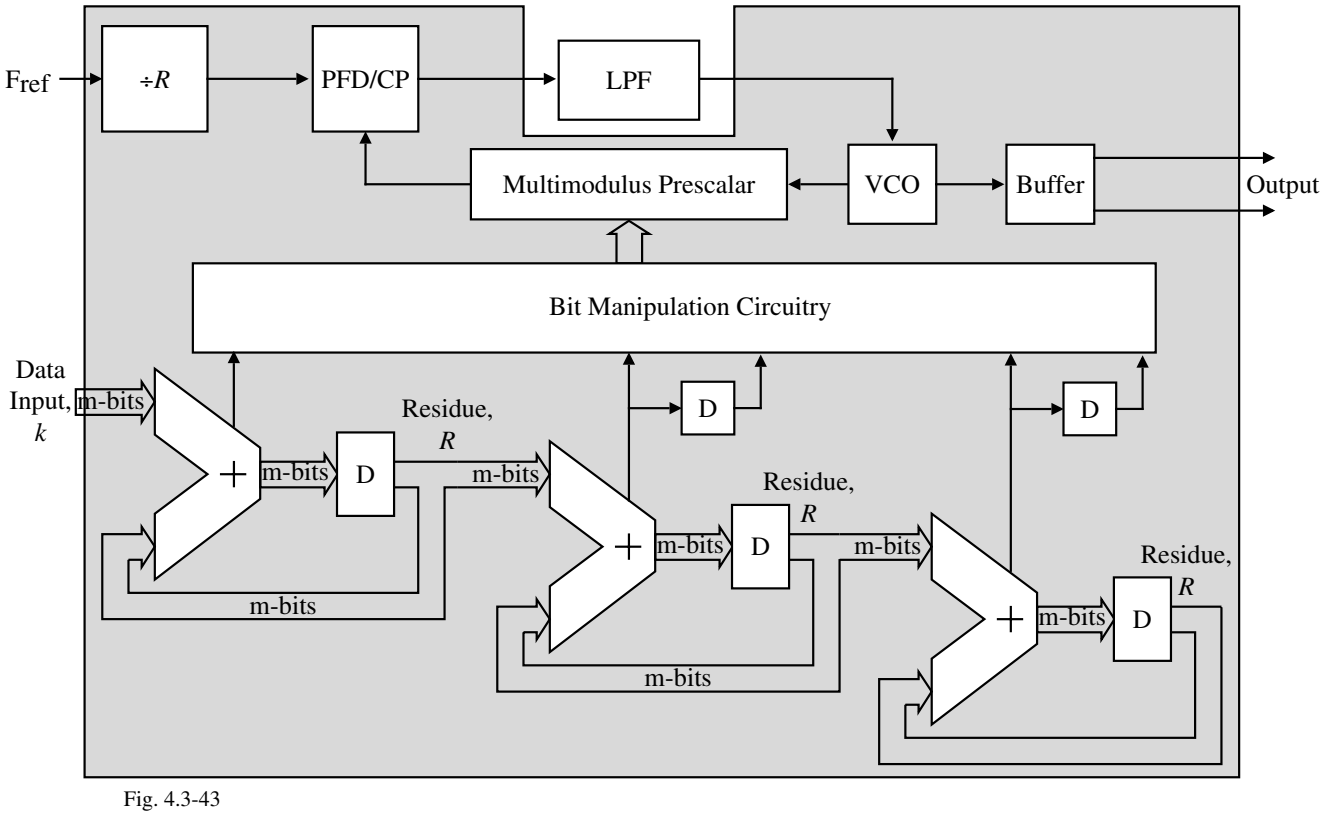
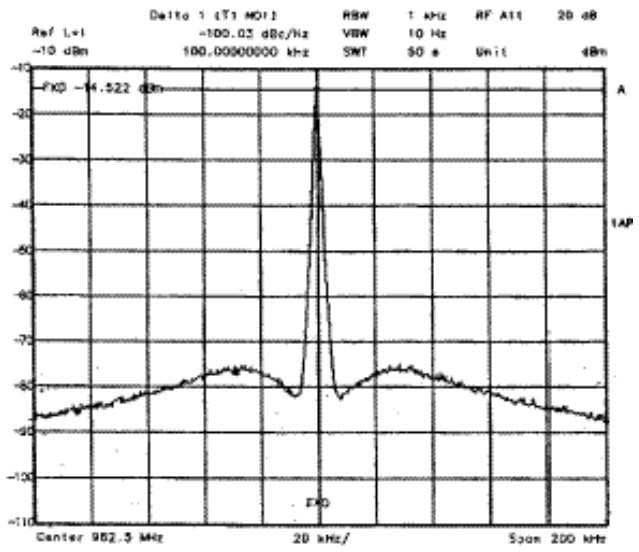


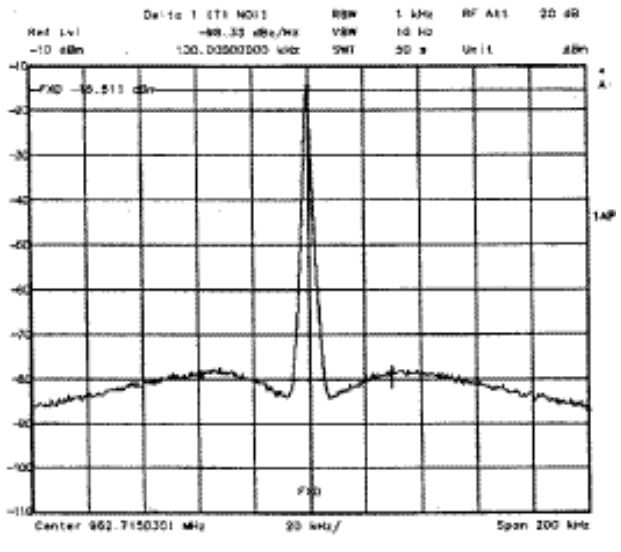
Fig. 4.3-43

Measurements – Close-In Spectrum

Close-in output spectrum with (962.5MHz) and without the delta-sigma modulator (962.715MHz, k =1):



No delta-sigma modulator

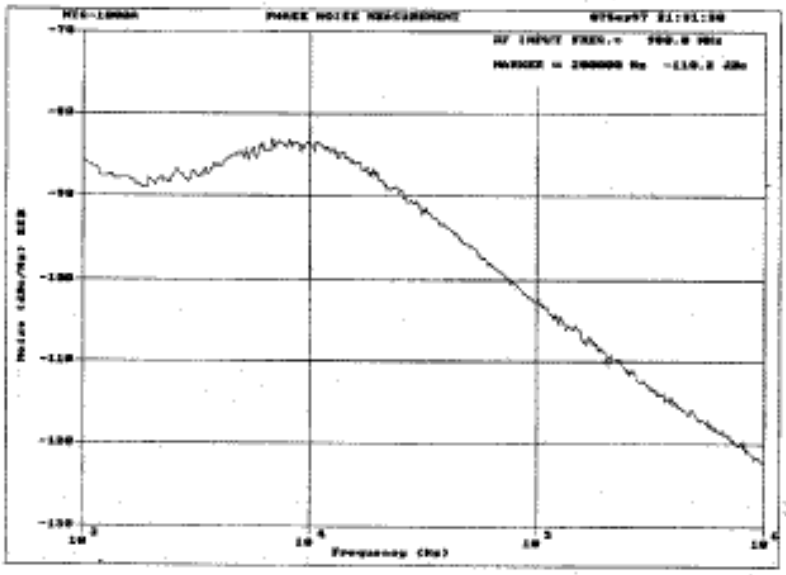


With delta-sigma modulator

The phase noise at an offset frequency of 100kHz is about 1.7dB better with the modulator.

Measurements – Single Sideband Phase Noise

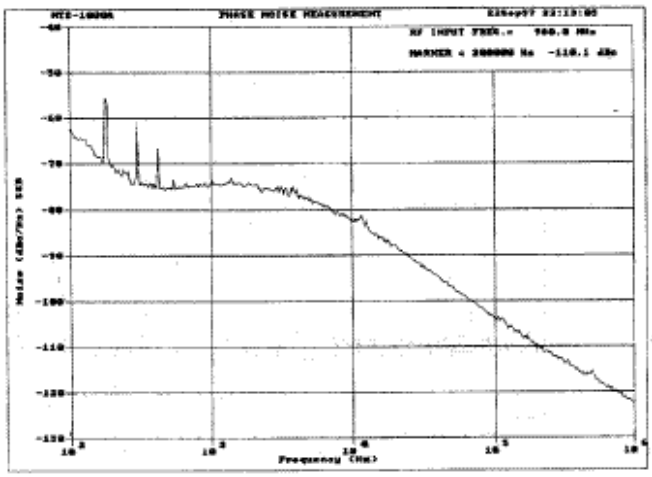
Loop bandwidth is 20kHz.

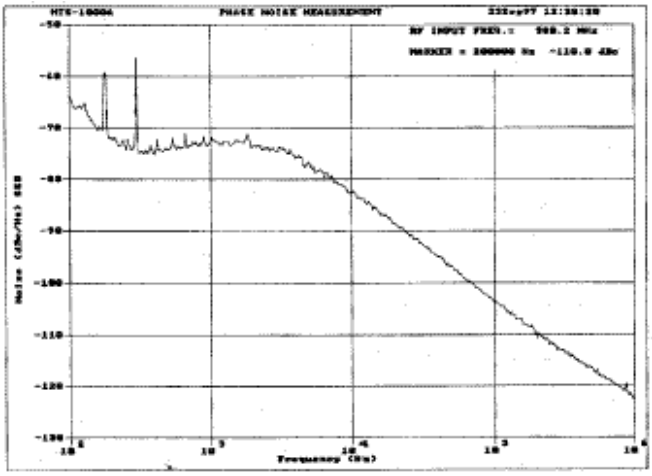


The measured phase noise is -110dBc/Hz at a 200kHz offset and -118dBc/Hz at a 600kHz offset.

Measurement – Phase Noise with a 5kHz Loop Bandwidth

f_{ref} = 14MHz, k=0 → 980MHz: f_{ref} = 14MHz, k=1 → 980.219MHz:

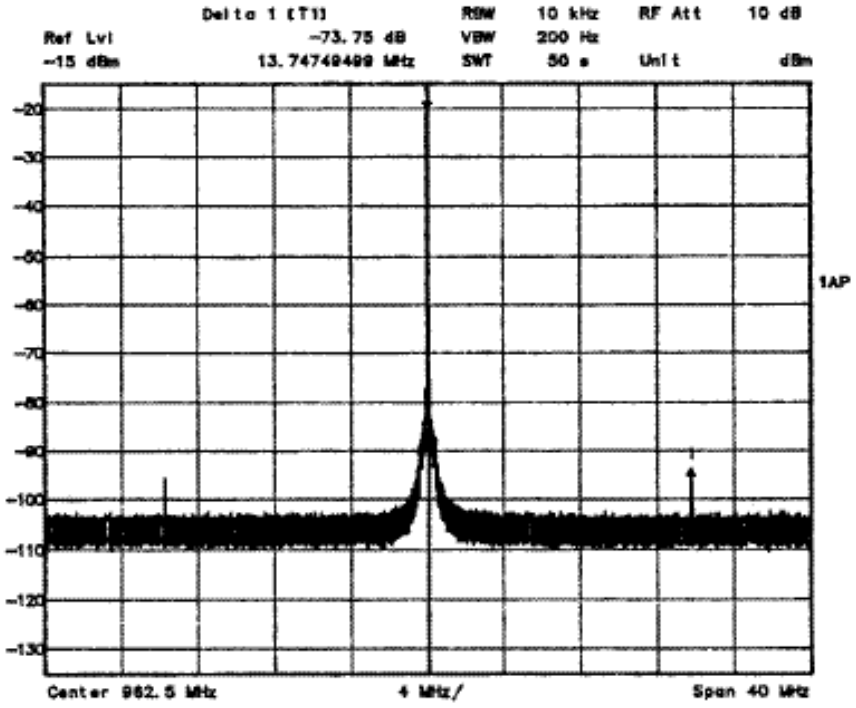




The loop filter was connected to the output of the charge pump and the input of the VCO by long wires which caused some pick-up noise to occur at the input of the VCO resulting in spur-like spikes within the loop bandwidth.

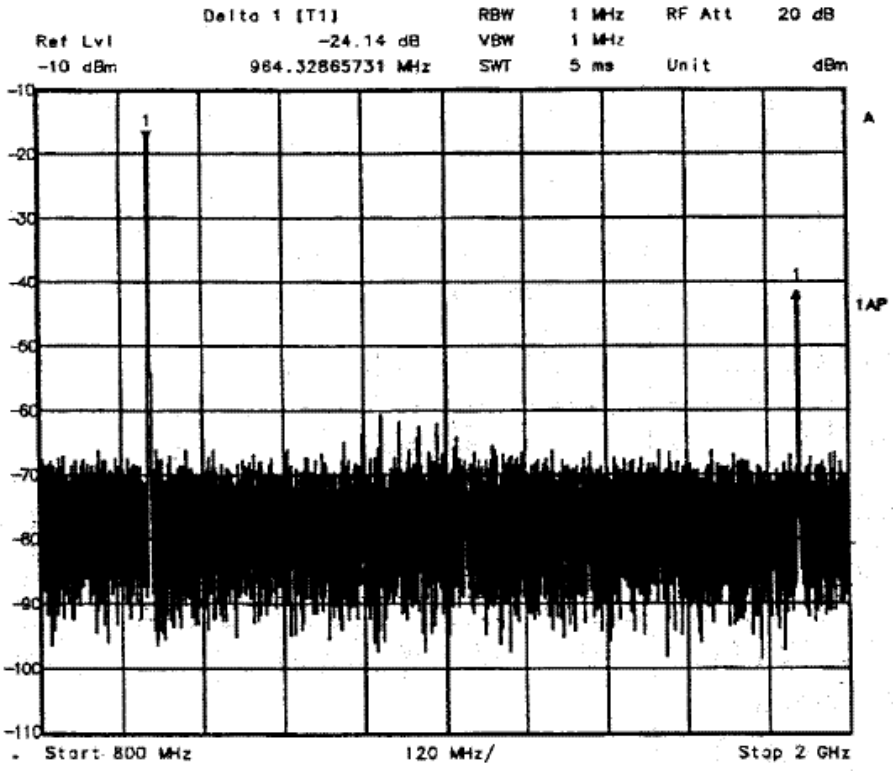
Measurements – Reference Sideband Spurs

f_o = 962.5MHz, loop bandwidth < 40kHz



The sideband spurs are less than –73.5dBc.

Measurements – Harmonic Distortion



The measured second harmonic is –24dBc.

Summary of Measured Results

Measurement	Prototype 1 (NMOS VCO)	Prototype 2 (PMOS VCO)
Close-in RMS Noise	< 2°	< 2°
Phase noise @ 200kHz	-110dBc/Hz	-110dBc/Hz
Frequency range	834-965 MHz	862-1004.5 MHz
Reference Spurs	< -71dBc	< -73.5dBc
2nd Harmonic	-24dBc	-24dBc
Simulated Settling Time	172μs	172μs
Loop bandwidth	20kHz	20kHz
Power dissipation	43mW@V_{DD} = 3.3V	43mW@V_{DD} = 3.3V 6.6mW-VCO 6.9mW-Prescaler 1.3mW-Bias 2mW-Charge Pump 0.7mW-Reference Buffer 1mW-Digital 24.4mW-VCO Buffer

SUMMARY

CMOS Frequency Synthesizer State-of-art Performance

Design	[1]	[2]	[3]	[4]
Architecture	Frac-N	Dual Loop	Frac-N	Int-N
Process	0.4µm CMOS	0.5µm CMOS	0.5µm CMOS	0.4µm CMOS
Application	DCS-1800	GSM	GSM, AMPS	WLAN
Frequency	1.8GHz	900MHz	1.1GHz	2.6/5.2GHz
Freq. Resolution	200kHz	200kHz	< 1Hz	23.5MHz
Ref. Frequency	26.6MHz	1.6MHz&205MHz	7.944MHz	11.75MHz
Loop BW	45kHz	40kHz & 27kHz	40kHz	N/A
Chip Area	3.23mm^2	2.64mm^2	11.03mm^2	2.01mm^2
Phase Noise	-121dBc/Hz @600MHz	-121.8dBc/Hz @600MHz	-92 dBc/Hz @10kHz	-115dBc/Hz @10MHz
Spurs	-75dBc	-79.5dBc	-95dBc	-53dBc
Switching Time	< 250µs	< 830µs	< 150µs	40µs
Supply Voltage	3V	2V	2.5V – 4V	2.6
Power	51mW	34mW	25mW	47mW

State-of-the Art Performance Summary – Continued

Design	[5]	[6]	[7]	[8]
Architecture	Int-N	Frac-N	Frac-N	DDS-Driven
Process	0.24µm CMOS	0.35µm CMOS	0.5µm CMOS	0.25µm CMOS
Application	WLAN	PCS	GSM	DCS-1800
Frequency	5GHz	1.9GHz	900MHa	1.7GHz
Freq. Resolution	22MHz	10kHz	12.5kHz	200kHz
Ref. Frequency	11MHz	19.68MHz	25.6MHz	≈ 8MHz
Loop BW	280kHz	N/A	80kHz	52kHz
Chip Area	1.6mm^2	5 mm^2	0.99 mm^2	> 2mm^2
Phase Noise	-101dBc/Hz @1MHz	-104dBc/Hz @100kHz	-118dBc/Hz @600kHz	N/A
Spurs	< -45dBc	N/A	-67dBc	< -70dBc
Switching Time	N/A	< 800µs	< 100µs	150µs
Supply Voltage	1.5V/2.0V	3V	1.5V	2.0V
Power	25mW	60mW	30mW	9mW

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