LECTURE 220 – CLOCK AND DATA RECOVERY CIRCUITS - III

(Reference [6])

A 10-Gb/s CMOS CLOCK AND DATA RECOVERY CIRCUIT WITH FREQUENCY DETECTION

Specification and Technology

Generic Clock and Data Recovery Block Diagram:

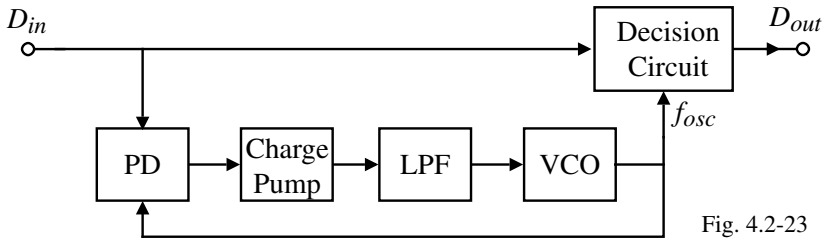


Fig. 4.2-23

Issues are:

- Jitter
- Skew between D_{in} and *Clk*
- Suitability for implementation in VLSI technology
- Power dissipation

Choice of Technology

Technology will be 0.18μm CMOS

Consequences:

- Limited speed:
  - Digital latches < 10 GHz
  - Phase detector < 10 GHz
- Low supply voltage (1.8V):
  - Limits the choice of circuit topologies
  - Leads to a large VCO gain and potentially high jitter

Choice of VCO

- LC
  - Small jitter
  - High center frequency
  - Narrow tuning range
  - Single-ended control
- Ring Oscillator
  - Large jitter
  - Low center frequency
  - Wide tuning range
  - Differential control

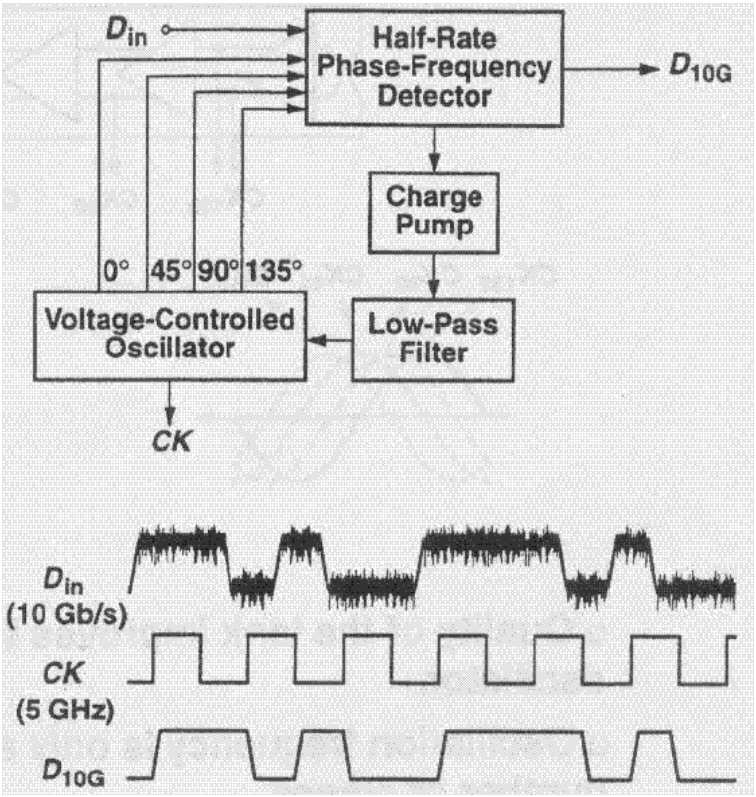
Phase Detector Design Issues

1.) System level
    Linear PD versus a bang-bang (Alexander)
2.) Technology limitations
    Full rate PD versus a half rate PD
3.) Skew problems
    No regeneration versus inherent regeneration

Frequency Detector Design Issues

1.) Capture range
    Analog versus digital
2.) System complexity
    Additional frequency detector versus phase detector compatibility
3.) Technology limitations
    Full rate FD versus a half rate FD

Clock Data Recovery Architecture for this Example



Multiphase VCO

Use a 4-stage ring oscillator with spiral inductors and MOS varactors.

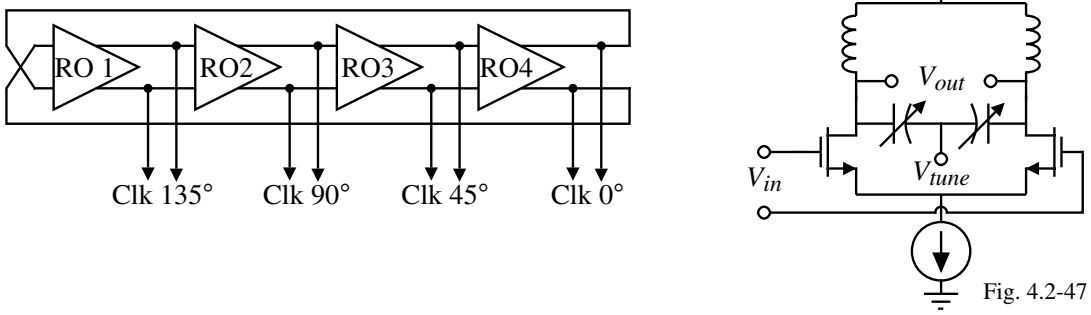


Fig. 4.2-47

Comments:

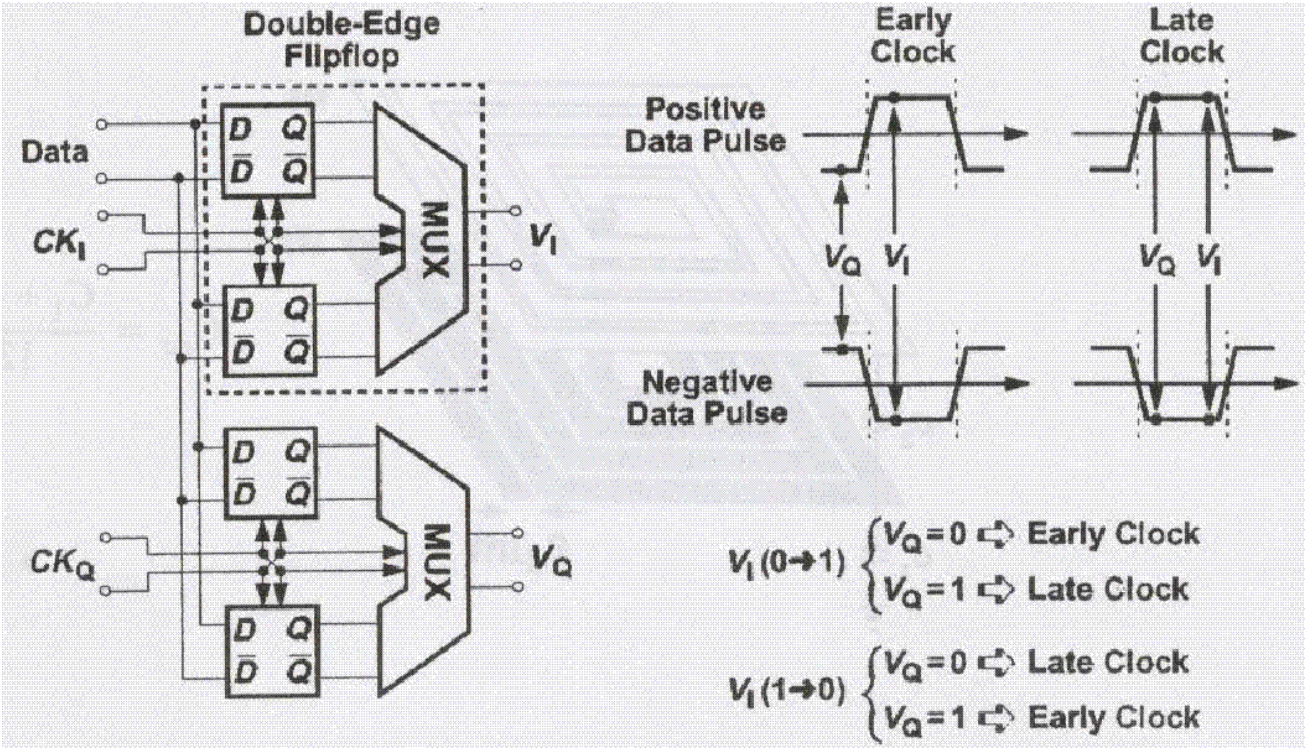
- The LC tank improves the phase noise of the oscillator
- The oscillation frequency is only a weak function of the number of stages

If we model each stage by a parallel RLC circuit, the phase shift of each stage should be 45°. Therefore,

$$\text{Arg}[Z(j\omega)] = 45° \quad \Rightarrow \quad \tan^{-1}\left(\frac{L\omega}{R_p(1\text{-}LCQ\omega^2)}\right) = 45° \quad \Rightarrow \quad \omega_{osc} = \frac{1}{\sqrt{LC}}\sqrt{1 - \frac{1}{Q}}$$

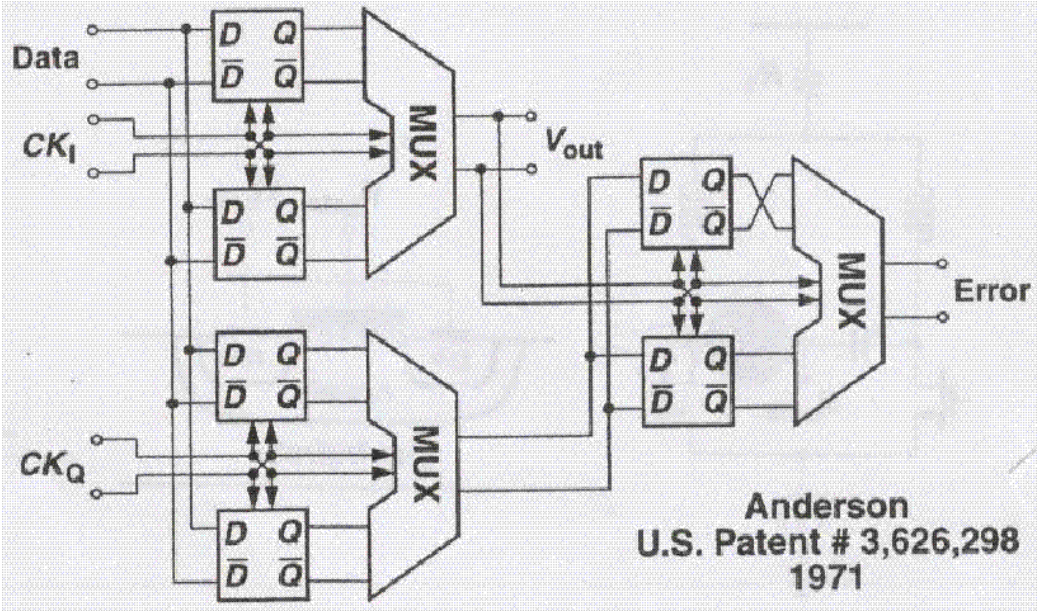
- The oscillator's common mode level is shifter to provide a large tuning range.

Half-Rate Phase Detection



If V_1 makes a high-to-low transition, V_Q must be inverted to provide consistent phase error information.

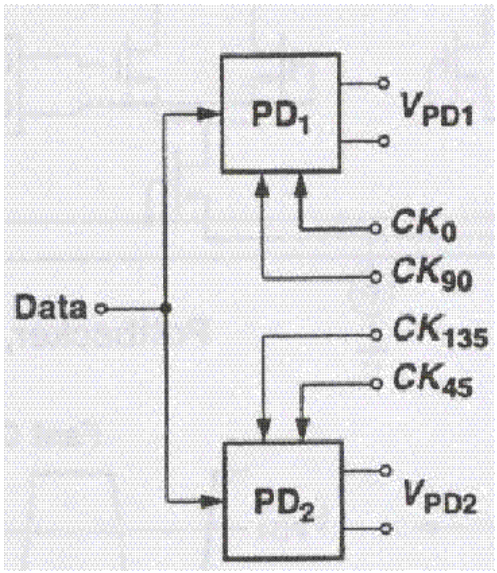
Overall Phase Detector

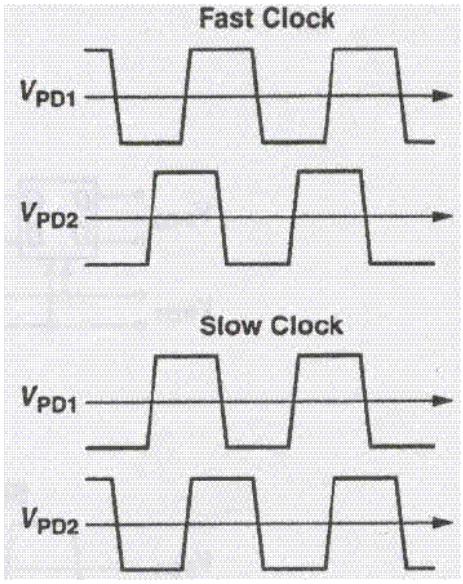


Comments:

- CK_I and CK_Q are 5GHz quadrature clock phases
- Data is a 10 Gb/s input data signal
- V_{out} is a 10 Gb/s output data signal

Half-Rate Frequency Detection

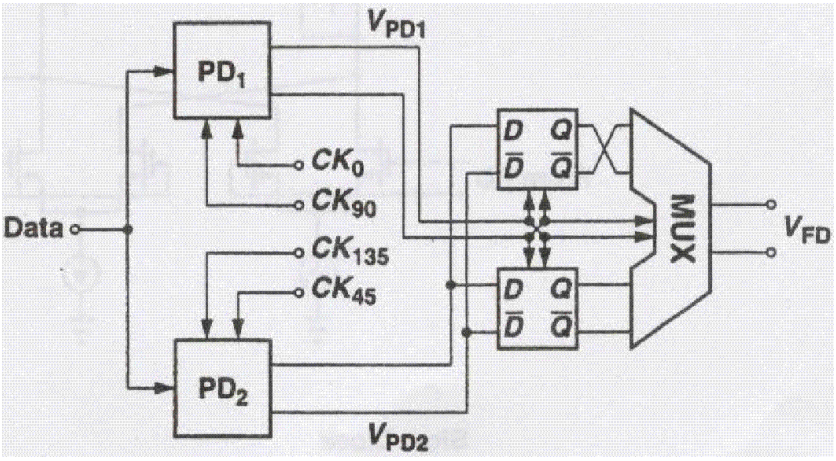




$$V_{PD1}(0\rightarrow 1)\begin{cases} V_{PD2}=0 \Rightarrow \text{Slow Clock} \\ V_{PD2}=1 \Rightarrow \text{Fast Clock} \end{cases}$$

$$V_{PD1}(1\rightarrow 0)\begin{cases} V_{PD2}=0 \Rightarrow \text{Fast Clock} \\ V_{PD2}=1 \Rightarrow \text{Slow Clock} \end{cases}$$

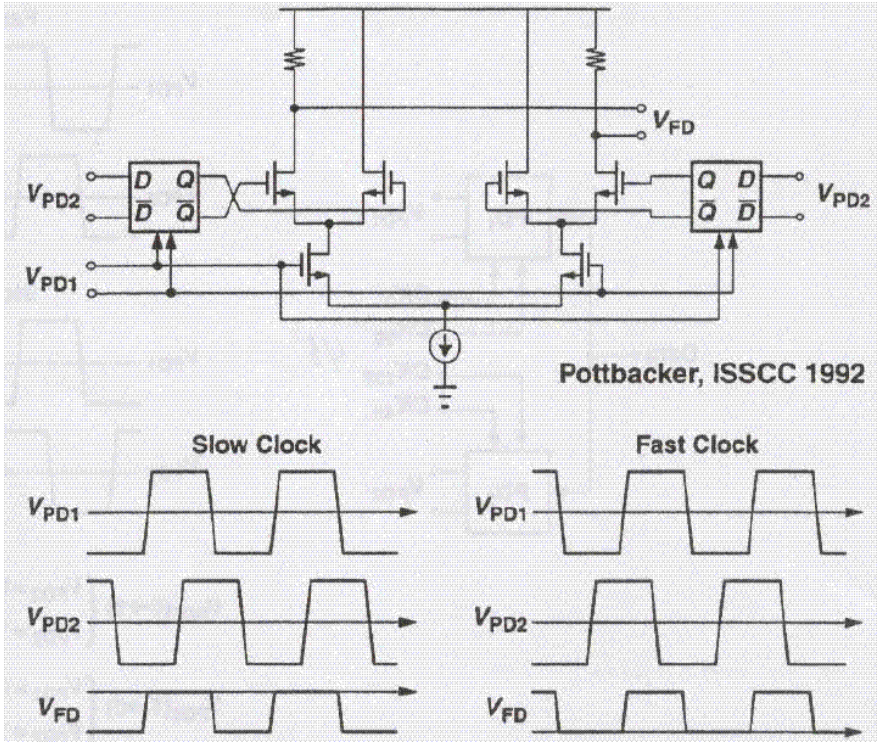
Half-Rate Frequency Detector



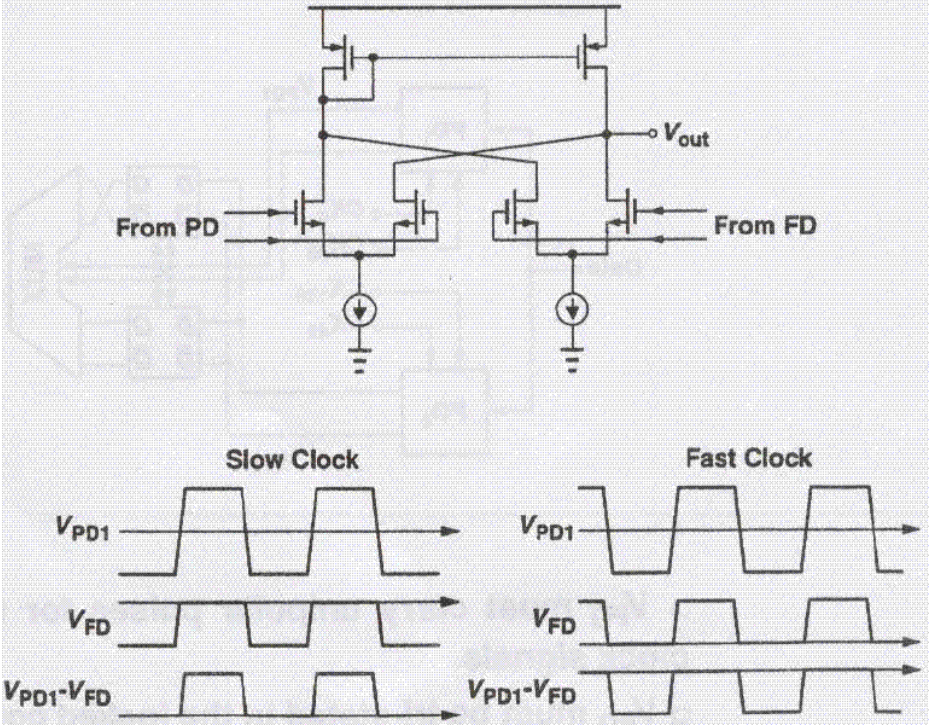
Comments:

- V_{FD} must carry unipolar pulses for fast and slow clock signals.
- V_{FD} must be a tri-state signal in the locked condition.

Modified Multiplexer



Charge Pump



Output Buffer

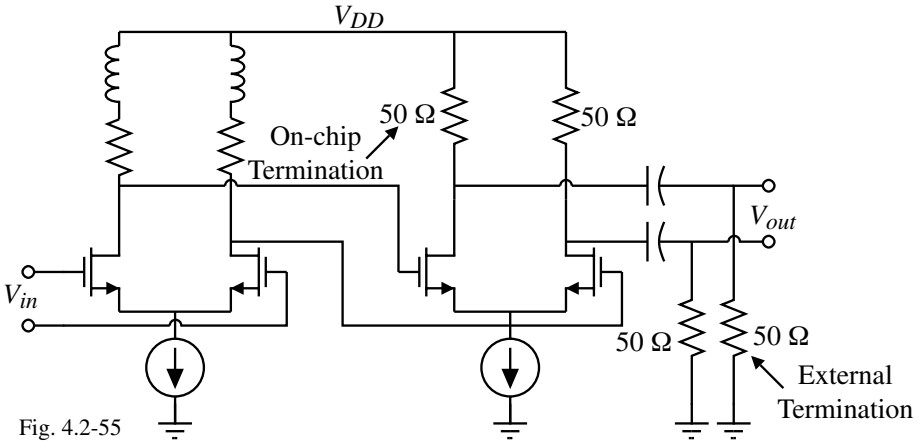
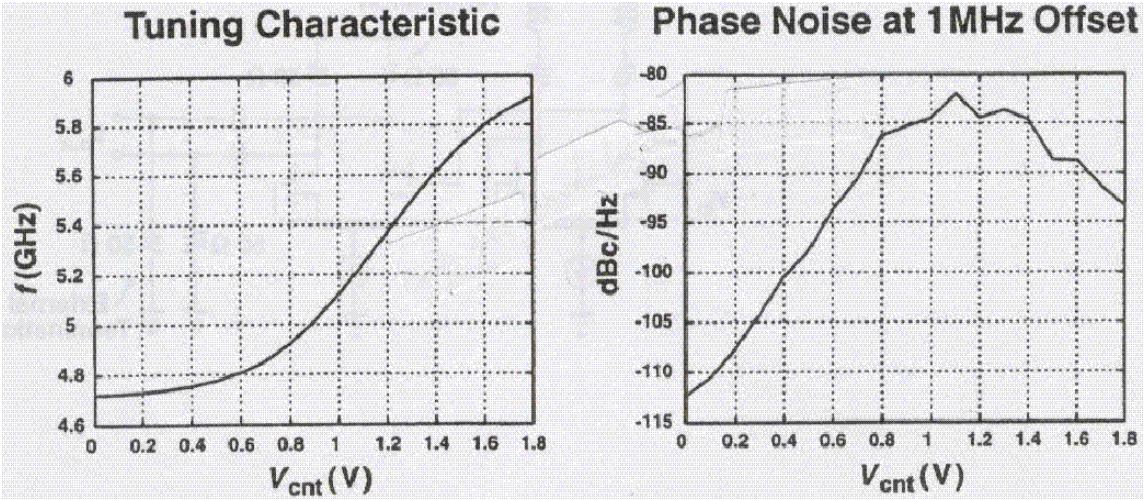


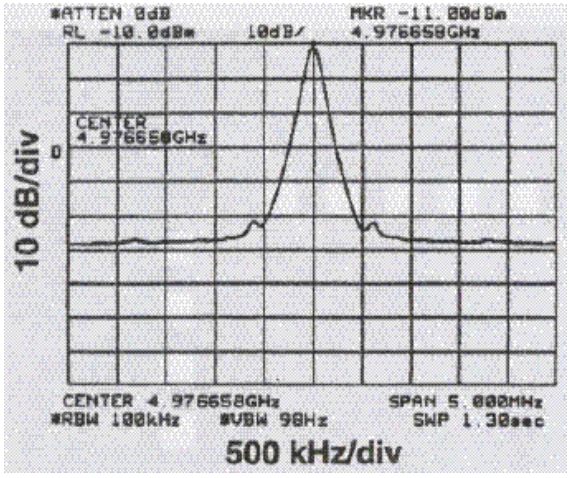
Fig. 4.2-55

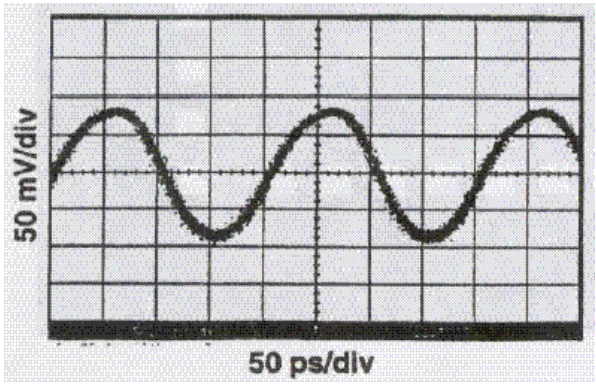
The inductors have a line width of 4μm to achieve a high self-resonance frequency.

Measured Open-Loop VCO Characteristics



Measured Recovered Clock

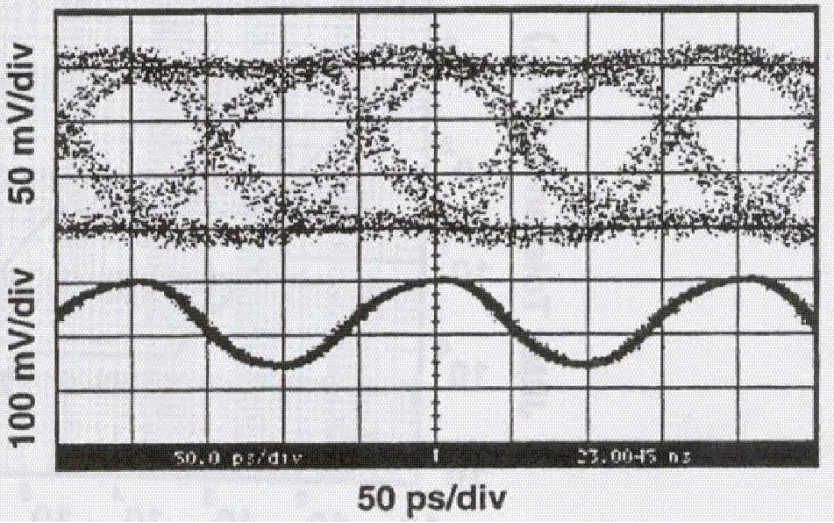




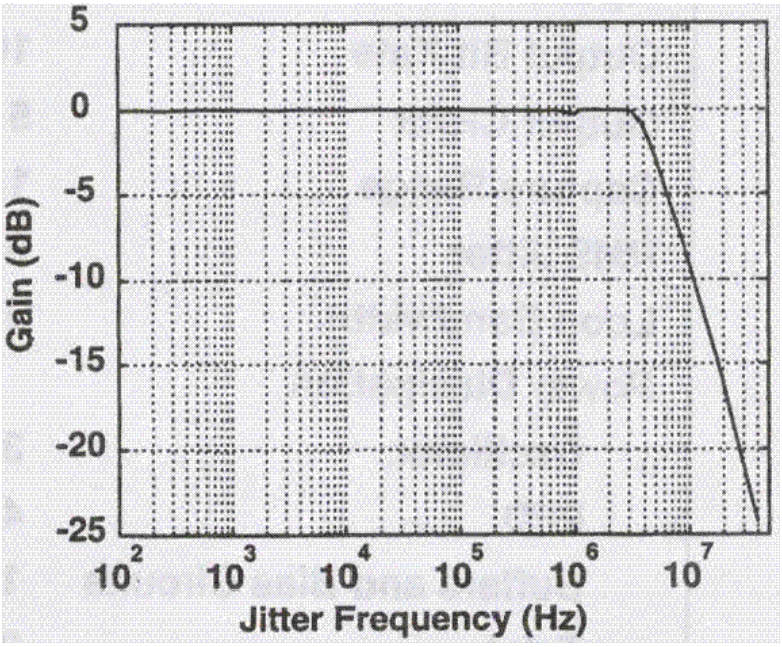
Phase noise: -107 dBc/Hz at 1MHz offset.

Input Sequence (PRBS)	Jitter (pp) (ps)	Jitter (rms) (ps)
2^{23}-1	9.9	0.8
2^{7}-1	2.4	0.4

Measured Data

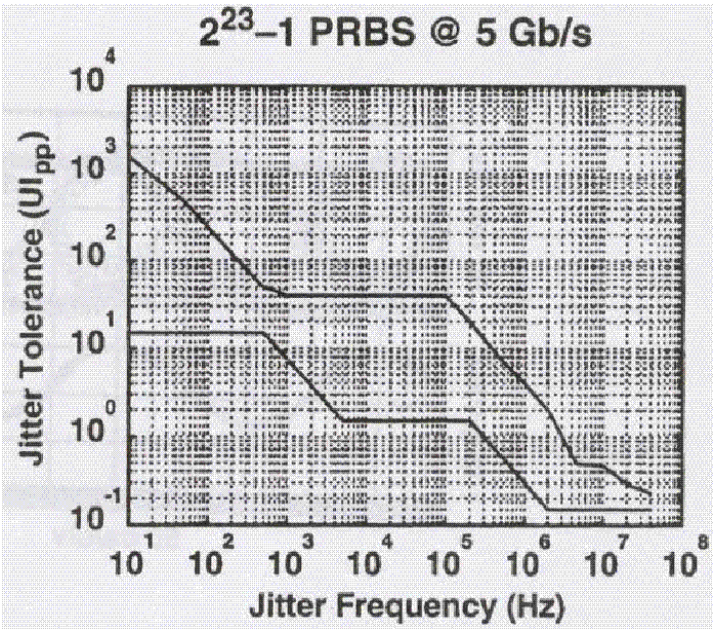


Measured Jitter Transfer Characteristic



Loop Bandwidth = 5.2 MHz
Jitter Peaking = 0.04 dB

Measured Jitter Tolerance Characteristic



BER@10Gb/s = 10^{-9}

BER@5Gb/s = 10^{-12}

Output buffer probably increases the BER at lower bit rates.

Performance Summary

Characteristic	Performance
Input Bit Rate	10 Gb/s
Output Bit Rate	10 Gb/s
Output Clock	5 GHz
Capture Range	1.43 GHz
RMS Jitter	0.8 ps
Loop Bandwidth	5.2 MHz
Power Dissipation Oscillator: PFD: Buffers and Bias Circuits Total	 30.6 mW 42.2 mW 18.2 mW 91 mW
Area	1.75 mm x 1.55 mm
Supply Voltage	1.8V
Technology	0.18 μm CMOS

Summary of 10Gb/s Example

- A half-rate architecture relaxes the speed constraints of the system.
- A four-stage LC oscillator provide multiple phases with low jitter.
- A half-rate phase and frequency detector with inherent retiming is introduced.
- Inductive peaking enhances speed of the output buffers.

SUMMARY

Outline of Material Covered

Introduction to Phase Locked Loops (PLLs)

Systems Perspective of PLLs

- Linear PLLs
- Digital PLLs (DPLLs)
- All-Digital PLL (ADPLLs)
- PLL Measurements

Circuits Perspective of PLLs

- Phase/Frequency Detectors
- Filters and Charge Pumps
- Voltage Controlled Oscillators (VCOs)
- Phase Noise in VCOs

PLL Applications and Examples

- Applications of PLLs
- Clock and Data Recovery Circuits
- Frequency Synthesizers for Wireless Applications

Objective

Understand and demonstrate the principles and applications of phase locked loops using integrated circuit technology with emphasis on CMOS technology.

CMOS Technology

How well does CMOS do the PLL?

- Very good for digital circuits and lower speed analog circuits
- Practical speed limits are found around 5-10 GHz. The primary challenge here is the VCO.
- At this point, circuit cleverness should allow most PLL applications to be possible and practical. With time, CMOS technology should allow the speed barrier to be pushed out.

Some Key Points

- CMOS is capable of implementing all types of PLLs – LPLL, DPLL, and ADPLL
- Noise in the PLL consists of component noise and timing jitter, both resulting in phase noise.
- Blocks of the PLL include the PFD/PD, filter, and VCO.
- To reduce phase noise in PLLs due to the VCO:
  - Make the tank Q or resonator Q large
  - Maximize the signal power
  - Minimize the impulse sensitivity function (ISF)
  - Force the energy restoring circuit to function when the ISF is at a minimum and to deliver its energy in the shorted possible time.
  - The best oscillators will possess symmetry which leads to minimum upconversion of 1/f noise.

Applications of PLLs

1.) Clock and data recovery
    2.5 Gb/s
    10 Gb/s
2.) Frequency synthesizer
    GSM
    Bluetooth

Pertinent References

1. F.M Gardner, *Phaselock Techniques*, 2nd edition, John-Wiley & Sons, Inc., New York, 1979.
2. B. Razavi (ed.), *Monolithic Phase-Locked Loops and Clock Recovery Circuits*, IEEE Press, 1997.
3. R.E. Best, *Phase-Locked Loops: Design, Simulation, and Applications*, 4th edition, McGraw-Hill, 1999.
4. T. H. Lee and A. Hajimiri, "Oscillator Phase Noise: A Tutorial," *IEEE J. of Solid-State Circuits*, Vol. 35, No. 3, March 2000, pp. 326-335.
5. A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and Phase Noise in Ring Oscillators," *IEEE J. of Solid-State Circuits*," Vol. 34, No. 6, June 1999, pp. 790-336.
6. B. Razavi, *Design of Integrated Circuits for Optical Communications*, McGraw-Hill, 2003
7. Recent publications of the *IEEE Journal of Solid-State Circuits* and the proceedings of the *International Solid-State Circuits Conference*.

