# RESEARCH OVERVIEW IN ANALOG IC DESIGN

## February 17, 2000

Prof. Phillip E. Allen
School of Electrical and Computer Engineering
Georgia Institute of Technology
pallen@ece.gatech.edu

## OUTLINE

- **Electronic Design Applications Area**
- **Analog Integrated Circuit Research Program**
  - **On-chip filter research**
  - **High-performance frequency synthesizers**
  - **1.5V, 1mW, 98dB $\Delta\Sigma$ analog-digital converter**
  - **On-chip, DC-DC conversion**
  - **Recent publications**
- **Summary**

# ELECTRONIC DESIGN AND APPLICATIONS AREA

## WHAT IS THE EDA AREA?

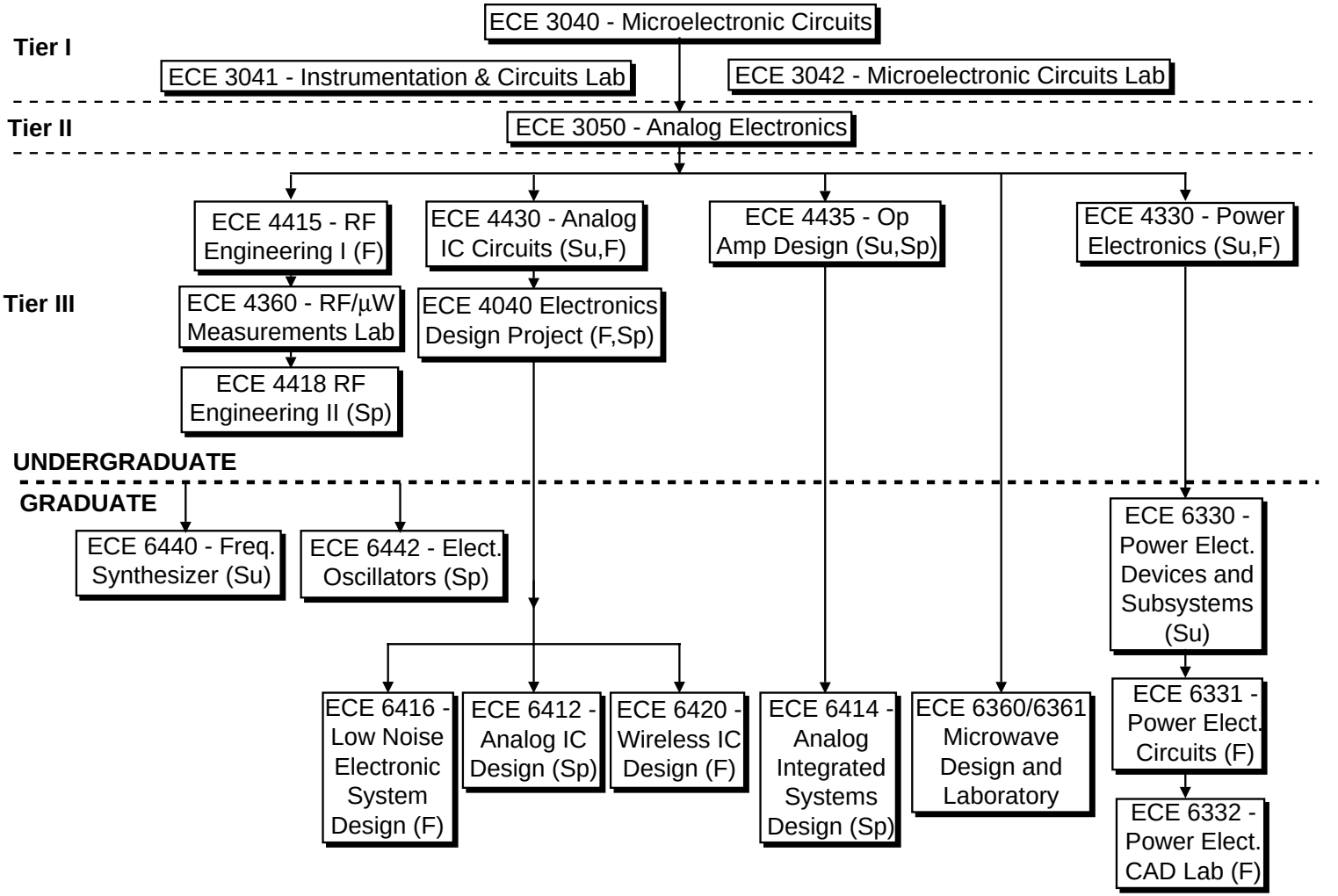
The EDA area is a group of faculty, graduate students, and courses in the area of electronic design using both discrete and integrated circuit technology.

The key activity of this area is design.

## FACULTY

Phillip Allen - Analog IC design
Martin Brooke - Analog IC design
Alvin Connelly - Analog IC design
Stephen DeWeerth - Analog VLSI design
Robert Feeney - RF circuits and systems design
Paul Hasler - Floating gate MOS applications in analog IC design
David Hertling - RF circuits and systems design
Steve Kenny - RF amplifiers and systems
Joy Laskar - Microwave circuits design
Marshal Leach - Audio circuit and systems design
Bill Sayle - Electronic design
John Uyemura - Digital IC design

# SEMESTER CURRICULUM IN ELECTRONIC DESIGN APPLICATIONS




PEA 2/15/00

# ANALOG INTEGRATED CIRCUIT RESEARCH PROGRAM

## OBJECTIVE

- Apply analog circuit design methods to standard technology to achieve improved performance
  - Increased frequency
  - Decreased power
  - Reduced area
  - Increased accuracy (dynamic range)
- Develop new design techniques and methods to increase the effectiveness of analog circuit design
  - Enhanced resuability and reconfigurability
  - Understand the implications of differing technology
  - Capture design expertise
  - Increased design robustness

## FOCUS

Wireless analog IC design particularly on-chip filters and low-phase noise frequency synthesizers suitable for software programmable radio applications.

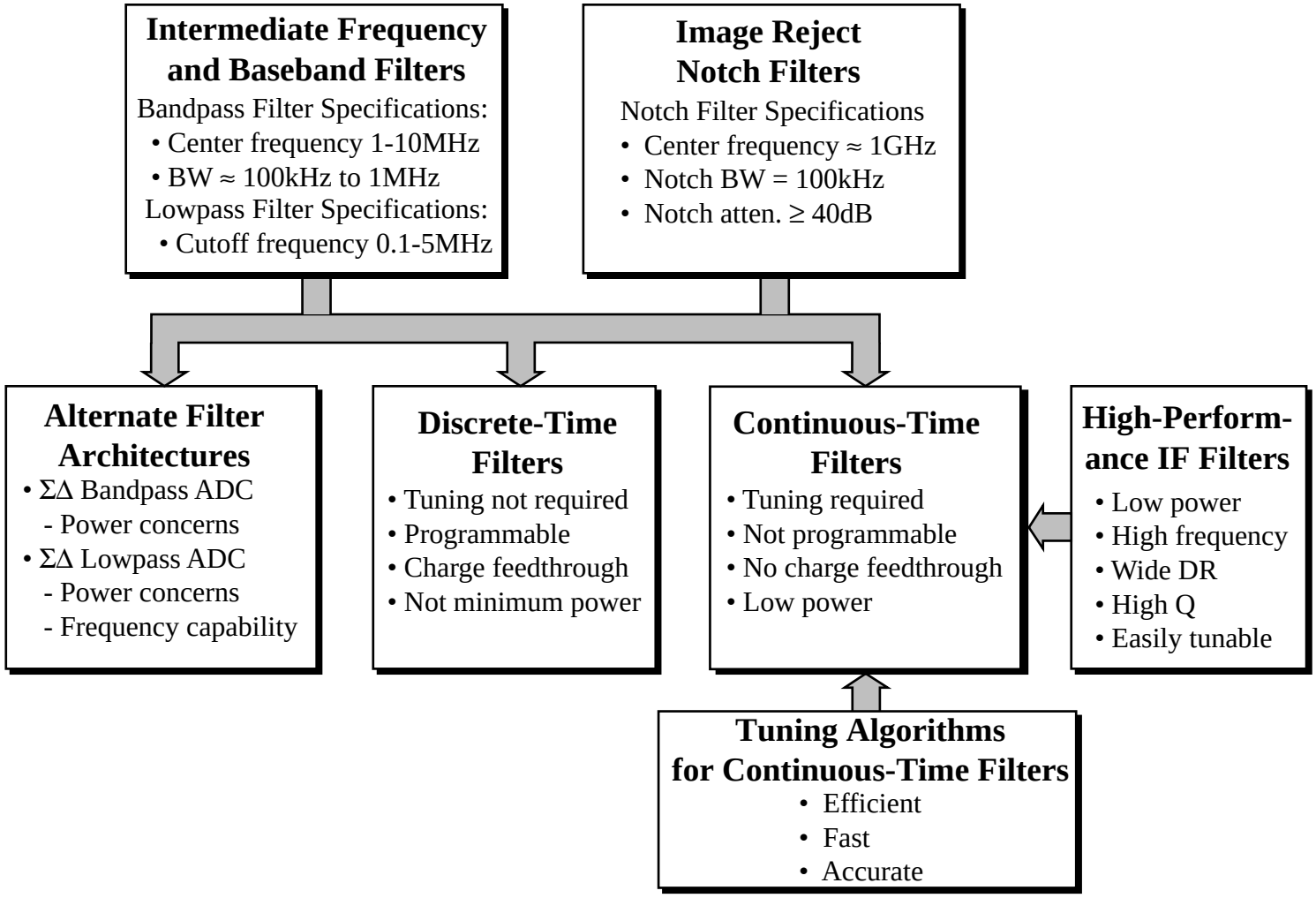
## PRESENT PROJECTS

- RF on-chip filters for band selection - *Mustafa Koroglu*
- IF on-chip filters for channel selection

  Switched current filters with reduced clock feedthrough - *Ganesh Balachandran*
  Low power bandpass, sigma-delta modulators for IF conversion - *Changhyuk Cho*
  Wide-dynamic range filters - *Fang Lin*
  Log domain filters using BiCMOS technology - *Franklin Bien*
  Low power filters - *Zhiwei Dong*
  Tuning algorithms for low power, high-accuracy continuous time filters - *Tien Pham*
- Frequency synthesizers

  CMOS fractional-N and integer-N frequency synthesizer - *Benyong Zhang* (NSC)
  SiGe frequency synthesizer for OFDM applications - *Han-Woong Son*
- Efficient, on-chip, DC-DC conversion and regulation - *Dr. Habetler, Wei-Chung Wu, Jonathan Griffith*
- Noise insensitive analog signal processing in a mixed signal environment - *Eric Kim*
- Op amps with gain-bandwidths of greater than 500MHz in standard CMOS - *Naratip Wongkomet*
- Low power, delta-sigma analog-digital converters - *Oguz Altun* (TI)
- A prefabricated design experience with CMOS op amps - *Lee-Kyung Kwon*
- A web-based analog testing capability - *Kyong-Pil Jeong*
- 1/f noise measurements for short-channel CMOS - *Hoon Lee*

# ON-CHIP FILTER RESEARCH

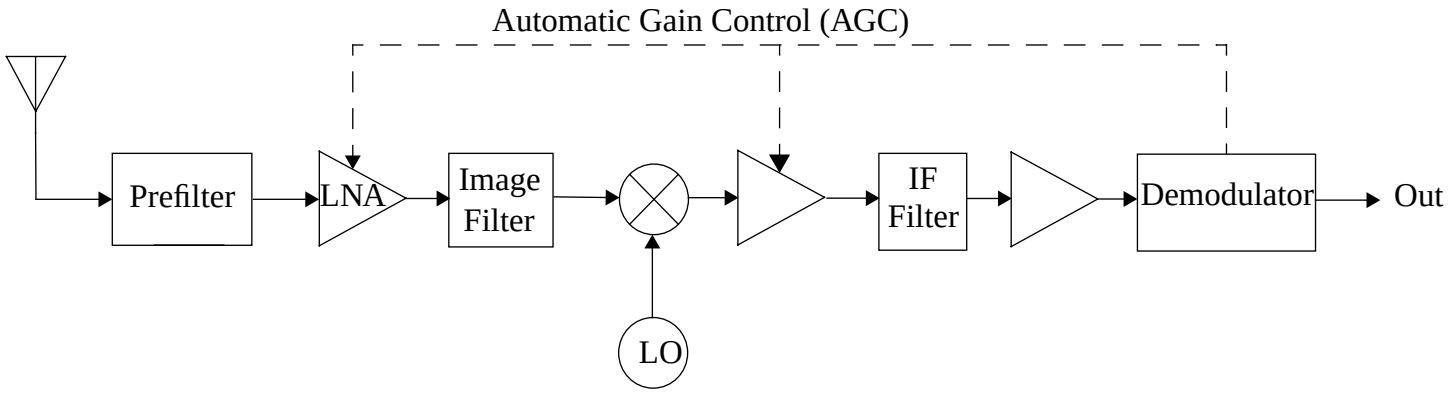


# REVIEW OF SOME ON-CHIP FILTER RESEARCH PROGRESS

- On-Chip Image-Reject Filters - Mustafa Koroglu
- Improved Memory Cells for Switched-Current Filters - Ganesh Balachandran
- Low Power Baseband Filters - Zhiwei Dong
- Tuning Algorithms for Continuous Time Filters - Tien Pham

**Superheterodyne Receivers**

# Superheterodyne Receiver Architecture




- **Prefilter** Low NF : Its NF directly adds to the overall NF

  High DR : > DR of incoming signals

- **Image Filter** NF requirement relaxed (LNA)

  DR requirement relaxed too if AGC techniques are employed

- **IF Filter** High Q

**Superheterodyne Receivers**

# Challenges & Advantages

- **Noise, linearity, dynamic range** (general RF considerations)
- **Image problem**

  The higher the IF frequency, the more image suppression

- **Channel Filtering**

  High Q off-chip bandpass filters used (integrated filter are noisy)

  The higher the IF frequency, the higher the Q

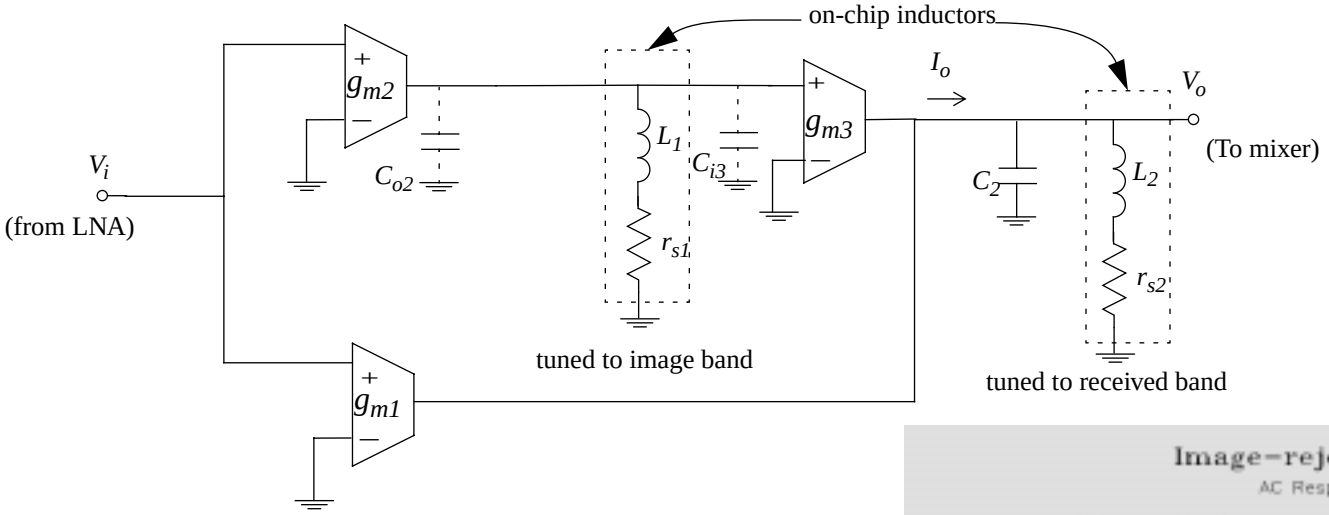
- **Trade-off between Image-rejection and channel selection!**
- **No DC offset problem**

  DC offset removed by ac coupling. Very robust to LO feedthrough second order nonlinearity effects that can result in dc offset.

- **Flicker noise less harmful**

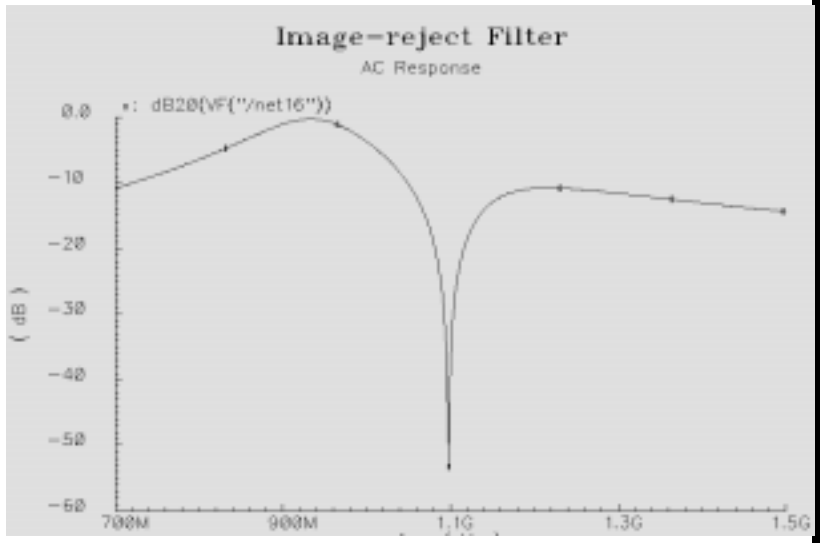
**On-chip Image-reject Filters**

# Image-reject Filters using on-chip Spiral Inductors




$$\frac{V_o}{V_i}(s) = g_{m1}\frac{sL_2 + r_{s2}}{s^2 L_2 C_2 + s r_{s2} C_2 + 1}\cdot\frac{s^2 + \left(\frac{r_{s1}}{L} - \frac{G}{C_1}\right)s + (1 - G r_{s1})/LC}{s^2 + \frac{r_{s1}}{L}s + \frac{1}{LC}}$$

$$G = \frac{g_{m2} g_{m3}}{g_{m1}}$$



**On-chip Image-reject Filters**

# Challenges & Benefits

- **Automatic tuning required**

  During TX, filter is converted to a VCO and using a PLL, VCO frequency is set to the desired reference frequency

  An amplitude-locked-loop is used to limit the oscillation amplitude by varying $g_{m3}$ to make sure small-signal behavior

- **No linearity degradation as in active bandpass filters**

  9dBm IP3 is simulated using 5.4 nH spiral inductors with Q of 6 and 6 mA total current consumption (BiCMOS 0.35um)

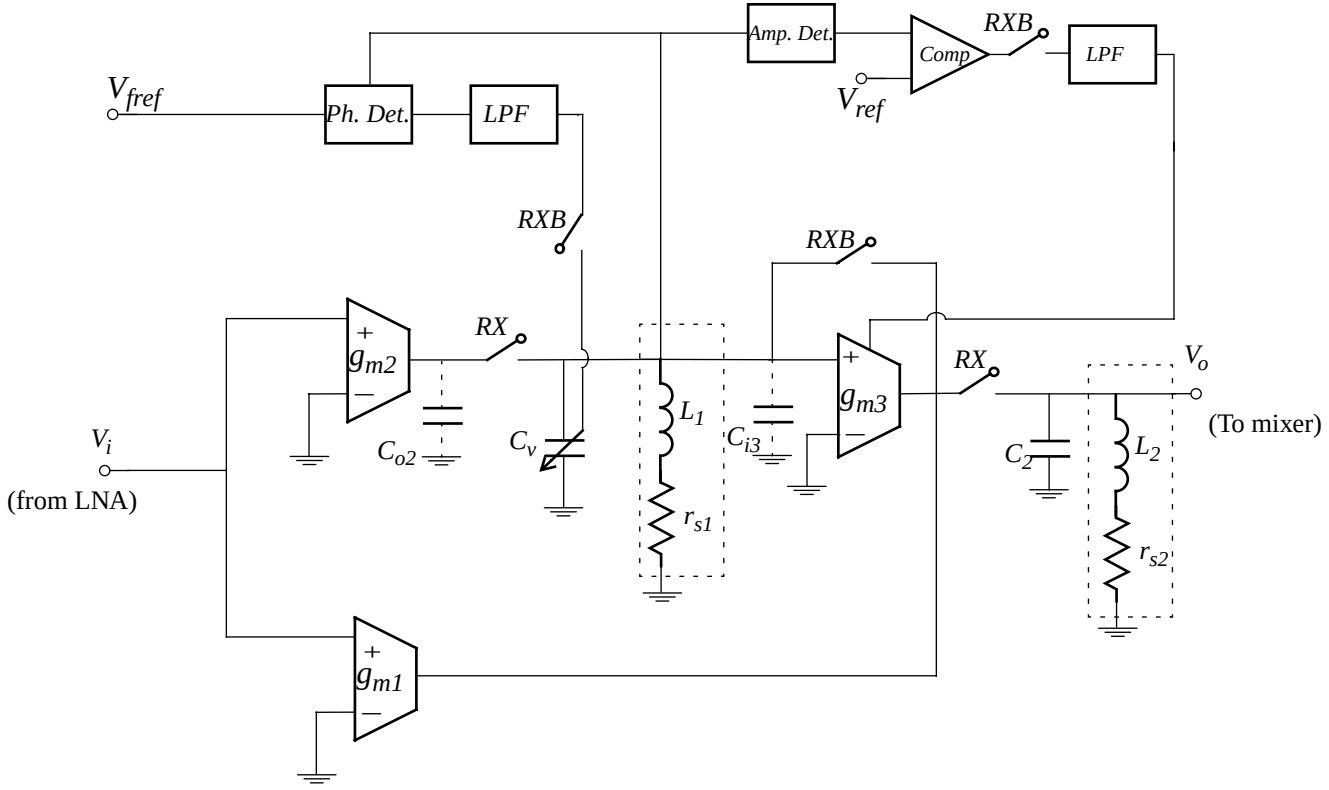
- **Image rejection limited by**

  matching between the transconductors $g_{m1}$ and $g_{m2}$ (for 40dB, 1% required)

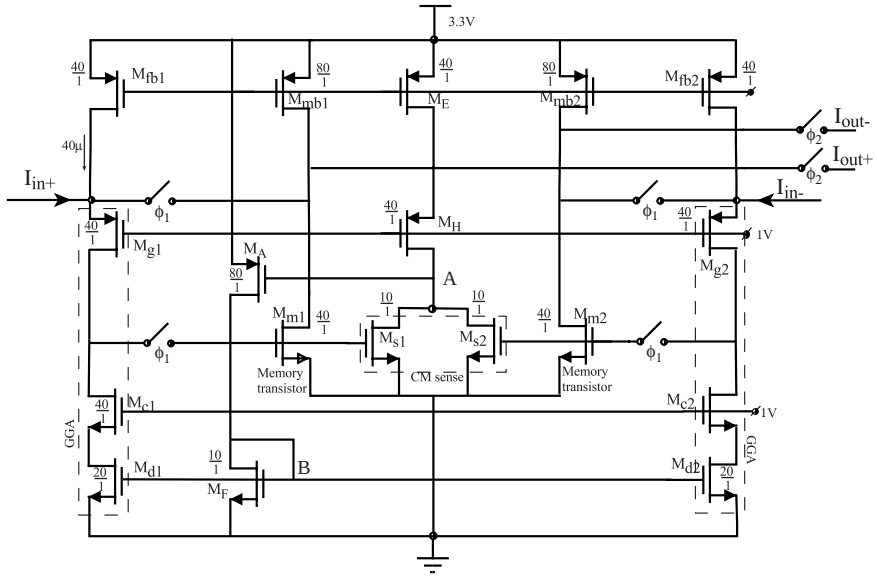
  width of the image band ( $IR \propto \Delta W_{image} / \omega_{image}$ )

**On-chip Image-reject Filters**

# Image-reject Filter with Tuning Circuitry



# Improved Memory Cells for Switched-Current Filters




A low-voltage fully differential memory cell

*G.K. Balachandran and P.E. Allen, Electronics Letters, Dec. 9, 1999.*

## *Research Emphasis*

- Design of memory cells with very low charge-feedthrough
- Development of Novel differential current-mode structures with common-mode feedback for low-voltage operation
- Develop new architectures for Switched-Current filters

# What affects integrator power dissipation?

The power dissipation equation is:

$$P = N \cdot \frac{Io}{Isignal} \cdot Vdd \cdot \sqrt{2DR} \cdot \sqrt{\overline{i^2_{total}}}$$

where Io is the bias current of the integrator, N is the number of the bias current of the integrator.
The power dissipation is determined by

1. Number of bias current N
2. The harmonic distortion HD,
3. Supplied voltage Vdd
4. Dynamic range DR
5. Noise power

# Switch Capacitor Integrator

The transfer function of the SC integrator is:

$$\frac{d}{dt}Vout = \frac{C1}{T \cdot C2}Vin$$

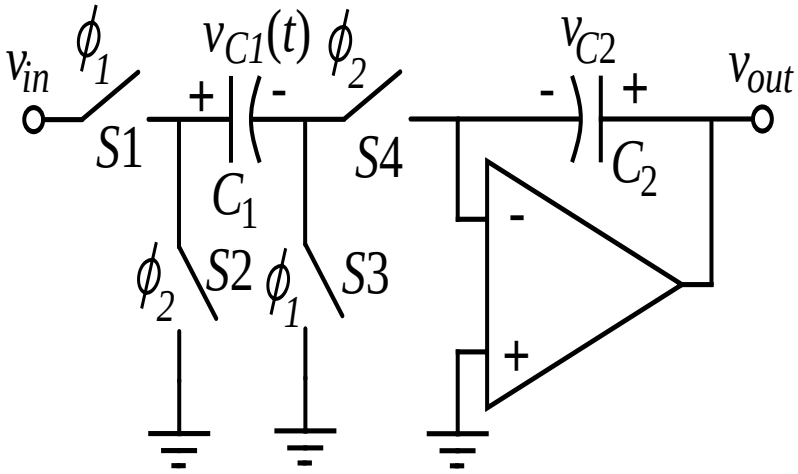



Figure 2

Advantages:

1. Tunable of clock frequency 1/T,
2. Controllable of the ratio of C1 to C2.

The gain bandwidth of the amplifier is:

$$GB = \frac{2}{HD} \cdot (s + \omega a)$$

where HD is the harmonic distortion and $\omega a$ is the 3dB frequency of the op amp.

If HD=1/100 and s= $\omega a$ =1MHz, we can get GB=0.4GHz, Avd(0)=400. For the operational amplifier with this performance, the power dissipation is around the 10mW level. This power dissipation is too large for a low power filter.

Therefore the SC integrator is not suitable for low power high frequency filters.

# Gm-C Integrator

The transfer function of the Gm-C integrator is:

$$\frac{d}{dt}Vout = \frac{Gm}{C}Vin;\left(Gm = \frac{1}{2}K\frac{W}{L}(Von1 + Von2)\right)$$

where Von is the gate source voltage Vgs minus threshold voltage Vt.

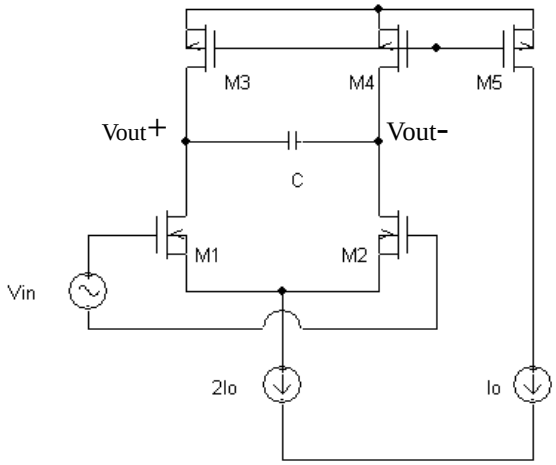



Figure 3

Advantages:

1. it is Simple 2. It can work over a large frequency range.

The power dissipation of this circuit as follows:

$$P = 3 \cdot Io \cdot Vdd = \frac{4 \cdot V_T \cdot q \cdot K \cdot \frac{W}{L} \cdot DR}{\pi \cdot C \cdot HD}Vdd$$

Let f=1MHz, C=10pF,W/L=5, DR=60DB, HD=1/100, Vdd=2V and K=110uS/V, the power dissipation of this integrator can be resulted 58.3uW. The power level of the filter made up by this kind of integrator is about 0.5mW, it is too large for a low power filter.

# Log Domain Integrator

The transfer function of Log Domain Integrator is:

$$\frac{di_{out}}{dt} = \frac{Io}{C \cdot V_T} \cdot (i_{in} - i_{out})$$

The power dissipation equation of the integrator can be resulted

$$P = 12 \cdot (\beta + 2B + 1) \cdot q \cdot f \cdot Vdd \cdot DR$$

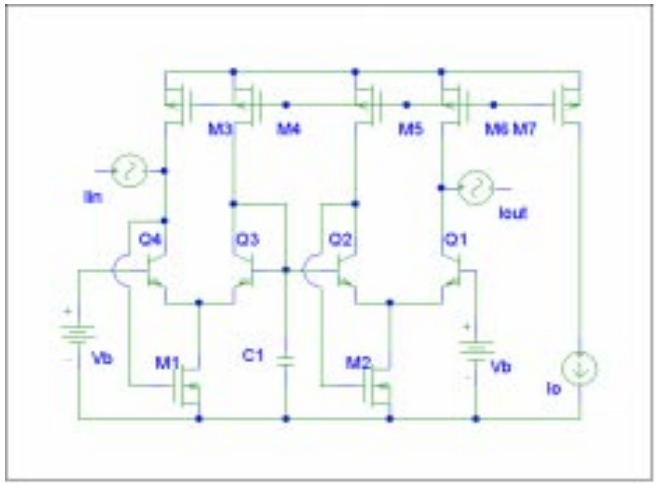



Figure 4

where B=rb*Gm, rb is the base resistor and Gm is the transconductance of the bipolar transistor.

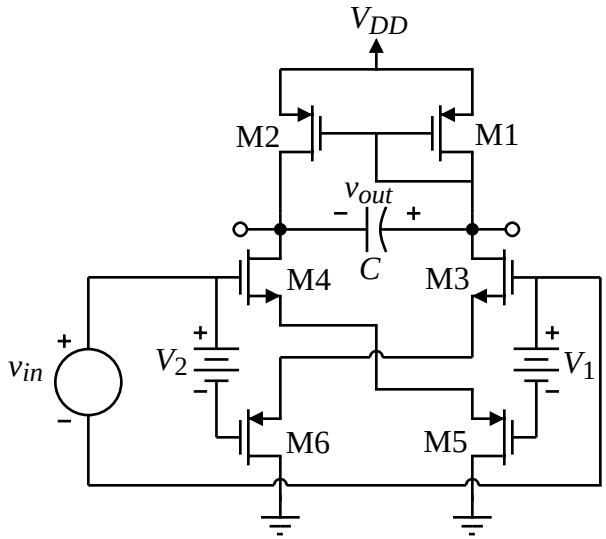
For f=1MHz, DR=60DB, Vdd=2V, B=0.5 and $\beta$ =2, the power dissipation is 15.4 uW.

The power dissipation of the log-domain integrator is smaller than the Gm-C integrator when the current gain of bipolar transistor is small. But normally the bipolar transistor performance is poor when its current gain is small.

## Constant $G_m$-C Integrator

Linearization of transconductance ⇒ Decreased harmonic distortion ⇒ Decreased power dissipation for the same dynamic range

Linear Transconductance Integrator:




The transfer function of the integrator is

$$\frac{dv_{out}}{dt} = \frac{g_m}{C} v_{in}$$

For this circuit the transconductance is given by,

$$g_m = 2 \cdot \frac{\frac{K_N W}{L}}{A+1+2\cdot\sqrt{A}} (V_{bias} - V_{TN} - |V_{TP}\})$$

where $A$ is defined from

$$\frac{K_N W_N}{L_N} = A\left(\frac{K_P W_P}{L_P}\right)$$

It can be shown that $g_m$ is constant with *vin*

# The power dissipation analysis of a constant Gm-C integrator

There is very little harmonic distortion for this integrator, Isignal = Io. The dynamic range equation is given by:

$$DR = \frac{\frac{1}{2} i_{signal}^2}{i_{total}^2} = \frac{\frac{1}{2} i_o^2}{i_{total}^2} = \frac{\pi \cdot C \cdot Von^2}{24 \cdot V_T \cdot q} = \frac{\pi \cdot C \cdot Io}{16 \cdot V_T \cdot q \cdot K \cdot \frac{W}{L}}$$

and the power dissipation of this integrator as:

$$P = Itotal \cdot Vdd = 3 \cdot Io \cdot Vdd = \frac{48 \cdot V_T \cdot q \cdot K \cdot \frac{W}{L} \cdot DR}{\pi \cdot C} Vdd$$

Let f=1MHz, C=10pF, W/L=5, DR=60DB, Vdd=2V and K=110uS/V, the power dissipation is 7.0uW.

The power dissipation is about one-eighth of the Gm-C integrator and about one-half of the log-domain integrator.

# Comparison of these four kinds of integrators

Let f=1MHz, C=10pF,W/L=5, DR=60DB, HD=1/100, Vdd=2V, $\beta$ =2 and B=0.5 K=110uS/V, and from the power dissipation equations of the Gm-C, the log domain and the constant Gm-C integrator, we get the power dissipation of 58.3uW, 15.4uW and 7.00uW respectively, shown on the following table.

**Table 1: Comparison of these four kinds of integrators**

| Integrator | Transfer equation | Dynamic range equation | Power dissipation equation | Power Dissipation |
|---|---|---|---|---|
| Switch Capacitor | $\frac{d}{dt}Vout = \frac{C1}{T \cdot C2} A \bullet Vin$ | ---------- | ---------- | 10mW |
| Gm-C | $\frac{d}{dt}Vout = \frac{Gm}{C}Vin$ | $DR = \frac{3 \cdot \pi \cdot C \cdot THD \cdot Io}{4 \cdot V_T \cdot q \cdot K \cdot \frac{W}{L}}$ | $P = \frac{4 \cdot V_T \cdot q \cdot K \cdot \frac{W}{L} \cdot DR}{\pi \cdot C \cdot THD} Vdd$ | 58.3uW |
| Log Domain | $\frac{di_{out}}{dt} = \frac{Io}{C \cdot V_T} \cdot (i_{in} - i_{out})$ | $DR = \frac{\pi \cdot C \cdot V_T}{2 \cdot q \cdot (\beta + 2B + 1)}$ | $P = 12 \cdot (\beta + 2B + 1) \cdot q \cdot \Delta f \cdot Vdd \cdot DR$ | 15.4 uW |
| Constant Gm-C | $\frac{d}{dt}Vout = \frac{Gm}{C}Vin$ | $DR = \frac{\pi \cdot C \cdot Io}{16 \cdot V_T \cdot q \cdot K \cdot \frac{W}{L}}$ | $P = \frac{48 \cdot V_T \cdot q \cdot K \cdot \frac{W}{L} \cdot DR}{\pi \cdot C} Vdd$ | 7.00uW |

Besides power dissipation, we should consider other aspects of integrator performance for filter design. The following table summarizes the advantages and disadvantages of these four kinds of integrators. From the table, we can also see the constant Gm-C is the best choice for low power dissipation.

**Table 1: Advantages and Disadvantages of Integrators**

| Integrator Form | Advantages | Disadvantages |
|---|---|---|
| Switch Capacitor | 1. Tunable of the cutoff frequency (by changing the sampling frequency)<br>2. Precisely controllable the ratio of C1 to C2 | 1. Harmonic distortion.<br>2. Low frequency range(<500khz)<br>3. Large chip area, |
| Gm-C | 1. Simple circuit.<br>2. Small chip area<br>3. Wide frequency range. | 1. Harmonic distortion.<br>2. Large power dissipation |
| Log Domain | 1. No harmonic distortion<br>2.Wide frequency range.<br>3. Low power dissipation | 1. High noise floor.<br>2. Cutoff frequency changed with temperature .<br>3. Can not be made by CMOS process.<br>4. Low current gain |
| Constant Gm-C | 1. No harmonic distortion.<br>2. Wide frequency range.<br>3. Low noise floor.<br>4. Low power dissipation | 1. Voltage shiftcircuit.<br>2. Higher supplied voltage. |

Figure 9, shows the comparison of the filters made in the past three years. The number in the figure is the number of reference. Because the power dissipation is linear with the order of filter, and increases with the cutoff (or center) frequency, then for a fair comparison, we let log(power/(order*cutoff frequency)) as the vertical axis, and dynamic range as the horizontal axis. Three integrators analyzed in this report are also shown in the figure as 'news'. From the figure, we can find that constant Gm-C filters dissipates at the lowest power. And switch capacitor filters and Gm-C filters are at the same power dissipation level.

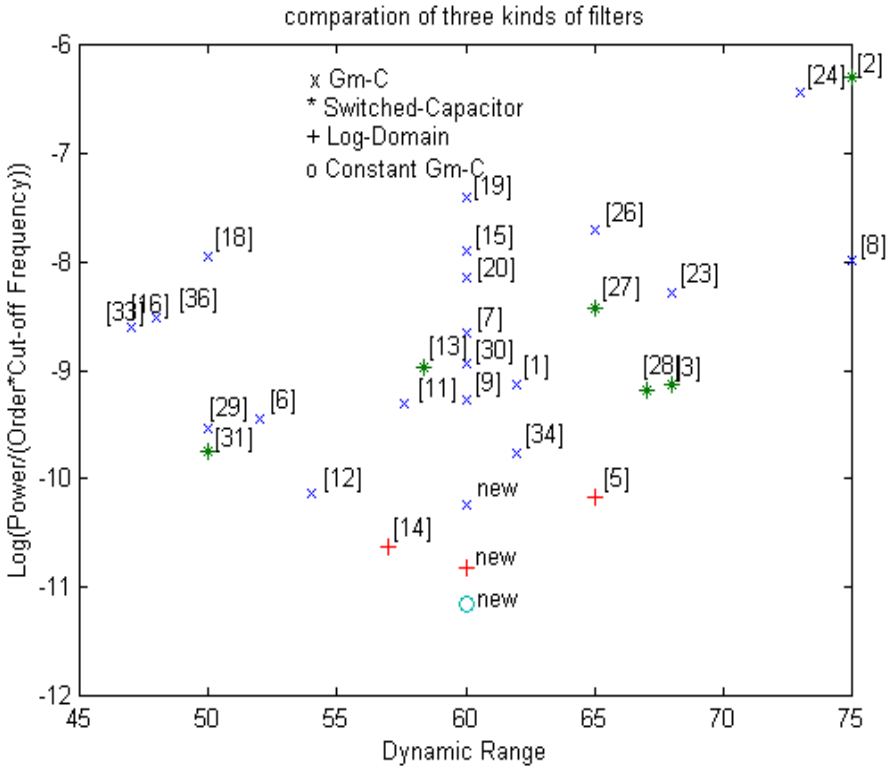
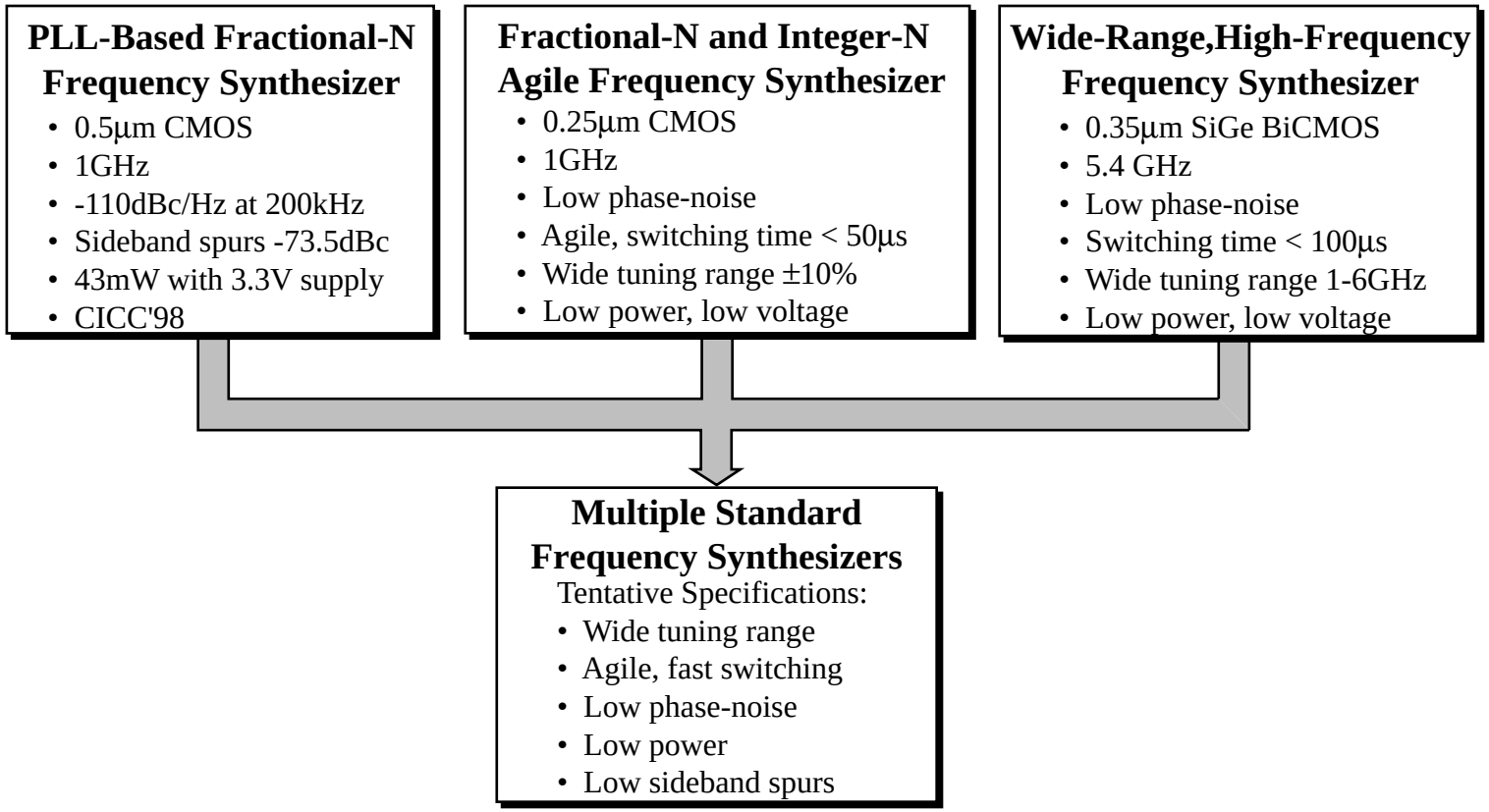



Figure 9

# HIGH PERFORMANCE FREQUENCY SYNTHESIZERS

(Frequency Synthesizers for Programmable Radios)

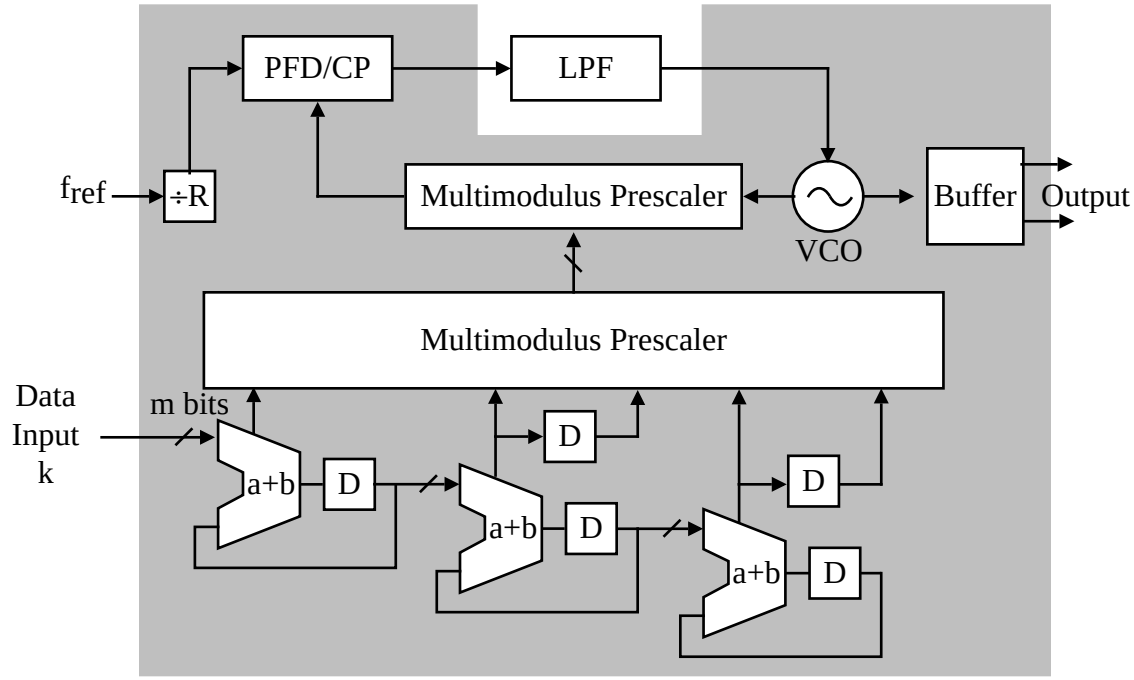


## Frequency Synthesizer Research Efforts

- **PLL-Based Fractional-N Frequency Synthesizer - Byeong-Ha Park**
- **Fractional-N and Integer-N Agile Frequency Synthesizer - Benyong Zhang**
- **Wide-Range, High-Frequency Frequency Synthesizer - Han-Woong Son**

## Low Phase-Noise Frequency Synthesizer

Fractional-N frequency synthesizer with a three-stage modulator.



# Experimental Results For The Low-Phase Noise Synthesizer

Measured Results:

| Proto-type | Close-in RMS noise | Phase noise @ 200KHz | Frequency Range | Reference Spurs | 2nd Harmonic | Settling Time | Loop BW | Power Dissipation |
|---|---|---|---|---|---|---|---|---|
| 1 | <2° | 110dBc/Hz° | 834-965MHz | < -71dBc | -24dBc | 172µs | 20kHz | 43mW@$V_{DD}$=3.3V |
| 2 | <2° | 110dBc/Hz° | 862-1004MHz | < -74dBc | -24dBc | 172µs | 20kHz | 43mW@$V_{DD}$=3.3V |

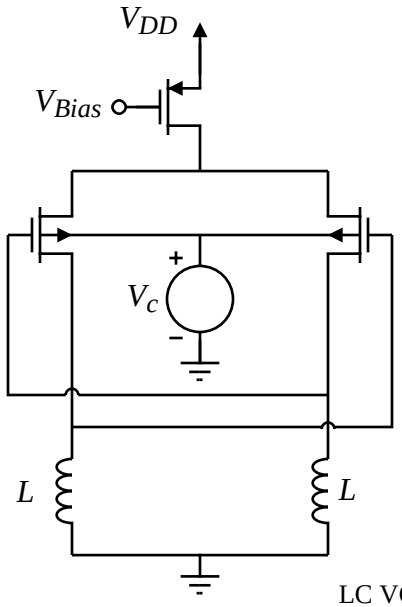
B. Park and P.E. Allen, "Low-Power, Low-Phase-Noise CMOS Voltage-Controlled-Oscillator with Integrated LC Resonator," *Proceedings of International Symposium on Circuits and Sytems*, May 31-June3, 1998, Paper MAA13-22, Monterey, CA.

## 2.4 GHz CMOS Frequency Synthesizer

A fractional-N and integer-N designs are being fabricated in 0.25μm CMOS

- Agile, fast frequency transition < 50μs
- Low power
- Uses a unique switched capacitor filter associated with the charge-pump

VCO using bulk tuning:




LC VCO

## Loop Filter Using Switched Capacitor Technique

The low pass filter in the PLL can be implemented by:

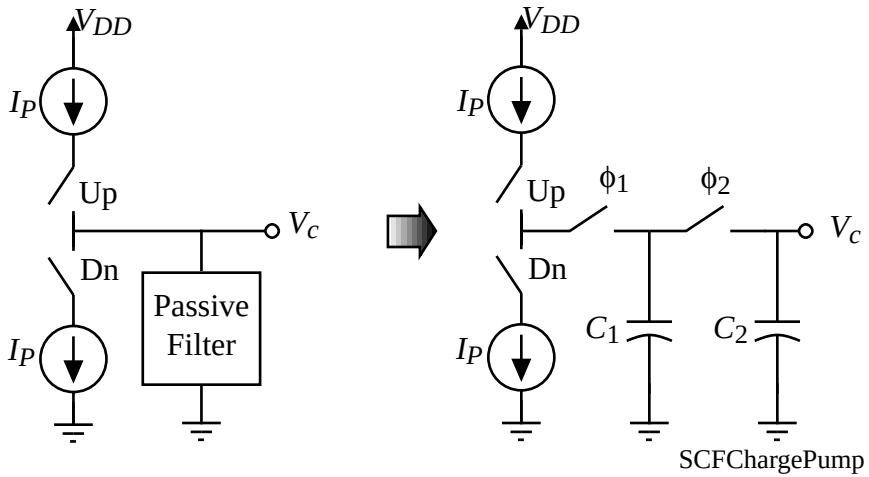
1.) Active filters which require an op amp

2.) Passive filters and a charge pump.

However, the passive filter components are generally off-chip.

A solution is to use switched capacitor techniques to achieve on-chip, quickly adjustable loop filters.

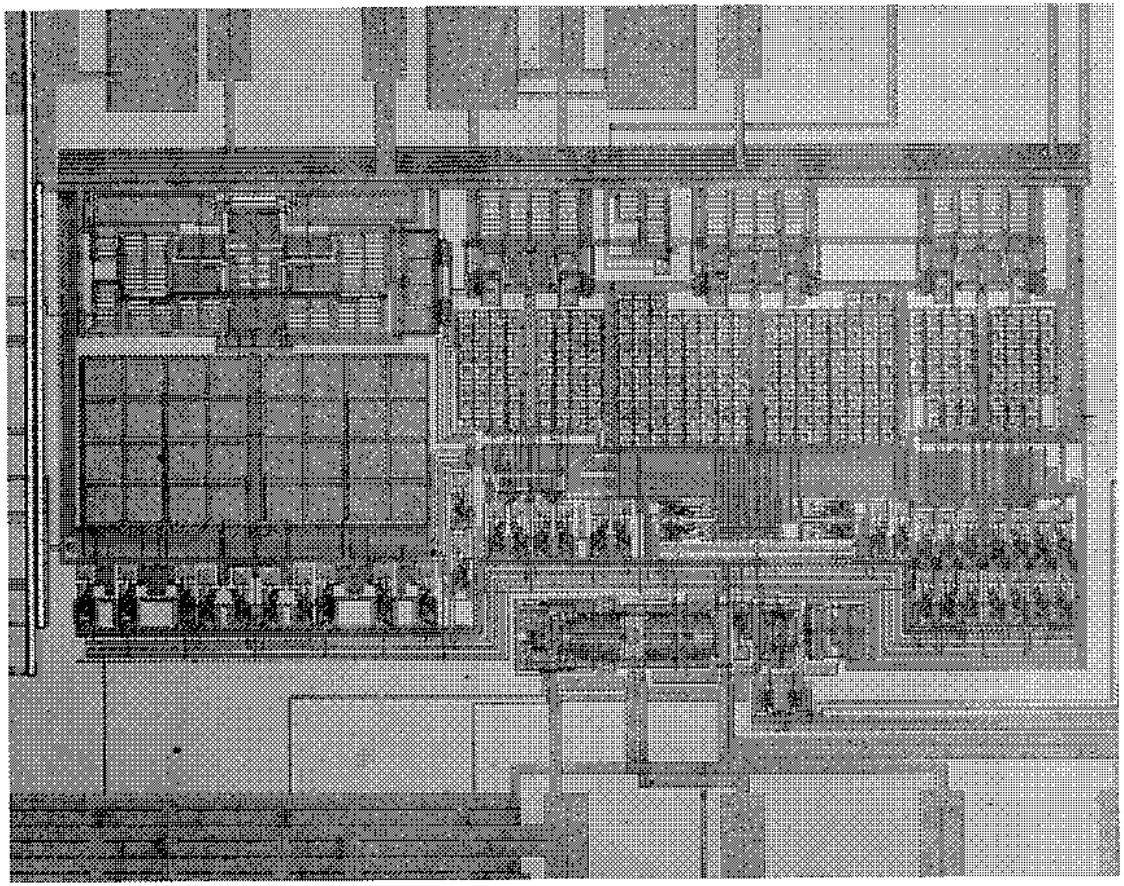
Concept:




$C_1$ and $C_2$ are on-chip components.

# 1.5V, 1mW, 98dB ΔΣ ANALOG-DIGITAL CONVERTER

Microphotograph of the experimental ΔΣ modulator.



# Measured 4th-Order ΔΣ Modulator Characteristics

Table 5.4

Measured fourth-order delta-sigma modulator characteristics

| Technology : 0.5 μm triple-metal single-poly n-well CMOS process | |
|---|---|
| Supply voltage | 1.5 V |
| Die area | 1.02 mm x 0.52 mm |
| Supply current | 660 μA |
| analog part | 630 μA |
| digital part | 30 μA |
| Reference voltage | 0.75V |
| Clock frequency | 2.8224MHz |
| Oversampling ratio | 64 |
| Signal bandwidth | 20kHz |
| Peak SNR | 89 dB |
| Peak SNDR | 87 dB |
| Peak S/D | 101dB |
| $HD_3$ @ -5dBv 2kHz input | -105dBv |
| DR | 98 dB |

A.L. Coban and P.E. Allen, "A 1.5V, 1mW Audio ΔΣ Modulator with 98dB Dynamic Range, "*Proc. of 1999 Int. Solid-State Circuits Conf.*, Feb. 1999, pp. 50-51.

# ON-CHIP POWER MANAGEMENT

Goal: Develop an on-chip power management scheme that provides optimum power for each block from a single, poorly regulated (battery) with all components on chip.

Requirements:

- Efficient
- Minimal area
- Compatible with standard digital CMOS technology

  Capacitors < 100pF

  Inductors < 10nH

Approach:

Power $\propto$ Component size x Frequency

1.) Reduce power to milliwatt level (many distributed converters)

2.) Increase the switching frequency (up to 100MHz)

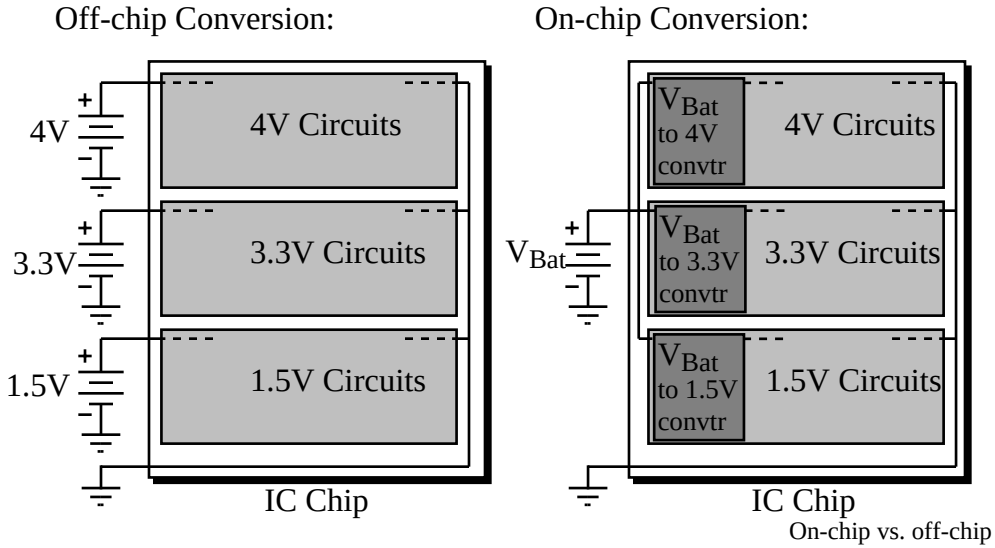
# Typical Power in a Telecom Chip

One-Watt, CMOS Telecom Chip:

| Function | Power | Voltage | Current | Regulation? |
|---|---|---|---|---|
| Micprocessor | 200mW | 1.5V | 133mA | Moderate |
| Memory | 250mW | 2V | 125mA | Moderate |
| Analog Front End | 200mW | 4V | 50mA | Yes |
| Baseband (SCF,A/D, D/A) | 100mW | 3.3V | 30mA | Yes |
| I/O Circuits | 100mW | 3.3 | 30mA | No |
| Digital (Filters, DSP, etc.) | 100mW | 1.5 | 67mA | Moderate |
| Power Control Ckts. | 50mW | 1-4V | - | - |

## Distribution of that Power

Off-chip conversion versus on-chip conversion

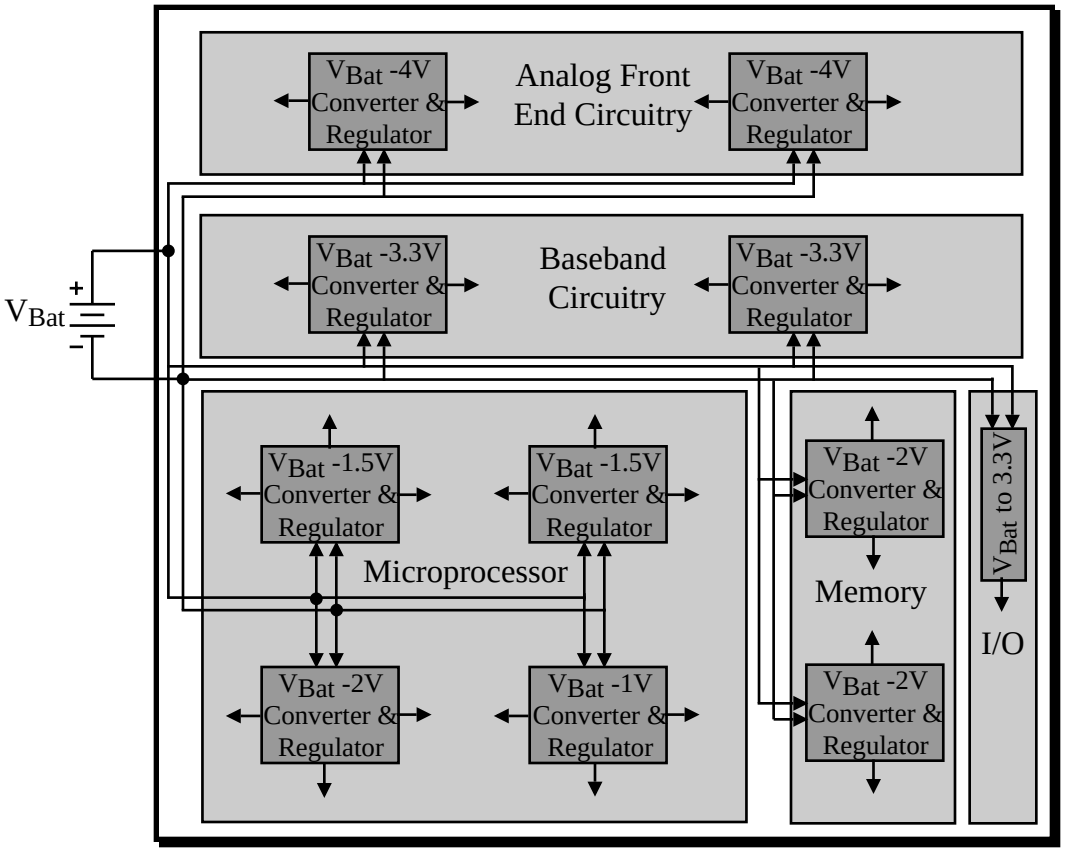



On-chip vs. off-chip

| Characteristic | Off-Chip Conversion | On-Chip Conversion |
|---|---|---|
| Regulation | Off chip | On chip |
| Noise Sensitivity | High | Low |
| $I^2R$ Losses | Reduces circuit voltage | No effect |
| Reliability | Poor - off-chip circuits | All connections on chip |
| System Flexibility | Poor | Changes can be made locally on chip |

# On-Chip Power Distribution

Example:

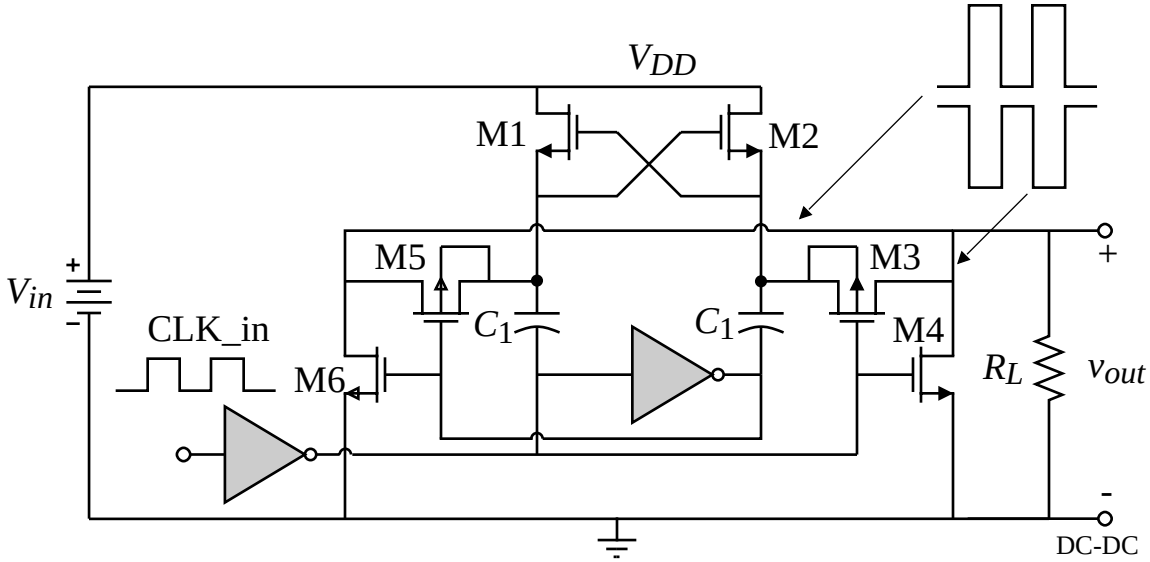



PwrDistScheme

- Conversion and regulation locally permits the noise on the power supply busses to be eliminated.
- Reduces the amount of external connections required for power supplies which permits lower inductance and resistance connections using multiple bonding wires.

# On-Chip DC-DC Converter

Simplified Circuit:




Performance (Simulated):

- Efficiency ≈ 75%
- Frequency of clock = 5Mhz
- Power out = 5mW
- Output voltage ≈ 2xInput
- Output ripple ≈ 20% (spike during switching)
- Capacitor values are 300pF and are MOS capacitors (will use fringing capacitors in next version)

# RECENT PUBLICATIONS

1. G.A. Rincon-Mora and P.E. Allen, "A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator," *J. of Solid-State Circuits*, Vol. 33, No. 1, January 1998, pp. 36-44.

2. G.A. Rincon-Mora and P.E. Allen, "Optimized Frequency-Shaping Circuit Topologies for LDO's," *Trans. on Circuits and Systems-II*, Vol. 45, No. 6, June 1998, pp. 703-708.

3. B.J. Blalock, P.E. Allen, and G.A Rincon-Mora, "Designing 1-V Op Amps Using Standard Digital CMOS Technology," *Trans. on Circuits and Systems-II*, vol. 45, no. 7, July 1998, pp. 769-780.

4. G.A. Rincon-Mora and P.E. Allen, "A 1.1-V Current-Mode and Piecewise-Linear Curvature-Corrected Bandgap Reference," *J. of Solid-State Circuits*, vol. 33, no. 10, October 1998, pp. 1551-1554.

5. B. Park and P.E. Allen, "1 GHz, low-phase noise CMOS frequency synthesizer with integrated LC VCO for wireless communications," *Proceedings of CICC*, May 1998, pp. 567-570.

6. A.L. Coban and P.E. Allen, "A 1.5V, 1mW Audio $\Delta\Sigma$ Modulator with 98dB Dynamic Range, *Proc. of 1999 Int. Solid-State Circuit Conf.*, Feb. 1999, pp. 50-51.

7. G.K. Balachandran and P.E. Allen, "A Low-Voltage, Fully-Differential, Switched-Current Memory Cell", *Electronic Letters*, Vol. 35, No. 25, Dec. 1999, pp. 2200-2201.

# SUMMARY

- EDA
  - Converting from quarter to semester system
  - New faculty member - Prof. Steve Kenney, ON Semiconductor Jr. Professor
  - Looking for two more faculty members in analog area
- 13 Ph.D students and 2 MS students
- Program focus is on wireless applications suitable for wide range applications
- Emphasis of the research is:
  - On-chip RF, IF, and baseband filters
  - High performance frequency synthesizers
- Working closely with Prof. Joy Laskar to develop system solutions to:
  - Bluetooth 28 dBm specification in CMOS technology
  - IEEE 802 WLAN specifications in SiGe technology