FINAL EXAMINATION

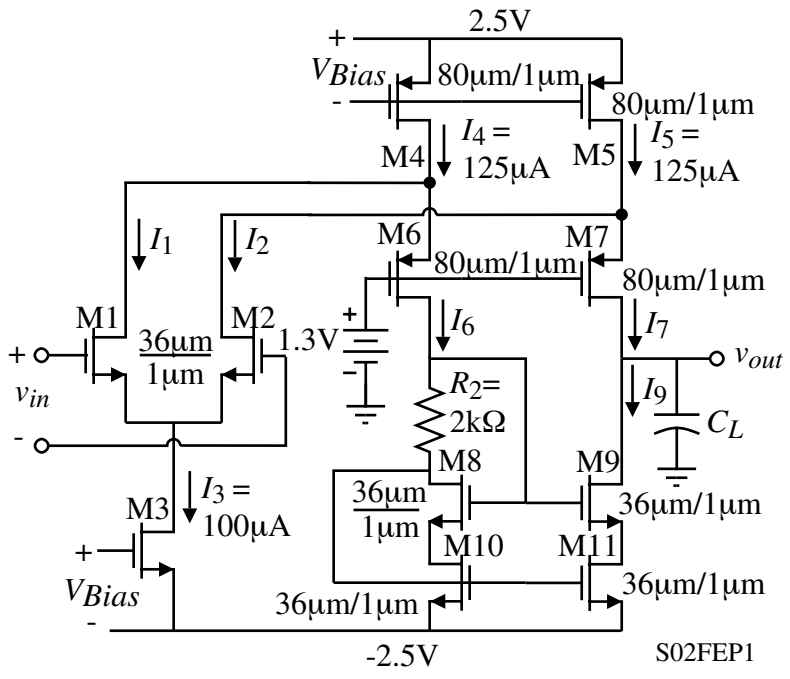
NAME_____SCORE_____/120

Problem	①	②	3	4	5	6	7	8
Score								

INSTRUCTIONS: This exam is closed book with four sheets of notes permitted. The exam consists of 8, 20-point problems of which you are to work only 6 for a total of 120 points. You must attempt problems 1 and 2. All other problems are optional. **Please circle the number in the table above of the remaining three problems you wish graded.** If you do not indicate the problems to be graded, then problems 1 through 6 will be graded regardless of whether they are worked or not. Be sure to turn in only the 6 problems you wish graded in proper numerical order. Please show your work leading to your answers so that maximum partial credit may be given where appropriate.

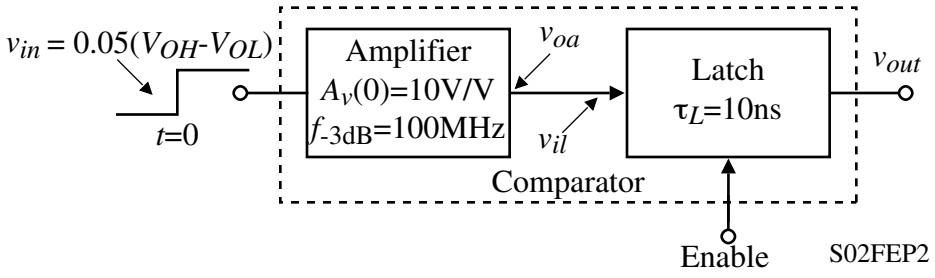
Problem 1 - (20 points - This problem is required)

If the folded-cascode op amp shown having a small-signal voltage gain of 7464V/V is used as a comparator, find the dominant pole if C_L = 5pF. If the input step is 10mV, determine whether the response is linear or slewing and find the propagation delay time. Assume the parameters of the NMOS transistors are K_N'=110V/μA^2, V_{TN} = 0.7V, λ_N=0.04V^{-1} and for the PMOS transistors are K_P'=50V/μA^2, V_{TP} = -0.7V, λ_P=0.05V^{-1}.



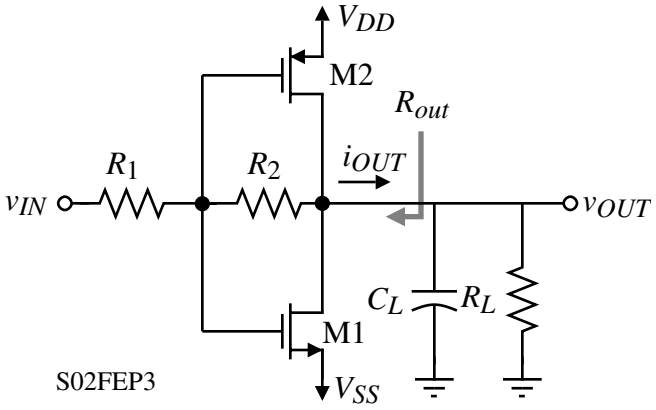
Problem 2 - (20 points - This problem is required)

A comparator consists of an amplifier cascaded with a latch as shown below. The amplifier has voltage gain of 10V/V and $-f_{-3dB}$ = 100MHz and the latch has a time constant of 10ns. The maximum and minimum voltage swings of the amplifier and latch are V_{OH} and V_{OL}. When should the latch be enabled after the application of a step input to the amplifier of $0.05(V_{OH}-V_{OL})$ to get minimum overall propagation time delay? What is the value of the minimum propagation time delay? It may useful to recall that the propagation time delay of the latch is given as $t_p = \tau_L \, ln\left(\frac{V_{OH}-V_{OL}}{2v_{il}}\right)$ where v_{il} is the latch input (ΔV_i of the text).

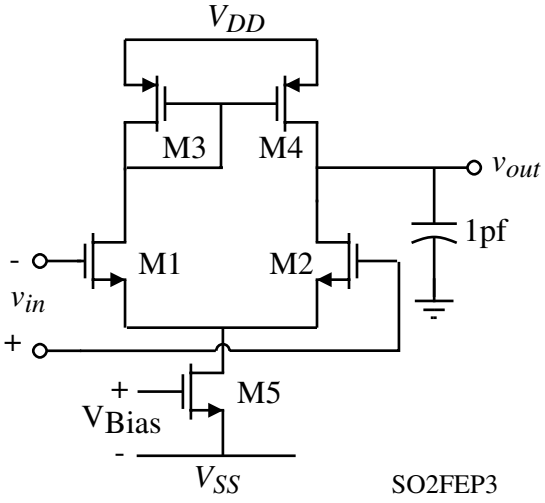


Problem 3 - (20 points - This problem is optional)

If $R_1 = R_2$ of the circuit shown, find an expression for the small-signal output resistance R_{out} ignoring R_L. Repeat including the influence of R_L on the output resistance. Let R_1=R_2 and R_L = 1kΩ, dc currents through M1 and M2 be 500μA, W_1/L_1 = 100μm/1μm and W_2/L_2 = 200μm/1μm. Find the value of R_{out}. Assume the parameters of the NMOS transistors are K_N'=110V/μA^2, V_{TN} = 0.7V, λ_N=0.04V^{-1} and for the PMOS transistors are K_P'=50V/μA^2, V_{TP} = -0.7V, λ_P=0.05V^{-1}. Assume that R_2>>r_{ds1} or r_{ds2}.



Problem 4 - (20 points - This problem is optional)

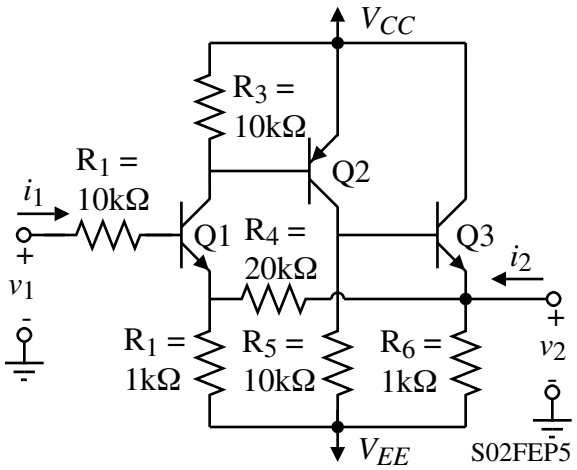


SO2FEP3

A current mirror load, CMOS differential amplifier is shown. The current in M5 is 100μA. Assume the parameters of the NMOS transistors are K_N' =110V/μA^2, V_{TN} = 0.7V, λ_N =0.04V^{-1} and for the PMOS transistors are K_P' =50V/μA^2, V_{TP} = -0.7V, λ_P =0.05V^{-1}. (a.) Find the small-signal output resistance and voltage gain if the W/L ratio of M1 and M2 is 100μm/1μm. (b.) If the W/L ratio of M3 and M4 is 50μm/1μm and C_{ox} = 24.7x10^{-4}F/m^2, and the effective output capacitance is 1pF, find all roots of this amplifier (ignore the influence of C_{gd4}). Ony include the capacitors in this problem that you can calculate from the information given. (c.) What is the –3dB frequency in Hertz?

Problem 5 - (20 points - This problem is optional)

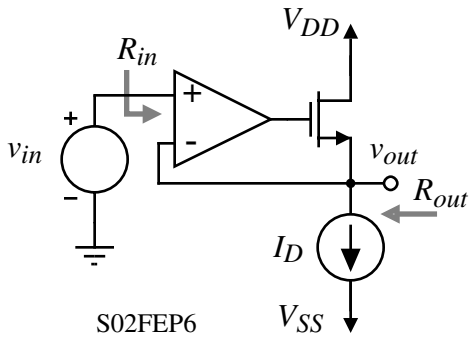
The simplified schematic of a feedback amplifier is shown. Use the method of feedback analysis to find v_2/v_1, $R_{in} = v_1/i_1$, and $R_{out} = v_2/i_2$. Assume that all transistors are matched and that $\beta = 100$, $r_\pi = 5\text{k}\Omega$ and $r_o = \infty$.



Problem 6 - (20 points - This problem is optional)

A voltage follower feedback circuit is shown. For the MOS transistor, I_D = 0.5mA, K' = 180μA/V^2, $r_{ds} = \infty$, and W/L = 100. Although, the bulk effect should be considered, g_{mbs}, for simplicity ignore the bulk effects in this problem. For the op amp, assume that R_i = 1MΩ, R_o = 10kΩ, and a_v = 1000. Calculate the input resistance and output resistance using Blackman's formula given below.

$$R_{out} = R_{out}\,(\text{Controlled source} = 0)\left[\frac{1 + RR(\text{output port shorted})}{1 + RR(\text{output port open})}\right]$$

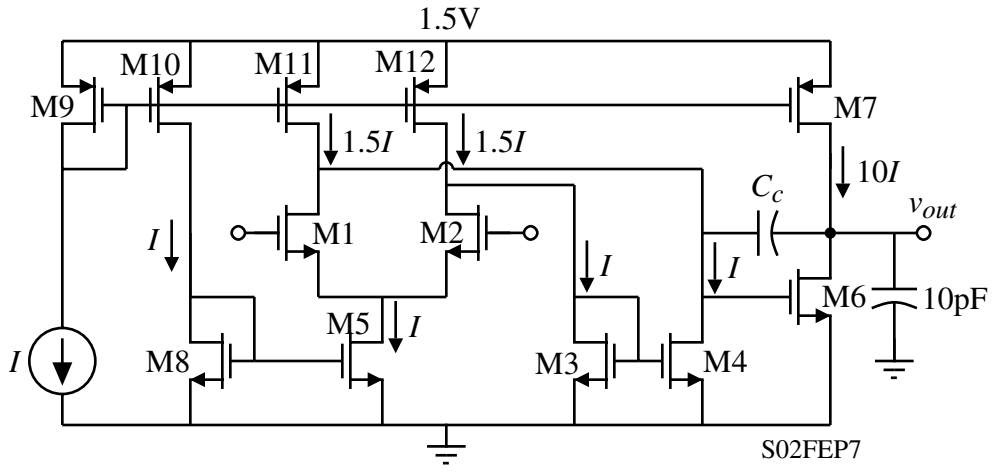


S02FEP6

Problem 7 – (20 points – This problem is optional)

A CMOS op amp capable of operating from 1.5V power supply is shown. All device lengths are 1μm and are to operate in the saturation region. Design all of the W values of every transistor of this op amp to meet the following specifications.

Slew rate = ±10V/μs	V_{out}(max) = 1.25V	V_{out}(min) = 0.75V
V_{ic}(min) = 1V	V_{ic}(max) = 2V	GB = 10MHz
Phase margin = 60° when the output pole = 2GB and the RHP zero = 10GB. Keep the mirror pole ≥ 10GB (C_{ox} = 0.5fF/μm^2).		

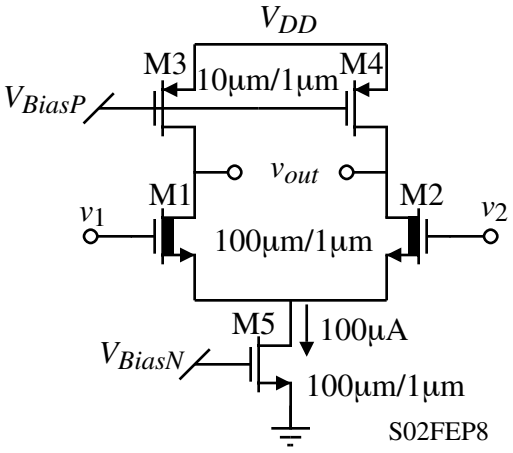


Your design should meet or exceed these specifications. Ignore bulk effects in this problem and summarize your W values to the nearest micron, the value of C_c(pF), and I(μA) in the following table. Use the following model parameters: K_N'=24μA/V^2, K_P' = 8μA/V^2, V_{TN} = - V_{TP} = 0.75V, λ_N = 0.01V^{-1} and λ_P = 0.02V^{-1}.

C_c	I	$W1=W2$	$W3 = W4$	$W5 = W8$	$W6$	$W7$	$W9 = W10$	$W11 = W12$	P_{diss}

Problem 8 – (20 points – This problem is optional)

A differential CMOS amplifier using depletion mode input devices is shown. Assume that the normal MOSFETs parameters are K_N' =110V/μA^2, V_{TN} = 0.7V, λ_N =0.04V^{-1} and for the PMOS transistors are K_P' =50V/μA^2, V_{TP} = -0.7V, λ_P =0.05V^{-1}. For the depletion mode NMOS transistors, the parameters are the same as the normal NMOS except that V_{TN} = -0.5V. (a.) What is the maximum input common-mode voltage, V_{icm}^+(max)? (b.) What is the minimum input common-mode voltage, V_{icm}^-(min)? (c.) What value of V_{DD} gives an $ICMR = 0.5V_{DD}$?



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