Homework Assignment No. 1

This homework assignment is due in class on Monday, January 13, 2003.

The following transistor parameters should used unless otherwise stated.

MOSFETS

MOSFET Parameter	n-channel	p-channel	units
K'	24	8	$\mu A/V^2$
V_{T0}	0.75	-0.75	V
γ	0.8	0.4	$V^{0.5}$
ϕ	0.6	0.6	V
λ	0.01	0.02	V^{-1}

C_{ox} = 0.7fF/μm^2 LD(NMOS) = 0.45μm LD(PMOS) = 0.6μm

n^+ diffusion to p-well (junction, bottom) = 0.33fF/μm^2
n^+ diffusion sidewall (junction, sidewall) = 0.9fF/μm
p^+ diffusion to substrate (junction, bottom) = 0.38fF/μm^2
p^+ diffusion sidewall (junction, sidewall) = 1.0fF/μm
n-channel to bulk (junction, bottom) = 0.1fF/μm^2
n-channel to bulk (junction, sidewall) = 0.3fF/μm
p-channel to bulk (junction, bottom) = 0.1fF/μm^2
p-channel to bulk (junction, sidewall) = 0.3fF/μm

BJTS

BJT Parameter	NPN	PNP (lateral)	units
ß	100	50	A/A
V_t	26	26	mV
I_S	10	10	fA
ϕ_B	0.8	0.8	V
V_{AF}	100	50	V

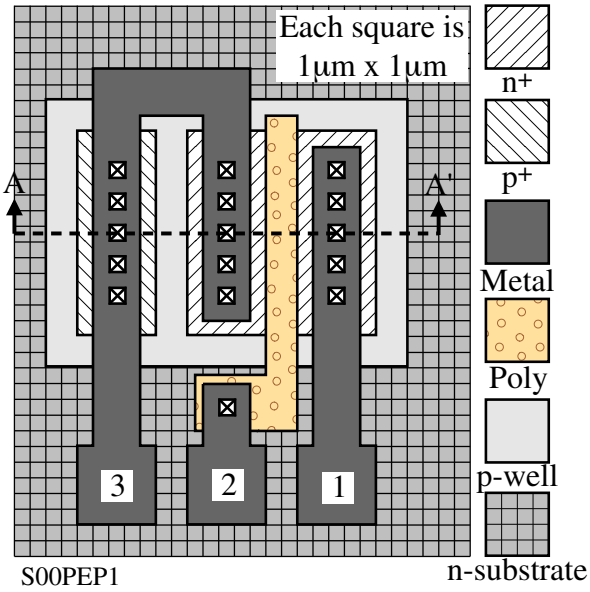
	C_{jE0}	C_{jC0}	C_{jS0}	n	ϕ_B	t_F
Vertical NPN	100fF	1000fF	2000fF	0.5	0.8V	0.5ns
Lateral PNP	80fF	500fF	2000fF	0.5	0.8V	5ns

Problem 1 - (10 points)

A top view of a MOS transistor is shown. (a) Identify the type of transistor (NMOS or PMOS) and its value of W and L.

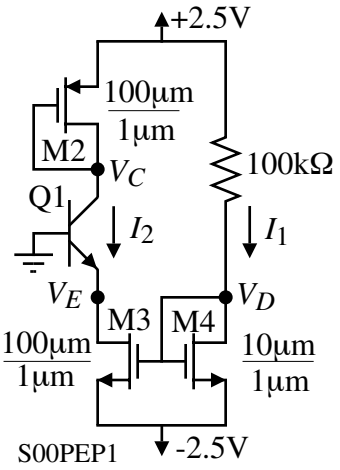
(b.) Draw the cross-section A-A' approximately to scale.

(c) Assume that dc voltage of terminal 1 is 5V, terminal 2 is 3V and terminal 3 is 0V. Find the numerical value of the capacitance between terminals 1 and 2, 2 and 3, and 1 and 3. Assume that the voltage dependence for pn junction capacitances is -0.5 (this is called MJ in SPICE).



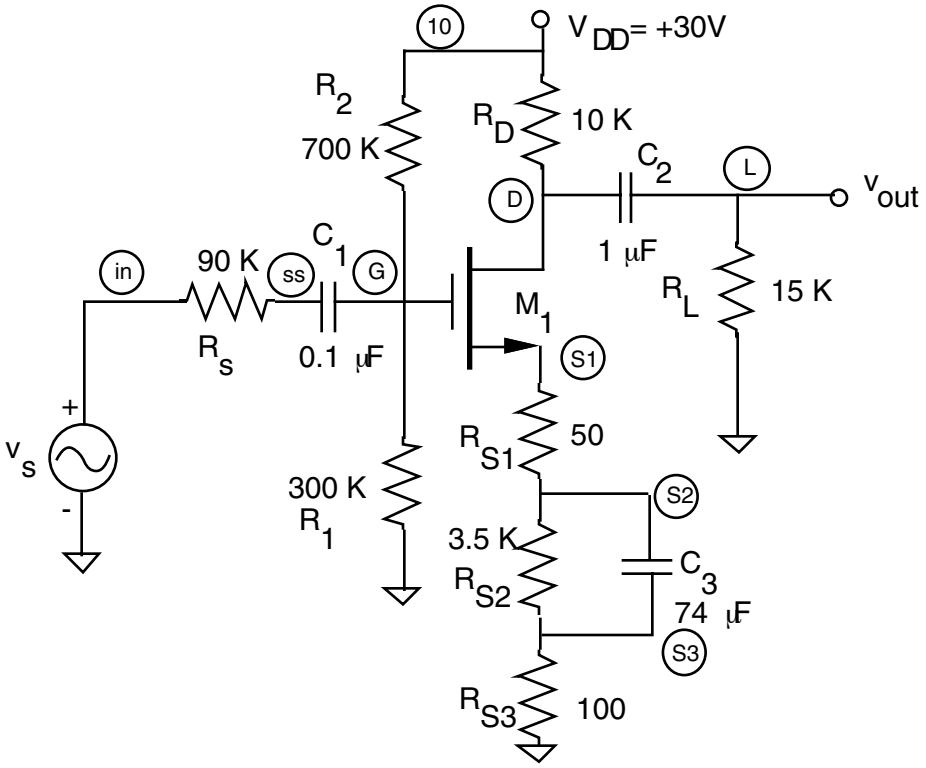
Problem 2 - (10 points)

Find the numerical values of I_1, I_2,V_D, V_E, and V_C to within ±5% accuracy.



Problem 3 - (10 points)

The circuit shown in the figure was simulated with SPICE using the indicated input control file. (The circled numbers and letters are node labels used in the simulation). The results from the output file after simulation of the dc analysis are given after the figure. You are required to draw the small-signal equivalent circuit that you would use to calculate the mid band voltage gain from the signal source to the indicated output. You are not required to perform any gain calculations – just draw and simplify the equivalent circuit that you could actually use to determine the mid band voltage gain. Indicate numerical values on all circuit elements. You may assume that the signal frequency of operation is high enough so that the capacitors present negligible reactance.



Input control file used for simulation

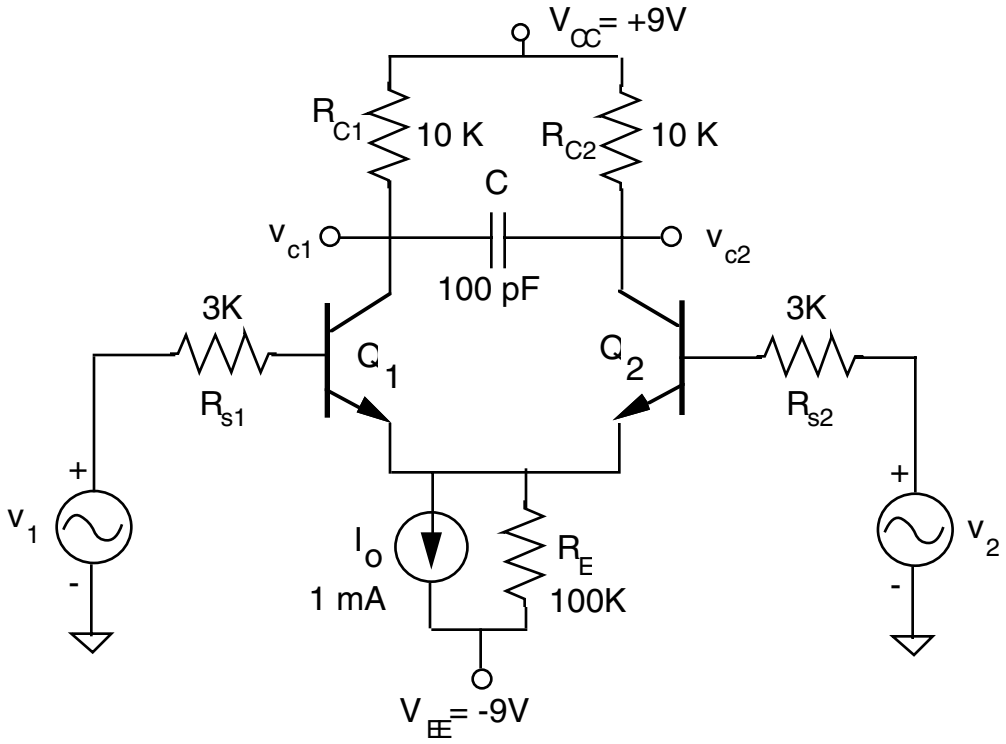
```
Vs  in  0  DC 0 AC 1
Rs   in  ss 90k
R1 G 0 300k
R2 10 G 700k
C1 ss G 0.1uF
RD 10  D 10k
RS1  S1 S2 50
RS2 S2 S3 3.5k
RS3 S3 0 100
C3 S2 S3 74uF
C2 D L 1uF
RL L 0 15k
M1 D G S1 S1 DNMOSFET
VDD 10 0  DC 30
.MODEL DNMOSFET
NMOS (VTO=1V,
Lambda=0.02 Kp=1m)
.OP
.AC DEC 10 1 10k
.END
```

Output file containing SPICE Simulation Results

NAME	M1	VTH	1.00E+00
MODEL	DNMOSFET	VDSAT	1.74E+00
ID	1.71E-03	GM	1.97E-03
VGS	2.74E+00	GDS	3.03E-05
VDS	6.59E+00	GMB	0.00E+00
VBS	0.00E+00		

Problem 4 - (10 points)

Consider the differential amplifier shown below. The transistors are identical devices with $\beta = 150$.



(a) Find the small signal, difference mode voltage gain defined as

$$A_{DM} = \frac{v_{c2} - v_{c1}}{v_2 - v_1} = \_\_\_\_\_$$

(b) Find the small signal, common mode voltage gain defined as

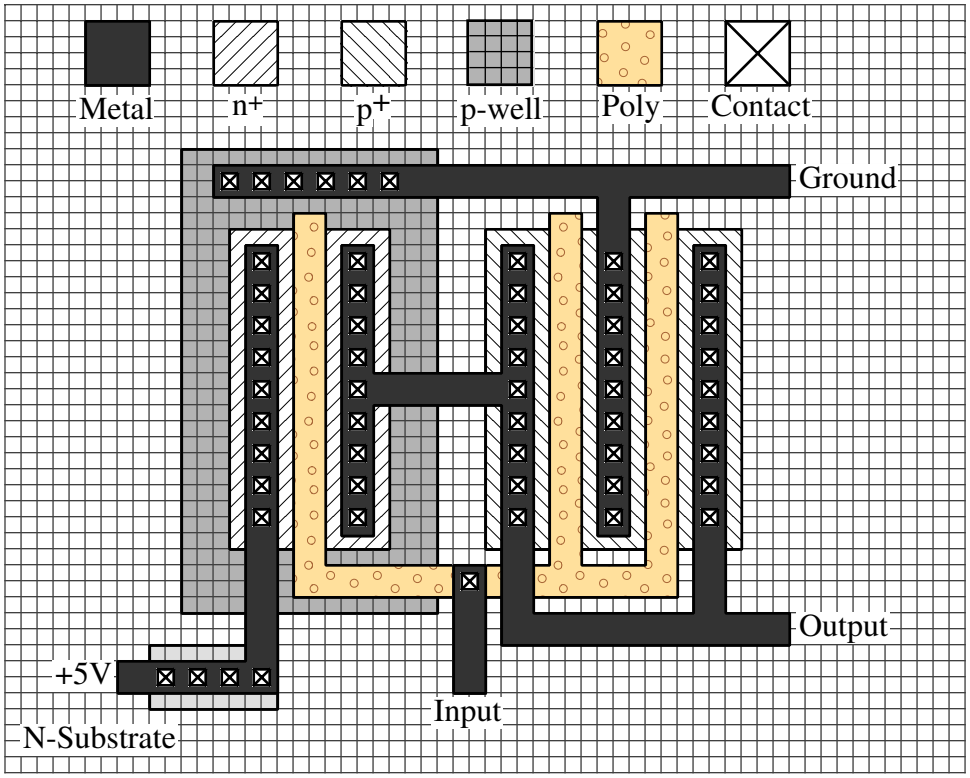
$$A_{CM} = \frac{0.5(v_{c2} + v_{c1})}{0.5(v_2 + v_1)} = \_\_\_\_\_$$

(c) Find the frequency where the difference mode voltage gain is down 3 dB.

$$f_{3dB} = \_\_\_\_\_$$

Problem 5 - (10 points)

Draw the electrical schematic using the proper symbols for the transistors. Identify on your schematic the terminals which are +5V, ground, input, and output. Label the transistors on the layout as M1, M2, etc. and determine their W/L values. Assume each square in the layout is 1 micron by 1 micron. Find the area in square microns and periphery in microns for the source and drain of each transistor.



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