Homework Assignment No. 8 - Solutions

Problem 1 - (10 points)

This problem deals with the op amp shown in Fig. P6.5-15. All device lengths are 1μm, the slew rate is ±10V/μs, the GB is 10MHz, the maximum output voltage is +2V, the minimum output voltage is -2V, and the input common mode range is from -1V to +2V. Design all W values of all transistors in this op amp. Your design must meet or exceed the specifications. When calculating the maximum or minimum output voltages, divide the voltage drop across series transistors equally. Ignore bulk effects in this problem. When you have completed your design, find the value of the small signal differential voltage gain, $A_{vd} = v_{out}/v_{id}$, where $v_{id} = v_1 - v_2$ and the small signal output resistance, R_{out}.

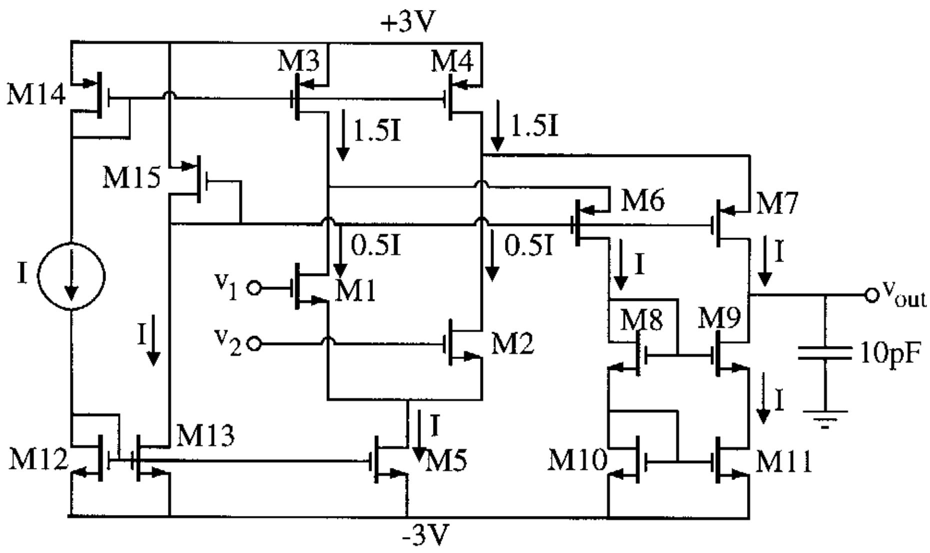


Figure P6.5-15

Solution

1.) The slew rate will specify I. $\therefore$ $I = C \cdot SR = 10^{-11} \cdot 10^{7} = 10^{-4} = 100\mu A$.

2.) Use GB to define W_1 and W_2.

$$GB = \frac{g_{m1}}{C} \quad \rightarrow \quad g_{m1} = GB \cdot C = 2\pi x 10^7 \cdot 10^{-11} = 628\mu S$$

$$\therefore W_1 = \frac{g_{m1}{}^2}{2K_N(0.5I)} = \frac{(628)^2}{2 \cdot 110 \cdot 50} = 35.85 \quad \Rightarrow \quad \underline{\underline{W_1 = W_2 = 36\mu m}}$$

3.) Design W_{15} to give V_T+2V_{ON} bias for M6 and M7. V_{ON} = 0.5V will meet the desired maximum output voltage specification. Therefore,

$$V_{SG15} = V_{ON15} + |V_T| = 2(0.5V) + |V_T| \quad \rightarrow V_{ON15} = 1V = \sqrt{\frac{2I}{K_P W_{15}}}$$

$$\therefore W_{15} = \frac{2I}{K_P V_{ON15}{}^2} = \frac{2 \cdot 100}{50 \cdot 1^2} = 4\mu m \quad \Rightarrow \quad \underline{\underline{W_{15} = 4\mu m}}$$

4.) Design W_3, W_4, W_6 and W_7 to have a saturation voltage of 0.5V with 1.5I current.

$$W_3 = W_4 = W_6 = W_7 = \frac{2(1.5I)}{K_P V_{ON}{}^2} = \frac{2 \cdot 150}{50 \cdot 0.5^2} = 24\mu m \quad \Rightarrow \underline{\underline{W_3 = W_4 = W_6 = W_7 = 24\mu m}}$$

Problem 6.5-15 – Continued

5.) Next design W_8, W_9, W_{10} and W_{11} to meet the minimum output voltage specification. Note that we have not taken advantage of smallest minimum output voltage because a normal cascode current mirror is used which has a minimum voltage across it of $V_T + 2V_{ON}$. Therefore, setting $V_T + 2V_{ON} = 1\text{V}$ gives $V_{ON} = 0.15\text{V}$. Using worst case current, we choose $1.5I$. Therefore,

$$W_8 = W_9 = W_{10} = W_{11} = \frac{2(1.5I)}{K_N V_{ON}^2} = \frac{2\cdot 150}{110\cdot 0.15^2} = 121\mu\text{m} \Rightarrow \underline{\underline{W_8 = W_9 = W_{10} = W_{11} = 121\mu\text{m}}}$$

6.) Check the maximum ICM voltage.

$$V_{ic}(\max) = V_{DD} + V_{SD3}(\text{sat}) + V_{TN} = 3\text{V} - 0.5 + 0.7 = 3.2\text{V} \text{ which exceeds spec.}$$

7.) Use the minimum ICM voltage to design W_5.

$$V_{ic}(\min) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1} = -3 + V_{DS5}(\text{sat}) + \left(\sqrt{\frac{2\cdot 50}{110\cdot 36}} + 0.7\right) = -1\text{V}$$

$$\therefore \quad V_{DS5}(\text{sat}) = 1.141 \rightarrow W_5 = \frac{2I}{K_N\ V_{DS5}(\text{sat})^2} = 1.39\mu\text{m} = 1.4\mu\text{m}$$

Also, let $W_{12} = W_{13} = W_5 \quad \Rightarrow \quad \underline{\underline{W_{12} = W_{13} = W_5 = 1.4\mu\text{m}}}$

8.) W_{14} is designed as

$$W_{14} = W_3 \frac{I_{14}}{I_3} = 24\mu\text{m}\ \frac{I}{1.5I} = 16\mu\text{m} \qquad \Rightarrow \qquad \underline{\underline{W_{14} = 16\mu\text{m}}}$$

Now, calculate the op amp small-signal performance.

$$R_{out} \approx r_{ds11} g_{m9} r_{ds9} || g_{m7} r_{ds7} (r_{ds2} || r_{ds4})$$

$$g_{m9} = \sqrt{2K_N \cdot I \cdot W_9} = 1632\mu\text{S}, \ r_{ds9} = r_{ds11} = \frac{25\text{V}}{100\mu\text{A}} = 0.25\text{M}\Omega,$$

$$g_{m7} = \sqrt{2K_P \cdot I \cdot W_7} = 490\mu\text{S}, \ r_{ds7} = \frac{20\text{V}}{100\mu\text{A}} = 0.2\text{M}\Omega, \ r_{d2} = \frac{25\text{V}}{50\mu\text{A}} = 0.5\text{M}\Omega$$

$$r_{ds4} = \frac{20\text{V}}{150\mu\text{A}} = 0.1333\text{M}\Omega \quad \therefore \quad \underline{\underline{R_{out} \approx 102\text{M}\Omega || 10.31\text{M}\Omega = 9.3682\text{M}\Omega}}$$

$$A_{vd} = \left(\frac{2+\text{k}}{2+2\text{k}}\right) g_{m1} R_{out}, \quad \text{k} = \frac{102\text{M}\Omega}{(r_{ds2}||r_{ds4}) g_{m7} r_{ds7}} = 9.888, \quad g_{m1} = \sqrt{K_N \cdot I \cdot W_1} = 629\mu\text{S}$$

$$\therefore \quad A_{vd} = (0.5459)(629\mu\text{S})(9.3682\text{M}\Omega) = 3{,}217\text{V/V} \quad \Rightarrow \quad \underline{\underline{A_{vd} = 3{,}217\text{V/V}}}$$

6.10 (6.28 4th ed)

If the bias current level of 741 input stage is doubled, then from (6.52) $G_{m1} = \frac{1}{2.7k\Omega}$

From (6.56)

$$R_{o1} = R_{out}|_{Q4} \| R_{out}|_{Q6}$$
$$= 2r_{o4} \| r_{o6}(1 + g_{m6} \times 1k\Omega)$$

Using $\eta_{npn} = 2\times10^{-4}$, $\eta_{pnp} = 5\times10^{-4}$ and $|I_C| = 19\mu A$, we have

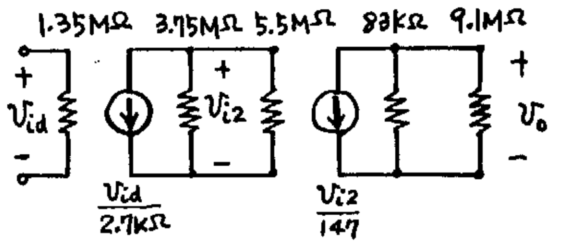
$$r_{o4} = \frac{1}{\eta g_m} = \frac{10^4}{5}\frac{26}{19\times10^{-3}} = 2.74M\Omega$$

$$r_{o6} = \frac{10^4}{2}\frac{26}{19\times10^{-3}} = 6.84M\Omega$$

$$g_{m6} \times 1k\Omega = 0.73$$

$$\therefore R_{o1} = (5.48)\|(6.84\times1.73)\ M\Omega$$
$$= 3.75\ M\Omega$$

741 equivalent



$$3.75 \| 5.5 = 2.23M\Omega$$

$$A_v = \frac{2230}{2.7} \times \frac{83}{0.147} = 826 \times 564$$
$$= 466{,}000$$

6.11 (6.29 4th ed)

If the 100Ω emitter resistor of Q_{17} is removed, then in (6.60a) we have

$$R_{eq1} = r_{\pi17} = \frac{\beta}{g_m} = 250 \times \frac{26}{0.55} = 11.8\ k\Omega$$

$$R_{i2} = r_{\pi16} + (1+\beta_0)(r_{\pi17} \| 50k\Omega)$$
$$= 406k\Omega + 251 \times 9.55k\Omega$$
$$= 2.8\ M\Omega$$

From (6.61)

$$G_{m2} \simeq g_{m17} = \frac{0.55}{26} = \frac{1}{47.3\Omega}$$

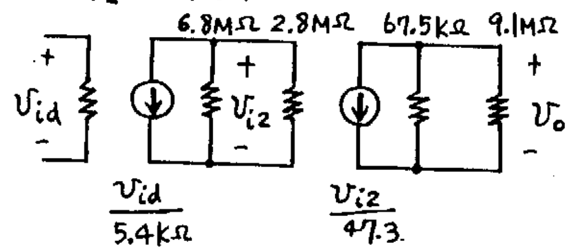
From (6.62)

$$R_{o2} = r_{o13B} \| r_{o17}$$

$$r_{o13B} = \frac{1}{\eta g_m} = \frac{10^4}{5}\frac{26}{0.55} = 94.5\ k\Omega$$

$$r_{o17} = \frac{1}{\eta g_m} = \frac{10^4}{2}\frac{26}{0.55} = 236\ k\Omega$$

$$\therefore R_{o2} = 67.5\ k\Omega$$



$$6.8 \| 2.8 = 1.98M\Omega$$

$$A_v = \frac{1980}{5.4} \times \frac{67.5}{0.047}$$
$$= 526{,}000$$

6.12 (6.30 4th ed.)

For positive input, the common-mode voltage limit is reached when Q_1 and Q_2 saturate and the input bias current increases greatly. This occurs for a CM input of

$$V^+ = V_{CC} - V_{CE(sat.)}$$

(Note that because of Q_8, the bias voltage at the collectors of Q_1 and Q_2 is $V_{CC} - V_{BE(on)}$, and

$$V^+ = V_{CC} - V_{BE_8(on)} - V_{CE_1}(sat.) + V_{BE_1(on)}$$
$$= V_{CC} - V_{CE(sat.)}\ )$$

For negative CM input voltage, the circuit ceases to function correctly when Q_3 and Q_4 saturated. This occurs for a CM input of

$$V^- = -V_{EE} + V_{BE6} + V_{BE7} + V_{CE(sat)} + V_{BE1}$$

6.12/6.30 - Cont'd

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741 AS A VOLTAGE FOLLOWER
*** INPUT STAGE
VCC 1 0 15V
VEE 2 0 -15V
Q12 3 3 1 PNP
R5 3 4 39K
Q11 4 4 2 NPN
Q10 6 4 5 NPN
R4 5 2 5K
Q9 6 7 1 PNP
Q8 7 7 1 PNP
Q1 7 8 10 NPN
Q2 7 9 11 NPN
Q3 12 6 10 PNP
Q4 16 6 11 PNP
Q5 12 13 14 NPN
Q6 16 13 15 NPN
R1 14 2 1K
R2 15 2 1K
Q7 1 12 13 NPN
R3 13 2 50K
*** DARLINGTON GAIN STAGE
Q16 1 16 17 NPN
R9 17 2 50K
Q17 19 17 18 NPN
R8 18 2 100
Q13B 19 3 1 PNPB
*** OUTPUT STAGE
Q13A 20 3 1 PNPA
Q19 20 20 21 NPN
Q18 20 21 22 NPN
R10 21 22 40K
Q23 2 19 22 PNP
Q20 2 22 23 PNP 3
R7 23 9 22
R6 25 9 27
Q14 1 20 25 NPN 3
.MODEL NPN NPN BF=250 IS=5E-15 VAF=130
.MODEL PNP PNP BF=50 IS=2E-15 VAF=52
.MODEL PNPA PNP BF=50 IS=0.5E-15 VAF=52
.MODEL PNPB PNP BF=50 IS=1.5E-15 VAF=52
VI1 8 0 0V
.DC VI1 -15 15 1
.PLOT DC V(9)
.OPTIONS NOPAGE NOMOD
.WIDTH OUT=80
.OP
.END
```

```
0****    DC TRANSFER CURVES
  VI1        V(9)
           -2.0D+01   -1.0D+01    0.0D+00    1.0D+01  2.0D+01
              ----------------------------------------
-1.500D+01 -1.312D+01 .      *  .         .         .         .
-1.400D+01 -1.312D+01 .      *  .         .         .         .
-1.300D+01 -1.300D+01 .      *  .         .         .         .
-1.200D+01 -1.200D+01 .       * .         .         .         .
-1.100D+01 -1.100D+01 .         *         .         .         .
-1.000D+01 -1.000D+01 .         *         .         .         .
-9.000D+00 -9.000D+00 .         .*        .         .         .
-8.000D+00 -8.000D+00 .         .  *      .         .         .
-7.000D+00 -7.000D+00 .         .   *     .         .         .
-6.000D+00 -6.000D+00 .         .    *    .         .         .
-5.000D+00 -5.000D+00 .         .     *   .         .         .
-4.000D+00 -4.000D+00 .         .      *  .         .         .
-3.000D+00 -3.000D+00 .         .       * .         .         .
-2.000D+00 -2.000D+00 .         .        *.         .         .
-1.000D+00 -9.997D-01 .         .         *         .         .
 0.000D+00  2.686D-04 .         .         *         .         .
 1.000D+00  1.000D+00 .         .         .*        .         .
 2.000D+00  2.000D+00 .         .         .  *      .         .
 3.000D+00  3.000D+00 .         .         .   *     .         .
 4.000D+00  4.000D+00 .         .         .    *    .         .
 5.000D+00  5.000D+00 .         .         .     *   .         .
 6.000D+00  6.000D+00 .         .         .      *  .         .
 7.000D+00  7.000D+00 .         .         .       * .         .
 8.000D+00  8.000D+00 .         .         .        *.         .
 9.000D+00  9.000D+00 .         .         .         *         .
 1.000D+01  1.000D+01 .         .         .         *         .
 1.100D+01  1.100D+01 .         .         .         .*        .
 1.200D+01  1.200D+01 .         .         .         . *       .
 1.300D+01  1.300D+01 .         .         .         .  *      .
 1.400D+01  1.400D+01 .         .         .         .   *     .
 1.500D+01  1.469D+01 .         .         .         .    *    .
              ----------------------------------------
```

```
0****    SMALL SIGNAL BIAS SOLUTION
 NODE   VOLTAGE
( 1)  15.0000   ( 2) -15.0000   ( 3)  14.3123   ( 4) -14.3351
( 5) -14.9034   ( 6)  -1.1086   ( 7)  14.4125   ( 8)  -0.0000
( 9)   0.0003   ( 10) -0.5441   ( 11) -0.5439   ( 12) -13.8948
( 13) -14.4462  ( 14) -14.9925  ( 15) -14.9925  ( 16) -13.7069
( 17) -14.2695  ( 18) -14.9306  ( 19)  -1.2605  ( 20)   0.5902
( 21)   0.0232  ( 22)  -0.6088  ( 23)  -0.0023  ( 25)   0.0035
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0**** BIPOLAR JUNCTION TRANSISTORS

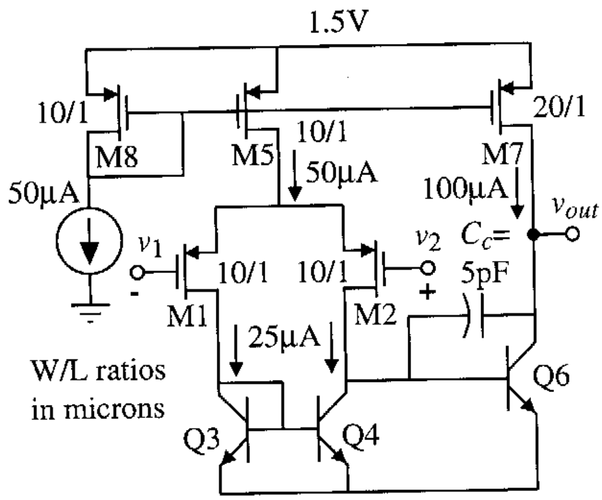
0	Q12	Q11	Q10	Q9	Q8	Q1	Q2
	PNP	NPN	NPN	PNP	PNP	NPN	NPN
IB	-1.41E-05	2.93E-06	6.99E-08	-2.93E-07	-2.93E-07	2.74E-08	2.75E-08
IC	-7.06E-04	7.32E-04	1.93E-05	-1.90E-05	-1.46E-05	7.60E-06	7.63E-06
VBE	-0.688	0.665	0.568	-0.587	-0.587	0.544	0.544
VBC	0.000	0.000	-13.226	15.521	0.000	-14.413	-14.412
VCE	-0.688	0.665	13.795	-16.109	-0.587	14.957	14.956

0	Q3	Q4	Q5	Q6	Q7	Q16	Q17
	PNP	PNP	NPN	NPN	NPN	NPN	NPN
IB	-1.21E-07	-1.21E-07	2.98E-08	2.98E-08	3.63E-08	5.59E-08	2.52E-06
IC	-7.51E-06	-7.54E-06	7.47E-06	7.48E-06	1.11E-05	1.71E-05	6.92E-04
VBE	-0.565	-0.565	0.546	0.546	0.551	0.563	0.661
VBC	12.786	12.598	-0.551	-0.739	-28.895	-28.707	-13.009
VCE	-13.351	-13.163	1.098	1.286	29.446	29.270	13.670

0	Q13B	Q13A	Q19	Q18	Q23	Q20	Q14
	PNPB	PNPA	NPN	NPN	PNP	PNP	NPN
IB	-1.06E-05	-3.53E-06	6.62E-08	8.21E-07	-3.50E-06	-1.83E-06	4.26E-07
IC	-6.89E-04	-2.23E-04	1.66E-05	2.06E-04	-2.21E-04	-1.17E-04	1.18E-04
VBE	-0.688	-0.688	0.567	0.632	-0.652	-0.606	0.587
VBC	15.573	13.722	0.000	-0.567	13.740	14.391	-14.410
VCE	-16.260	-14.410	0.567	1.199	-14.391	-14.998	14.997

Problem 5 – (10 points)

A two-stage, BiCMOS op amp is shown. For the PMOS transistors, the model parameters are K_P'=50µA/V^2, V_{TP} = -0.7V and $\lambda_P = 0.05\text{V}^{-1}$. For the NPN BJTs, the model parameters are β_F = 100, V_{CE}(sat) = 0.2V, V_A = 25V, V_t = 26mV, I_s = 10fA and n=1. (a.) Identify which input is positive and which input is negative. (b.) Find the numerical values of differential voltage gain magnitude, $|A_v(0)|$, GB (in Hertz), the slew rate, SR, and the location of the RHP zero. (c.) Find the numerical value of the maximum and minimum input common mode voltages.



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Solution

(a.) The plus and minus signs on the schematic show which input is positive and negative.

(b.) The differential voltage gain, $A_v(0)$, is given as

$$A_v(0) = \frac{g_{m1}}{g_{ds2}+g_{o4}+g_{\pi6}} \cdot \frac{g_{m6}}{g_{ds7}+g_{o6}} \qquad g_{m1} = g_{m2} = \sqrt{2\cdot50\cdot25\cdot10} = 158.1\mu S$$

$$r_{ds2} = \frac{1}{\lambda_P I_D} = \frac{20}{25\mu A} = 0.8M\Omega,\ r_{o4} = \frac{V_A}{I_C} = \frac{25V}{25\mu A} = 1M\Omega,\ g_{m6} = \frac{I_C}{V_t} = \frac{100\mu A}{26mV} = 3846\mu S$$

$$r_{\pi6} = \frac{\beta_F}{g_{m6}} = 26k\Omega, \quad r_{ds7} = \frac{1}{\lambda_P I_D} = \frac{20}{100\mu A} = 0.2M\Omega \text{ and } r_{o6} = \frac{V_A}{I_C} = \frac{25V}{100\mu A} = 0.25M\Omega$$

$\therefore$ $|A_v(0)| = [158.1(0.8||1||0.026)][3846(0.2||0.25)] = 3.888\cdot427.36 =$ 1,659.6V/V

$$GB = \frac{g_{m1}}{C_c} = \frac{158.1\mu S}{5pF} = 31.62\text{x}10^6 \text{ rads/sec} \rightarrow GB = 5.0325\text{MHz}$$

$$SR = \frac{50\mu A}{5pF} = 10V/\mu s$$

$$\text{RHP zero} = \frac{g_{m6}}{C_c} = \frac{3.846mS}{5pF} = 769.24\text{x}10^6 \text{ rads/sec. (122MHz)}$$

(c.) The maximum input common mode voltage is given as

$$v_{icm}+ = V_{CC}-V_{DS5}(\text{sat}) - V_{SG1} = 1.5 - \sqrt{\frac{2\cdot50}{50\cdot10}} - 0.7 - \sqrt{\frac{2\cdot25}{50\cdot10}} = 0.8 - 0.447 - 0.316 =$$

$\therefore$ $v_{icm}+ =$ 0.0367V

$$v_{icm}- = -1.5 + V_{BE3} - V_{T1} = -1.5 + V_t \ln\left(\frac{25\mu A}{10fA}\right) - 0.7 = -2.2 + 0.5626 = -1.6374V$$