

LECTURE 020 – ECE 4430 REVIEW II (READING: GHLM - Chap. 2)

Objective

The objective of this presentation is:

- 1.) Identify the prerequisite material as taught in ECE 4430
- 2.) Insure that the students of ECE 6412 are adequately prepared

Outline

- Models for Integrated-Circuit Active Devices
- Bipolar, MOS, and BiCMOS IC Technology
- Single-Transistor and Multiple-Transistor Amplifiers
- Transistor Current Sources and Active Loads

BIPOLAR, MOS, AND BICMOS IC TECHNOLOGY

Bipolar Technology

- *npn* BJT technology
- Compatible *pnp* BJTs
- Modifications to the standard *npn* BJT technology

Major Processing Steps for a Junction Isolated BJT Technology

Start with a *p* substrate.

1. Implantation of the buried n^+ layer
2. Growth of the epitaxial layer
3. p^+ isolation diffusion
4. Base *p*-type diffusion
5. Emitter n^+ diffusion
6. p^+ ohmic contact
7. Contact etching
8. Metal deposition and etching
9. Passivation and bond pad opening

Integrated Circuit NPN BJT

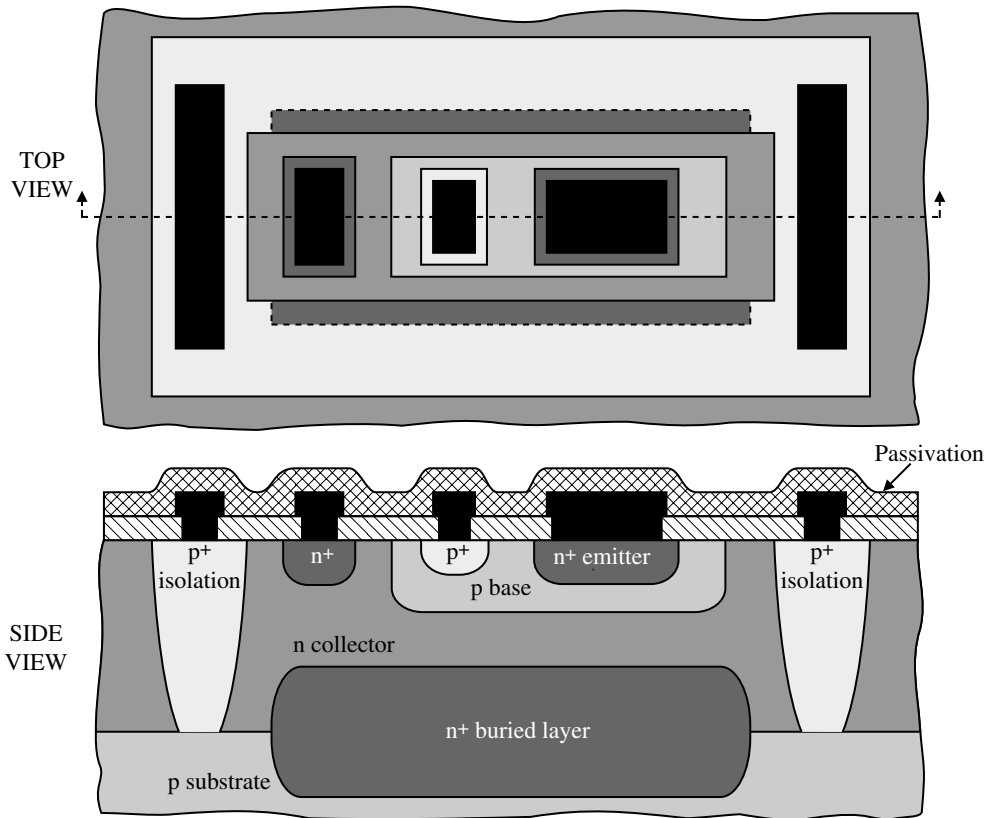


Fig.020-01

Substrate *pnp* BJT

Collector is connected to the substrate potential which is the most negative DC potential.

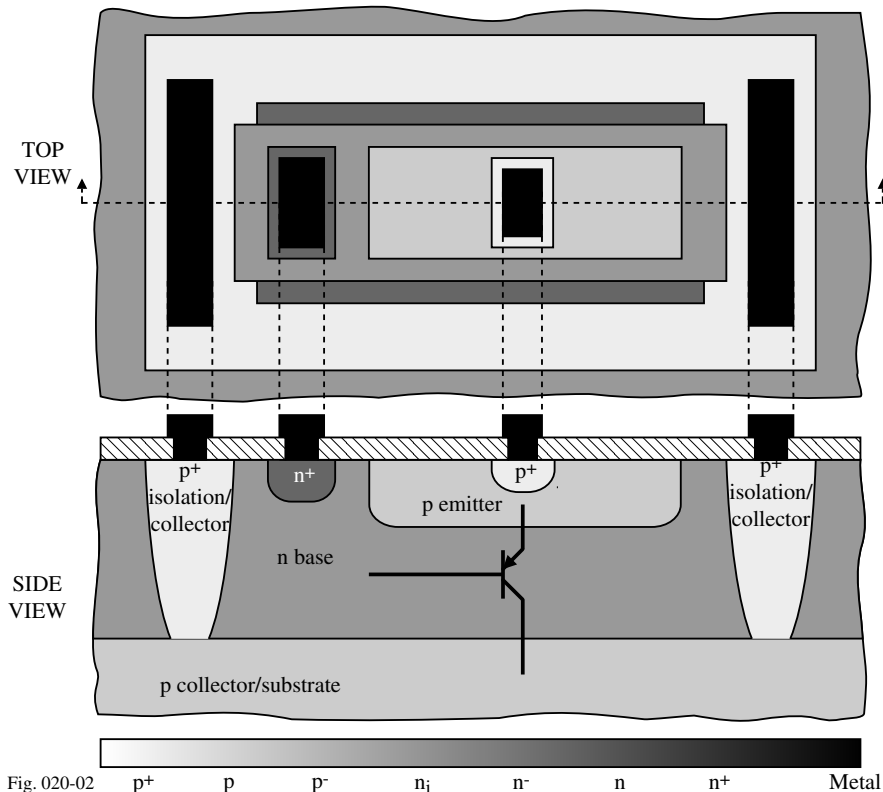
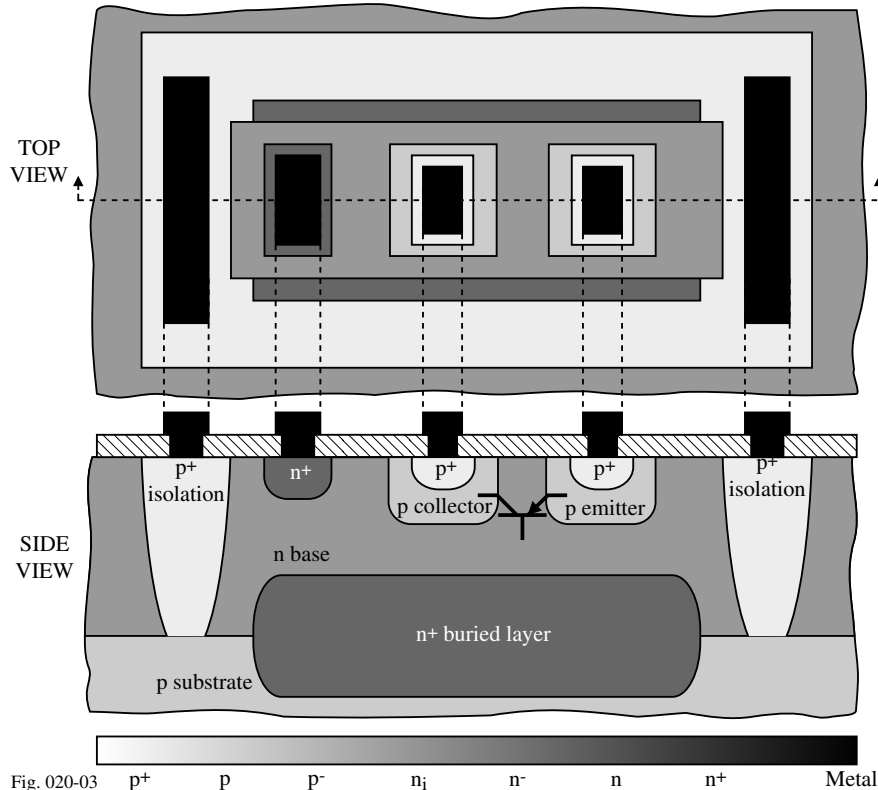


Fig. 020-02

Lateral *pnp* BJT

Collector is not constrained to a fixed dc potential.



ECE 6412 - Analog Integrated Circuits and Systems II

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CMOS Technology

N-Well CMOS Fabrication Major Steps:

- 1.) Implant and diffuse the n-well
- 2.) Deposition of silicon nitride
- 3.) n-type field (channel stop) implant
- 4.) p-type field (channel stop) implant
- 5.) Grow a thick field oxide (FOX)
- 6.) Grow a thin oxide and deposit polysilicon
- 7.) Remove poly and form LDD spacers
- 8.) Implantation of NMOS S/D and n-material contacts
- 9.) Remove spacers and implant NMOS LDDs
- 10.) Repeat steps 8.) and 9.) for PMOS
- 11.) Anneal to activate the implanted ions
- 12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)
- 13.) Open contacts, deposit first level metal and etch unwanted metal
- 14.) Deposit another interlayer dielectric (CVD SiO₂), open vias and deposit second level metal
- 15.) Etch unwanted metal, deposit a passivation layer and open over bonding pads

Typical CMOS Technology

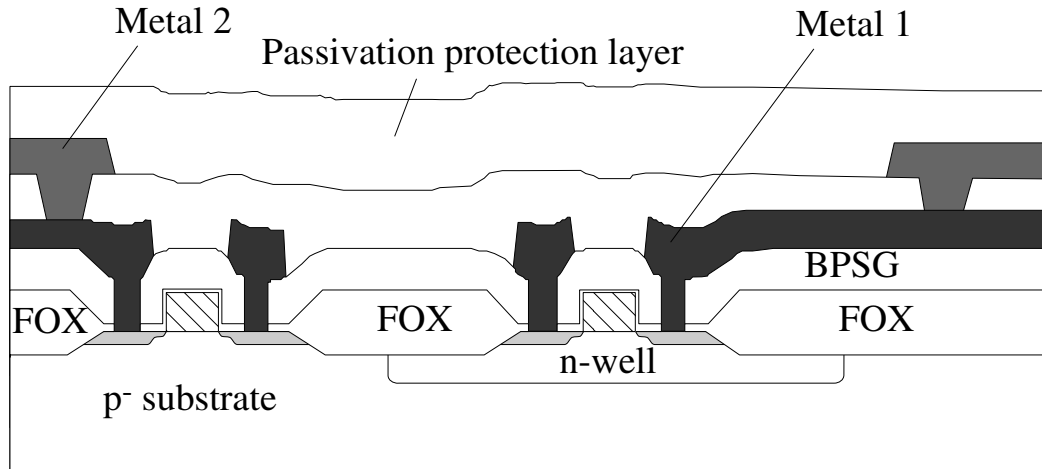


Fig. 020-04

p-well process is similar but starts with a p-well implant rather than an n-well implant.

Example of 0.5µm CMOS Technology

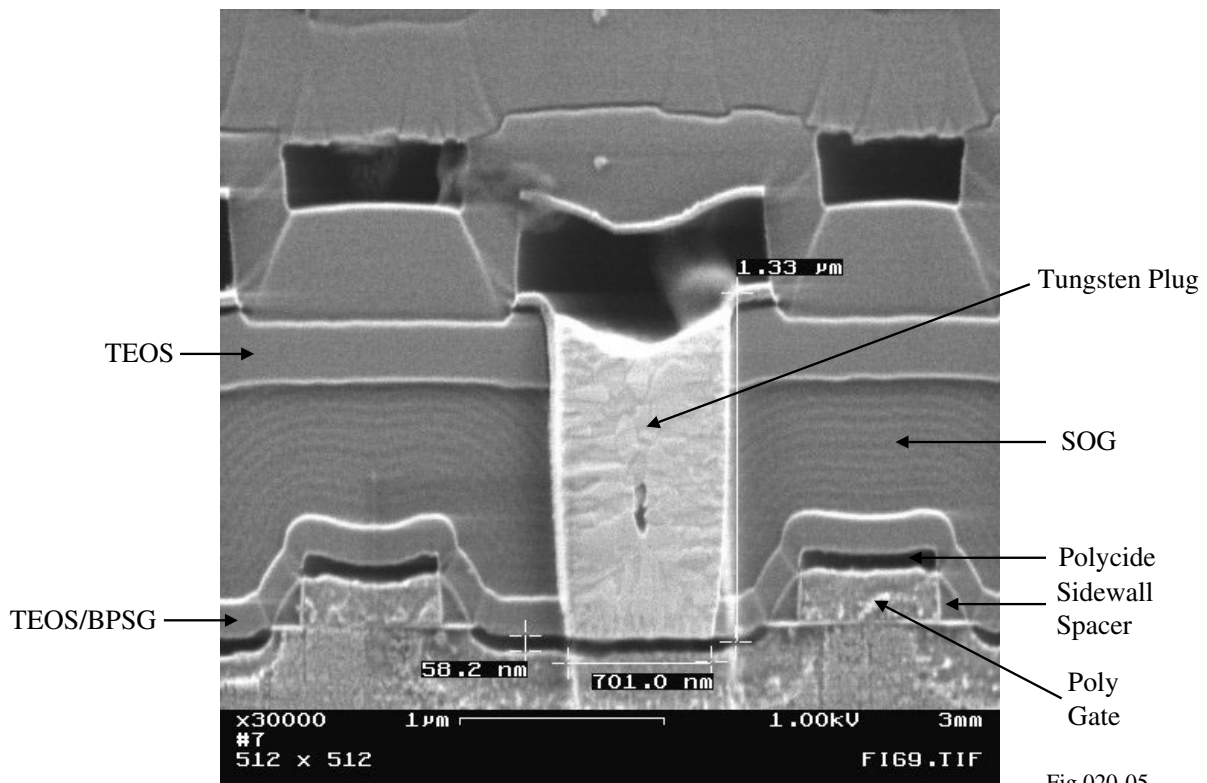


Fig.020-05

BiCMOS Technology

The following steps are typical of a 0.5 μm BiCMOS process typical of today's deep submicron technologies.

Masking Sequence:

- | | |
|--------------------------------|---------------------------------|
| 1. Buried n ⁺ layer | 13. PMOS lightly doped drain |
| 2. Buried p ⁺ layer | 14. n ⁺ source/drain |
| 3. Collector tub | 15. p ⁺ source/drain |
| 4. Active area | 16. Silicide protection |
| 5. Collector sinker | 17. Contacts |
| 6. n-well | 18. Metal 1 |
| 7. p-well | 19. Via 1 |
| 8. Emitter window | 20. Metal 2 |
| 9. Base oxide/implant | 21. Via 2 |
| 10. Emitter implant | 22. Metal 3 |
| 11. Poly 1 | 23. Nitride passivation |
| 12. NMOS lightly doped drain | |

BiCMOS Technology Illustration

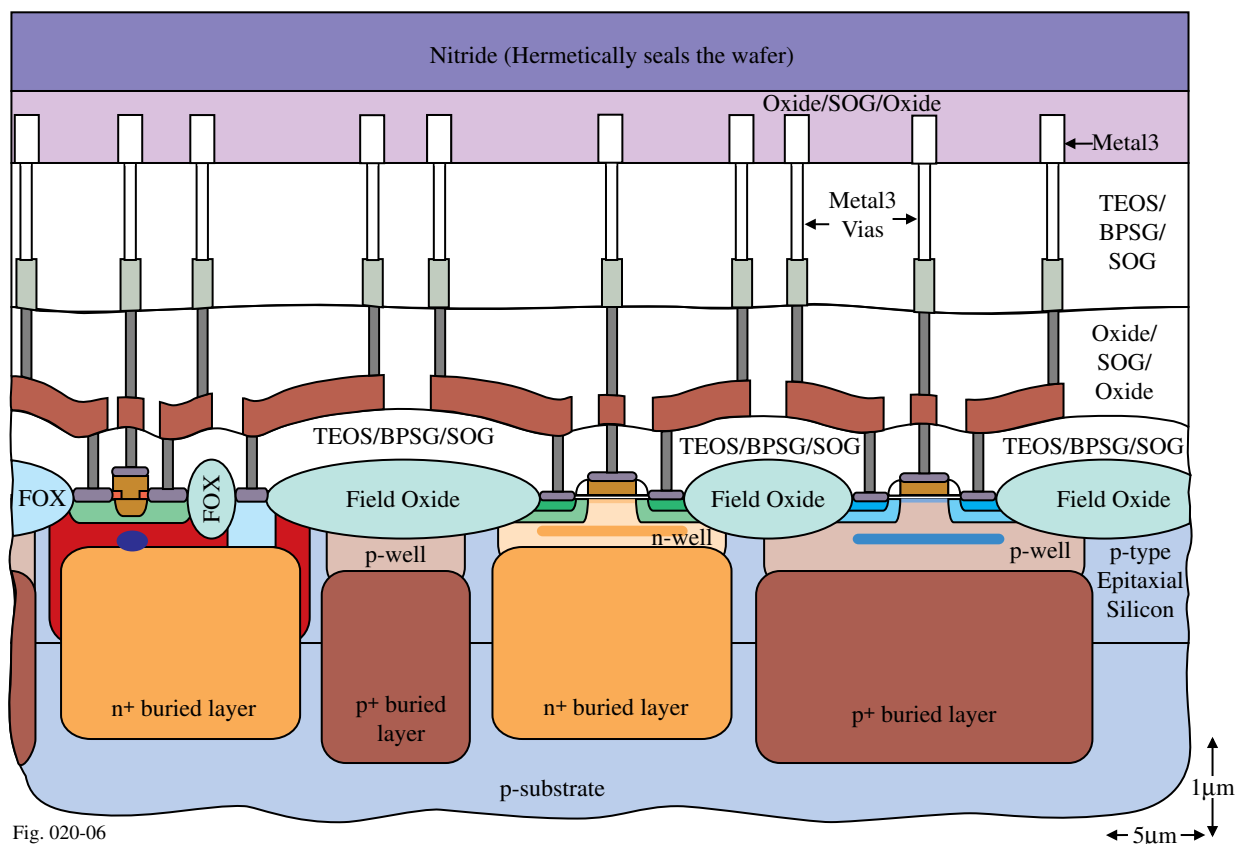


Fig. 020-06

Passive Components - Collector-Base Capacitance (C_{μ})

Illustration:

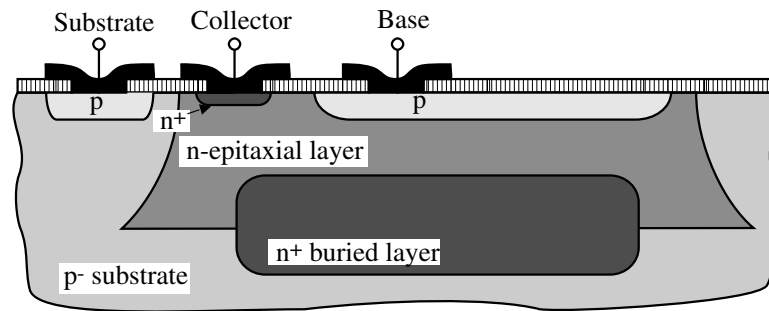


Fig. 020-07

Model:

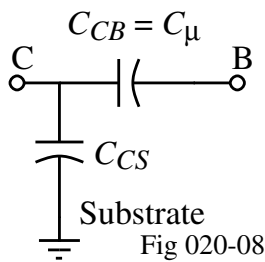


Fig 020-08

Sidewall contribution:

$$A_{sidewall} = P \cdot d \frac{\pi}{2}$$

where

P = perimeter of the capacitor

d = depth of the diffusion

Values (Includes the bottom plus sidewall capacitance):

$$C_{\mu} \approx 1\text{fF}/\mu\text{m}^2 \text{ (dependent on the reverse bias voltage)}$$

Can also have base-emitter capacitance and collector-substrate capacitance

MOS Capacitors

Polysilicon-Oxide-Channel for Enhancement MOSFETs

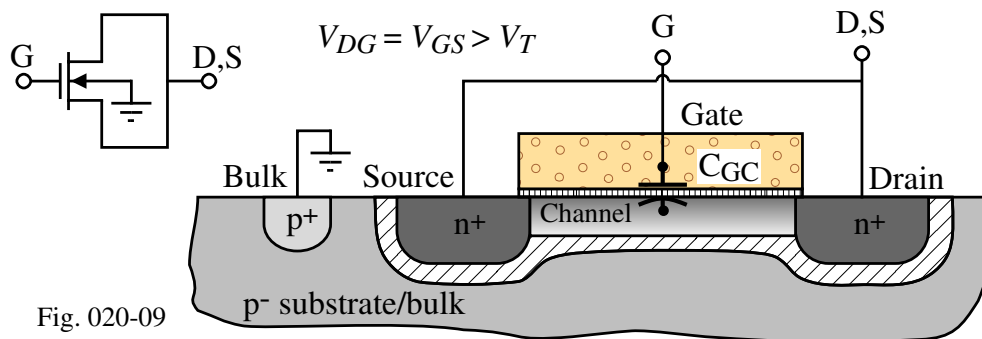


Fig. 020-09

Comments:

- The capacitance variation is achieved by changing the mode of operation from depletion (minimum capacitance) to inversion (maximum capacitance).
- Capacitance = $C_{GS} \approx C_{ox} W \cdot L$
- Channel must be formed, therefore $V_{GS} > V_T$
- With $V_{GS} > V_T$ and $V_{DS} = 0$, the transistor is in the active region.
- LDD transistors will give lower Q because of the increase of series resistance.

MOS Capacitors

Bulk tuning of the polysilicon-oxide-channel capacitor (0.35 μ m CMOS)

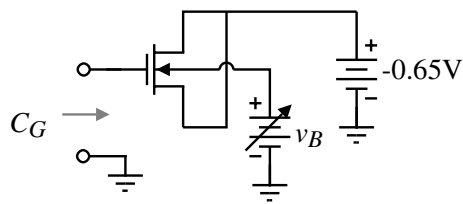
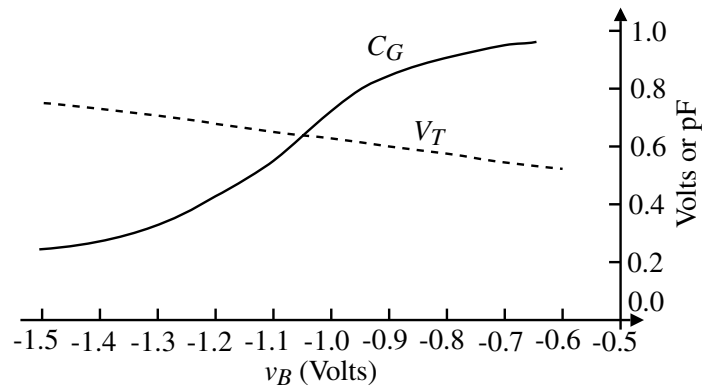


Fig. 020-10



$$C_{\max}/C_{\min} \approx 4$$

Accumulation-Mode Capacitor¹²

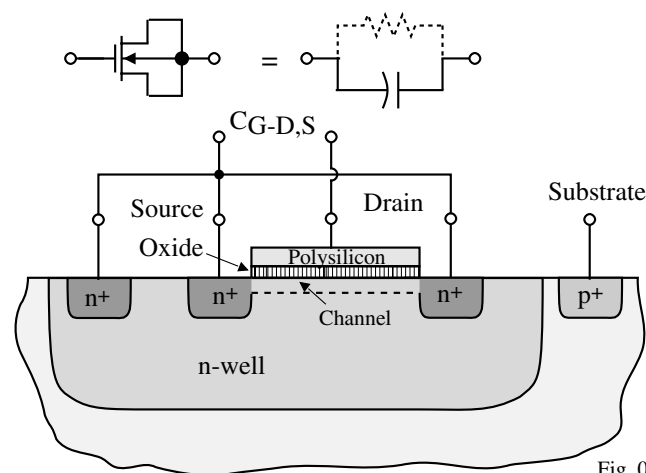


Fig. 020-11

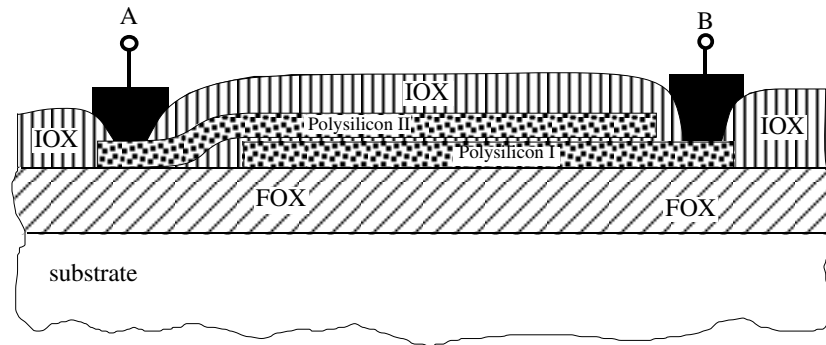
Comments:

- Again, the capacitor variation is achieved by moving from the depletion (min. C) to accumulation (max. C)
- $\pm 30\%$ tuning range (Tuned by the voltage across the capacitor terminals)
- $Q \approx 25$ for 3.1 pF at 1.8 GHz (optimization leads to Q s of 200 or greater)

¹ T. Soorapanth, et. al., "Analysis and Optimization of Accumulation-Mode Varactor for RF ICs," Proc. 1998 Symposium on VLSI Circuits, *Digest of Papers*, pp. 32-33, 1998.

² R. Castello, et. al., "A $\pm 30\%$ Tuning Range Varactor Compatible with future Scaled Technologies," Proc. 1998 Symposium on VLSI Circuits, *Digest of Papers*, pp. 34-35, 1998.

Polysilicon-Oxide-Polysilicon (Poly-Poly)



Best possible capacitor for analog circuits

Less parasitics

Voltage independent

Capacitor Errors:

- 1.) Oxide gradients
- 2.) Edge effects
- 3.) Parasitics
- 4.) Voltage dependence
- 5.) Temperature dependence

Horizontal Metal Capacitors

Capacitance between conductors on the same level and use lateral flux..

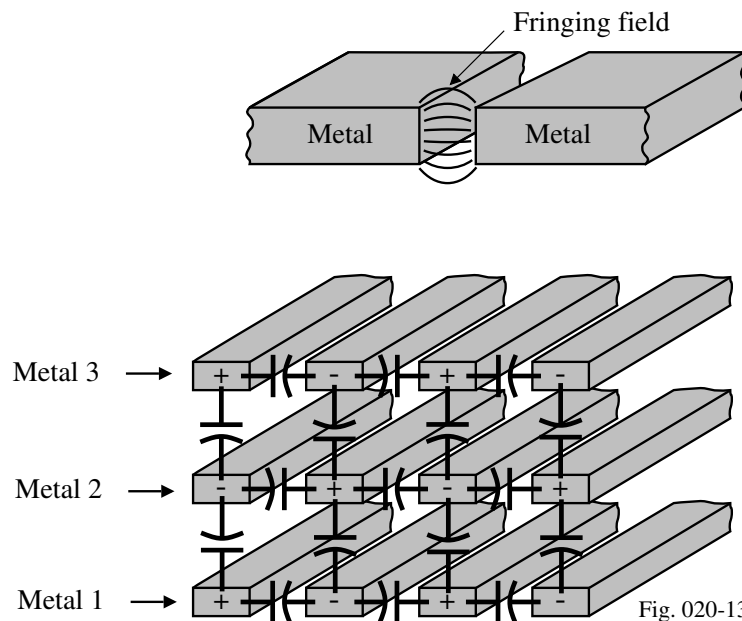


Fig. 020-13

These capacitors are called fractal capacitors because the fractal patterns are structures that enclose a finite area with an infinite perimeter.

In certain cases, the capacitor/area can be increased by a factor of 10 over vertical flux capacitors.

Integrated Circuit Resistors - Layout

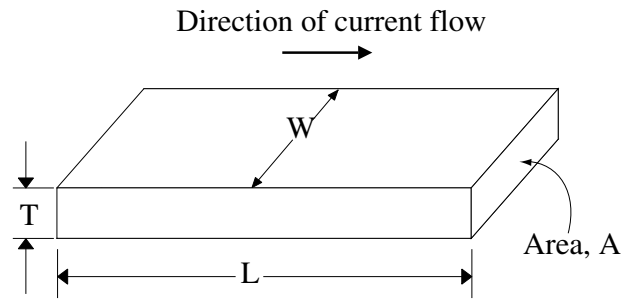


Fig. 020-14/170-02

Resistance of a conductive sheet is expressed in terms of

$$R = \frac{\rho L}{A} = \frac{\rho L}{WT} \quad (\Omega)$$

where

ρ = resistivity in $\Omega\text{-m}$

Ohms/square:

$$R = \left(\frac{\rho}{T}\right) \frac{L}{W} = \rho_S \frac{L}{W} \quad (\Omega)$$

where

ρ_S is a sheet resistivity and has the units of ohms/square

Base and Emitter Diffused Resistors

Cross-section of a Base Resistor:

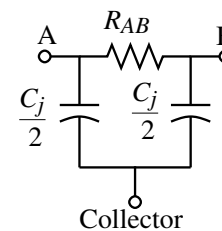
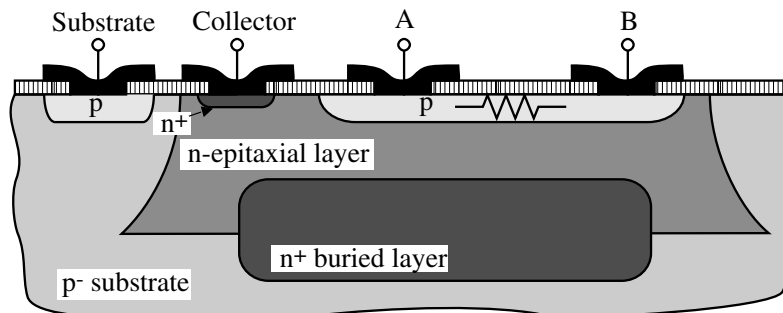


Fig. 020-15/170-03

Comments:

Sheet resistance $\approx 100 \Omega/\text{sq.}$ to $200 \Omega/\text{sq.}$

TCR = $+1500\text{ppm}/^\circ\text{C}$

Note:

$$\frac{1\%}{^\circ\text{C}} = \frac{10^4\text{ppm}}{^\circ\text{C}}$$

Emitter Resistor:

Sheet resistance $\approx 2 \Omega/\text{sq.}$ to $10 \Omega/\text{sq.}$ (Generally too small to make sufficient resistance in reasonable area)

TCR = $+600\text{ppm}/^\circ\text{C}$

Epitaxial Pinched Resistor

Good for large values of sheet resistance.

Cross-section:

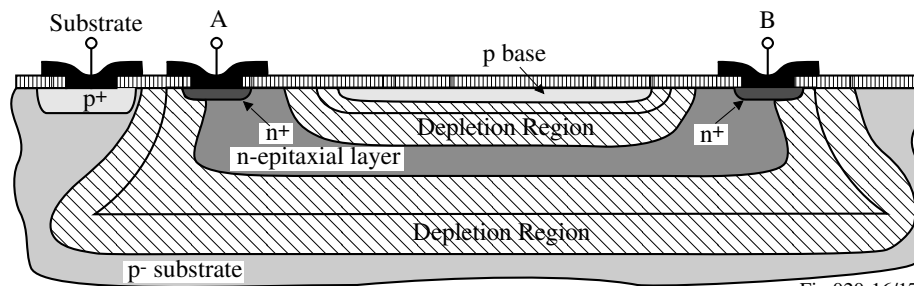


Fig 020-16/170-05

IV Curves and Model:

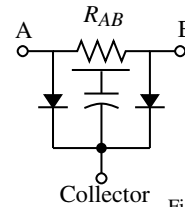
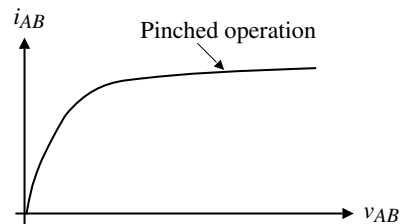


Fig. 020-17/170-06

Comments:

Sheet resistance is 4 to 10k Ω /sq.

Voltage across the resistor is limited to 6V or less because of breakdown

TCR \approx 2500ppm/ $^{\circ}$ C

MOS Resistors - Source/Drain Resistor

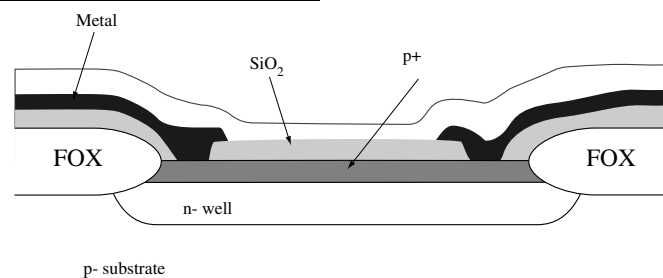


Fig. 020-18

Diffusion:

10-100 ohms/square

Absolute accuracy = $\pm 35\%$

Relative accuracy = 2% (5 μ m),
0.2% (50 μ m)

Temperature coefficient = 1500 ppm/ $^{\circ}$ C

Voltage coefficient \approx 200 ppm/V

Ion Implanted:

500-2000 ohms/square

Absolute accuracy = $\pm 15\%$

Relative accuracy = 2% (5 μ m),
0.15% (50 μ m)

Temperature coefficient = 400 ppm/ $^{\circ}$ C

Voltage coefficient \approx 800 ppm/V

Comments:

- Parasitic capacitance to well is voltage dependent.
- Piezoresistance effects occur due to chip strain from mounting.

Polysilicon Resistor

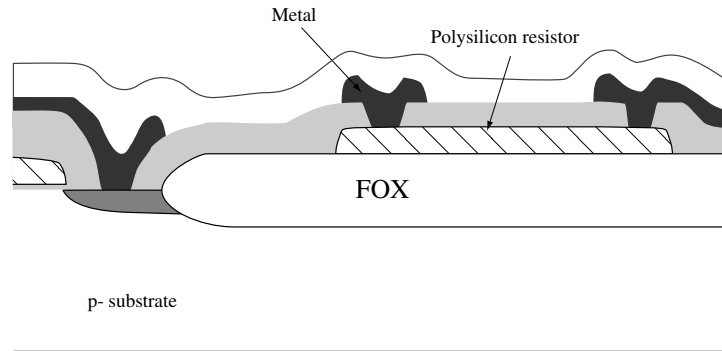


Fig. 020-19

30-100 ohms/square (unshielded)

100-500 ohms/square (shielded)

Absolute accuracy = $\pm 30\%$

Relative accuracy = 2% ($5\ \mu\text{m}$)

Temperature coefficient = $500\text{-}1000\ \text{ppm}/^\circ\text{C}$

Voltage coefficient $\approx 100\ \text{ppm}/\text{V}$

Comments:

- Used for fuzes and laser trimming
- Good general resistor with low parasitics

N-well Resistor

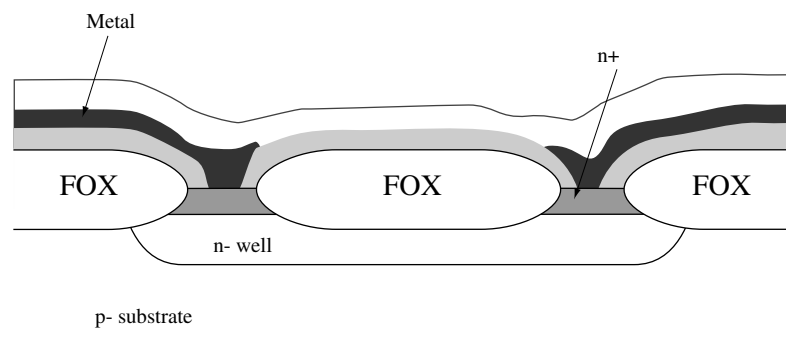


Fig. 020-20

1000-5000 ohms/square

Absolute accuracy = $\pm 40\%$

Relative accuracy $\approx 5\%$

Temperature coefficient = $4000\ \text{ppm}/^\circ\text{C}$

Voltage coefficient is large $\approx 8000\ \text{ppm}/\text{V}$

Comments:

- Good when large values of resistance are needed.
- Parasitics are large and resistance is voltage dependent

Integrated Circuit Passive Component Performance Summary

Component Type	Range of Values	Absolute Accuracy	Relative Accuracy	Temperature Coefficient	Voltage Coefficient
MOS Capacitor	0.35-1.0 fF/ μm^2	10%	0.1%	20ppm/ $^{\circ}\text{C}$	± 20 ppm/V
Poly-Poly Capacitor	0.3-1.0 fF/ μm^2	20%	0.1%	25ppm/ $^{\circ}\text{C}$	± 50 ppm/V
Base Diffused	100-200 Ω /sq.	$\pm 20\%$	0.2%	+1750ppm/ $^{\circ}\text{C}$	-
Emitter Diffused	2-10 Ω /sq.	$\pm 20\%$	$\pm 2\%$	+600ppm/ $^{\circ}\text{C}$	-
Base Pinched	2k-10k Ω /sq.	$\pm 50\%$	$\pm 10\%$	+2500ppm/ $^{\circ}\text{C}$	Poor
Epitaxial Pinched	2k-5k Ω /sq.	$\pm 50\%$	$\pm 7\%$	+3000ppm/ $^{\circ}\text{C}$	Poor
S/D Diffused	10-100 Ω /sq.	35%	2%	1500ppm/ $^{\circ}\text{C}$	200ppm/V
Implanted Resistor	0.5-2 k Ω /sq.	15%	2%	400ppm/ $^{\circ}\text{C}$	800ppm/V
Poly Resistor	30-200 Ω /sq.	30%	2%	1500ppm/ $^{\circ}\text{C}$	100ppm/V
n-well Resistor	1-10 k Ω /sq.	40%	5%	8000ppm/ $^{\circ}\text{C}$	10kppm/V
Thin Film	0.1k-2k Ω /sq.	± 5 - $\pm 20\%$	± 0.2 - $\pm 2\%$	± 10 to ± 200 ppm/ $^{\circ}\text{C}$	-

SUMMARY

- Bipolar Technology
 - Vertical NPN transistor
 - Substrate PNP transistor
 - Lateral PNP transistor
- CMOS Technology
 - Substrate BJT
 - Lateral BJT
- BiCMOS Technology
 - Vertical NPN transistor
 - CMOS transistors
- Passive Components Compatible with IC Technology
 - Resistors
 - Capacitors