LECTURE 060 – PUSH-PULL OUTPUT STAGES
(READING: GHLM – 362-384, AH – 226-229)

Objective

The objective of this presentation is:

Show how to design stages that

1.) Provide sufficient output power in the form of voltage or current.

2.) Avoid signal distortion.

3.) Be efficient

4.) Provide protection from abnormal conditions (short circuit, over temperature, etc.)

Outline

- Push-Pull MOS (Class B)
- Push-Pull BJT (Class B)
- Summary

PUSH-PULL MOS OUTPUT STAGES (Class AB and B)

Push-Pull Source Follower

Can both sink and source current and provide a slightly lower output resistance.

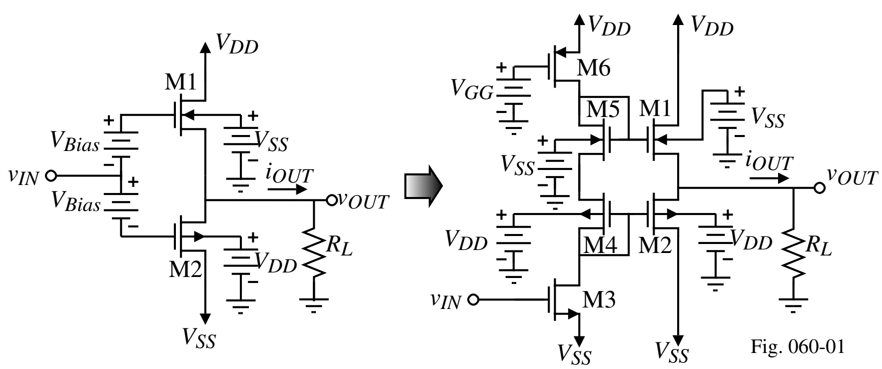


Fig. 060-01

Efficiency:

Depends on how the transistors are biased.

- Class B - one transistor has current flow for only 180° of the sinusoid (half period)

$$\therefore \text{ Efficiency} = \frac{P_{RL}}{P_{VDD}} = \frac{\dfrac{v_{OUT}(\text{peak})^2}{2R_L}}{(V_{DD}-V_{SS})\left(\dfrac{1}{2}\right)\left(\dfrac{2v_{OUT}(\text{peak})}{\pi R_L}\right)} = \frac{\pi}{2}\,\frac{v_{OUT}(\text{peak})}{V_{DD}-V_{SS}}$$

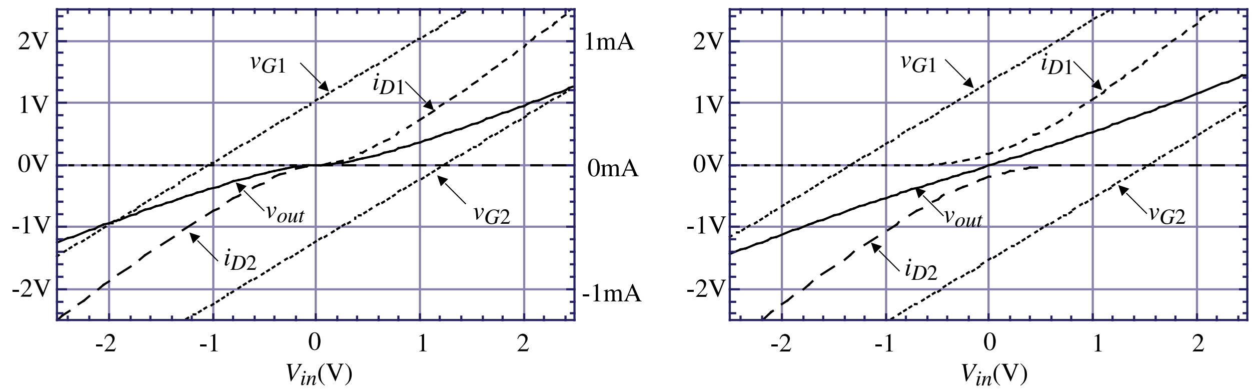
Maximum efficiency occurs when $v_{OUT}(\text{peak}) = V_{DD}$ and is 78.5%

- Class AB - each transistor has current flow for more than 180° of the sinusoid.

Maximum efficiency is between 25% and 78.5%

Illustration of Class B and Class AB Push-Pull, Source Follower

Output current and voltage characteristics of the push-pull, source follower (R_L = 1kΩ):



Class B, push-pull, source follower

Class AB, push-pull, source follower

Fig. 060-02

Comments:

- Note that v_{OUT} cannot reach the extreme values of V_{DD} and V_{SS}
- I_{OUT}^+(max) and I_{OUT}^-(max) is always less than V_{DD}/R_L or V_{SS}/R_L
- For v_{OUT} = 0V, there is quiescent current flowing in M1 and M2 for Class AB
- Note that there is significant distortion at v_{IN} =0V for the Class B push-pull follower

Small-Signal Performance of the Push-Pull Follower

Model:

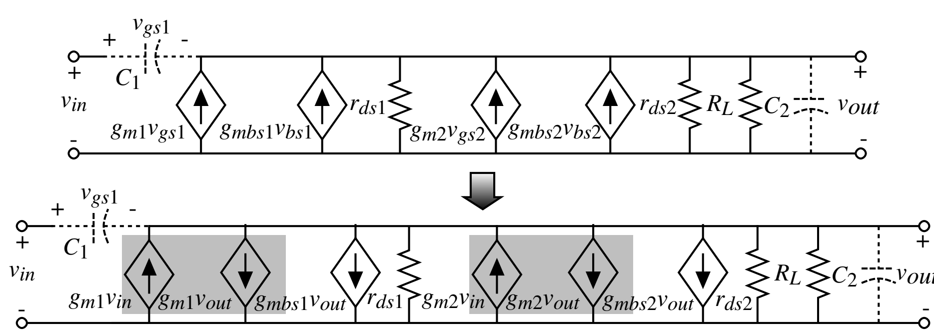


Fig. 060-03

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1} + g_{m2}}{g_{ds1}+g_{ds2}+g_{m1}+g_{mbs1}+g_{m2}+g_{mbs2}+G_L}$$

$$R_{out} = \frac{1}{g_{ds1}+g_{ds2}+g_{m1}+g_{mbs1}+g_{m2}+g_{mbs2}} \text{ (does not include } R_L\text{)}$$

If V_{DD} = -V_{SS} = 2.5V, V_{out} = 0V, I_{D1} = I_{D2} = 500µA, and W/L = 20µm/2µm, A_v = 0.787 (R_L=∞) and R_{out} = 448Ω.

A zero and pole are located at

$$z = \frac{-(g_{m1}+g_{m2})}{C_1} \qquad p = \frac{-(g_{ds1}+g_{ds2}+g_{m1}+g_{mbs1}+g_{m2}+g_{mbs2}+G_L)}{C_1+C_2}.$$

These roots will be high-frequency because the associated resistances are small.

Push-Pull, Common Source Amplifiers

Similar to the class A but can operate as class B providing higher efficiency.

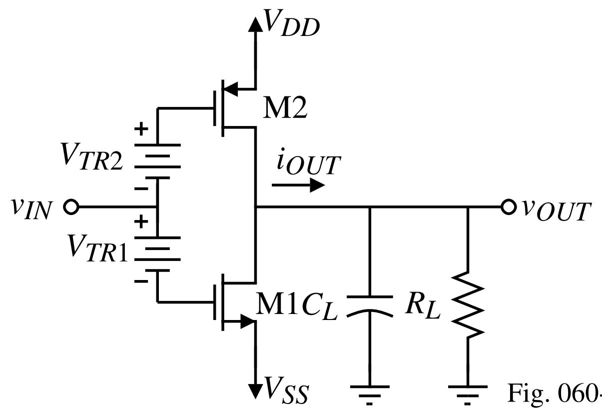


Fig. 060-04

Comments:

- The batteries V_{TR1} and V_{TR2} are necessary to control the bias current in M1 and M2.
- The efficiency is the same as the push-pull, source follower.

Practical Implementation of the Push-Pull, Common Source Amplifier

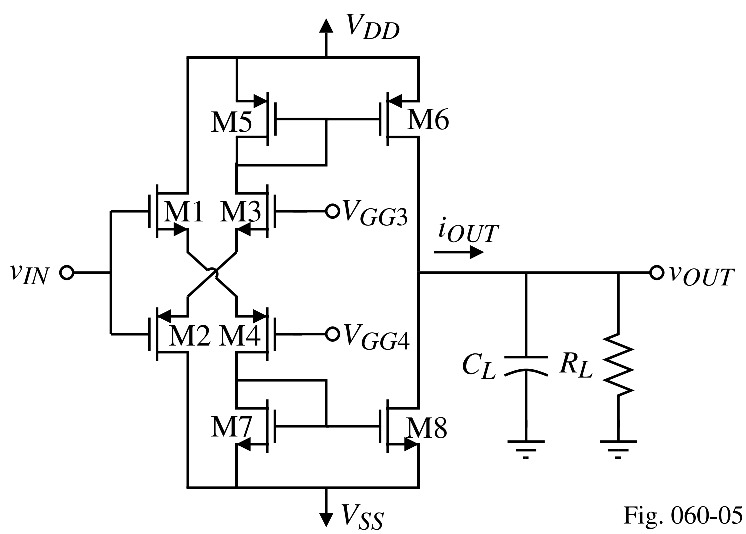


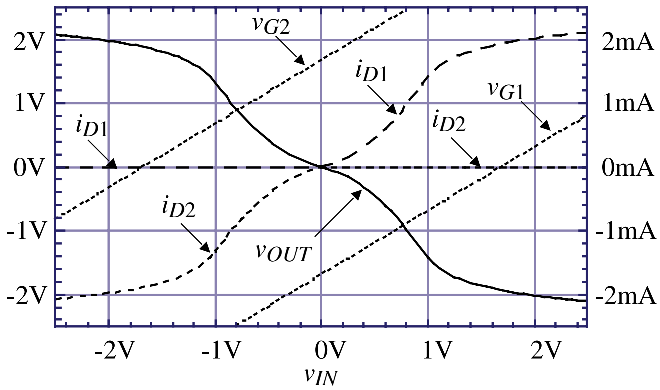
Fig. 060-05

V_{GG3} and V_{GG4} can be used to bias this amplifier in class AB or class B operation.

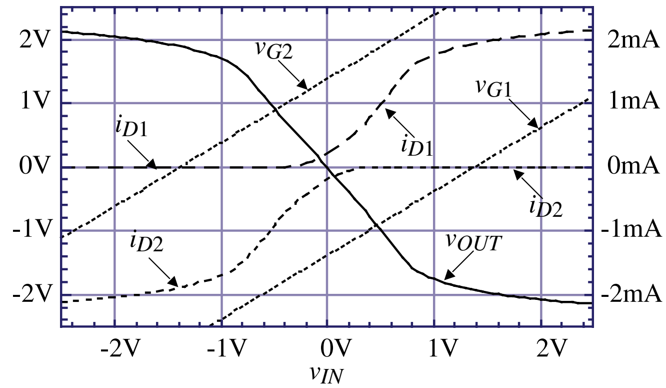
Note, that the bias current in M6 and M8 is not dependent upon V_{DD} or V_{SS} (assuming V_{GG3} and V_{GG4} are not dependent on V_{DD} and V_{SS}).

Illustration of Class B and Class AB Push-Pull, Inverting Amplifier

Output current and voltage characteristics of the push-pull, inverting amplifier (R_L = 1kΩ):



Class B, push-pull, inverting amplifier.



Class AB, push-pull, inverting amplifier. Fig.060-06

Comments:

- Note that there is significant distortion at v_{IN} =0V for the Class B inverter
- Note that v_{OUT} cannot reach the extreme values of V_{DD} and V_{SS}
- I_{OUT}^+(max) and I_{OUT}^-(max) is always less than V_{DD}/R_L or V_{SS}/R_L
- For v_{OUT} = 0V, there is quiescent current flowing in M1 and M2 for Class AB

Use of Negative, Shunt Feedback to Reduce the Output Resistance

Concept:

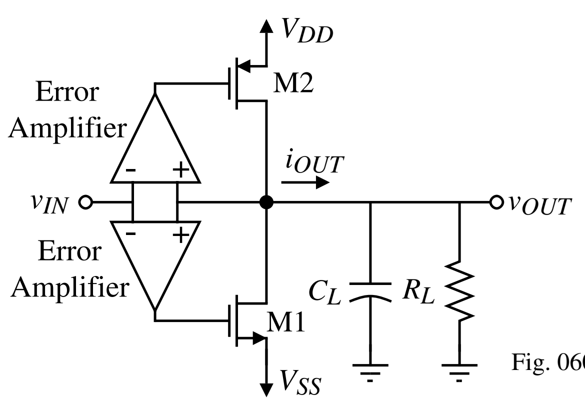


Fig. 060-07

$$R_{out} = \frac{r_{ds1}||r_{ds2}}{1+\text{Loop Gain}}$$

Comments:

- Can achieve output resistances as low as 10Ω.
- If the error amplifiers are not balanced, it is difficult to control the quiescent current in M1 and M2
- Great linearity because of the strong feedback
- Can be efficient if operated in class B or class AB

Simple Implementation of Neg., Shunt Feedback to Reduce the Output Resistance

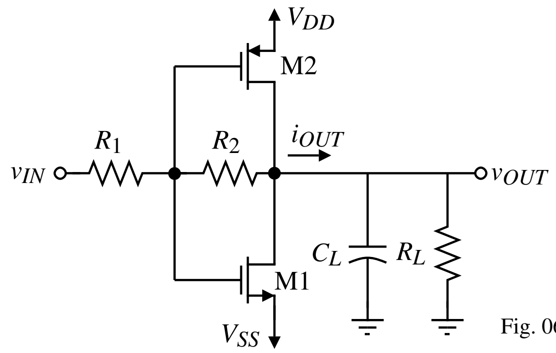


Fig. 060-08

$$\text{Loop gain} \approx \left(\frac{R_1}{R_1+R_2}\right)\left(\frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}+G_L}\right)$$

$$\therefore \qquad R_{out} = \frac{r_{ds1}||r_{ds2}}{1+\left(\frac{R_1}{R_1+R_2}\right)\left(\frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}+G_L}\right)}$$

Let $R_1 = R_2$, $R_L = \infty$, I_{Bias} = 500µA, W_1/L_1 = 100µm/1µm and W_2/L_2 = 200µm/1µm.

Thus, g_{m1} = 3.316mS, g_{m2} = 3.162mS, r_{ds1} = 50kΩ and r_{ds2} = 40kΩ.

$$\therefore \quad R_{out} = \frac{50\text{k}\Omega||40\text{k}\Omega}{1+0.5\left(\frac{3316+3162}{25+20}\right)} = \frac{22.22\text{k}\Omega}{1+0.5(143.9)} = 304\Omega \qquad (R_{out} = 5.42\text{k}\Omega \text{ if } R_L = 1\text{k}\Omega)$$

What about the use of BJTs in CMOS Technology?

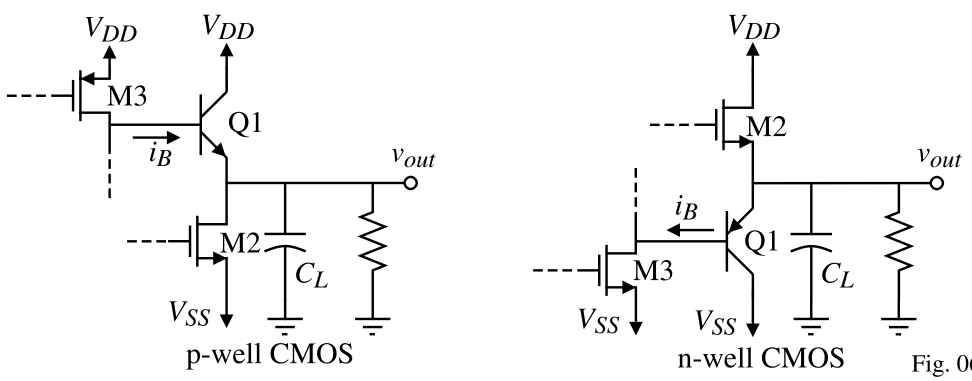


Fig. 060-09

Comments:

- Can use either substrate or lateral BJTs.
- Small-signal output resistance is $1/g_m$ which can easily be less than 100Ω.
- Unfortunately, only PNP or NPN BJTs are available but not both on a standard CMOS technology.
- In order for the BJT to sink (or source) large currents, the base current, i_B, must be large. Providing large currents as the voltage gets to extreme values is difficult for MOSFET circuits to accomplish.
- If one considers the MOSFET driver, the emitter can only pull to within $v_{BE}+V_{ON}$ of the power supply rails. This value can be 1V or more.

PUSH-PULL BJT OUTPUT STAGES (Class AB and B)

Simple Class B Output Stage

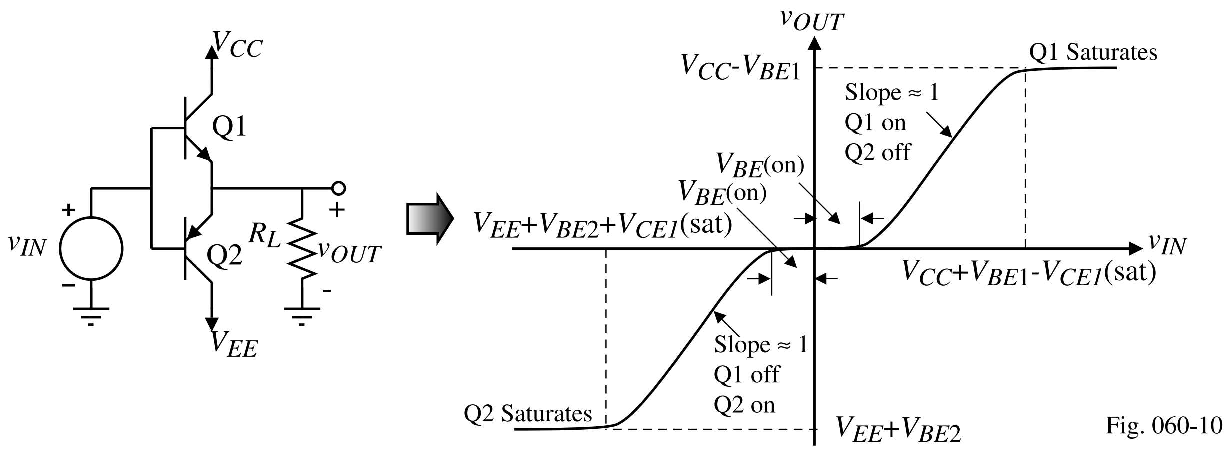


Fig. 060-10

Class B operation: Two active devices are used to deliver the power instead of one. Each device conducts for alternate half cycles.

Efficiency can approach 78.5%

Can suffer from crossover distortion - the transition from one device to the other.

Class AB Output Stage

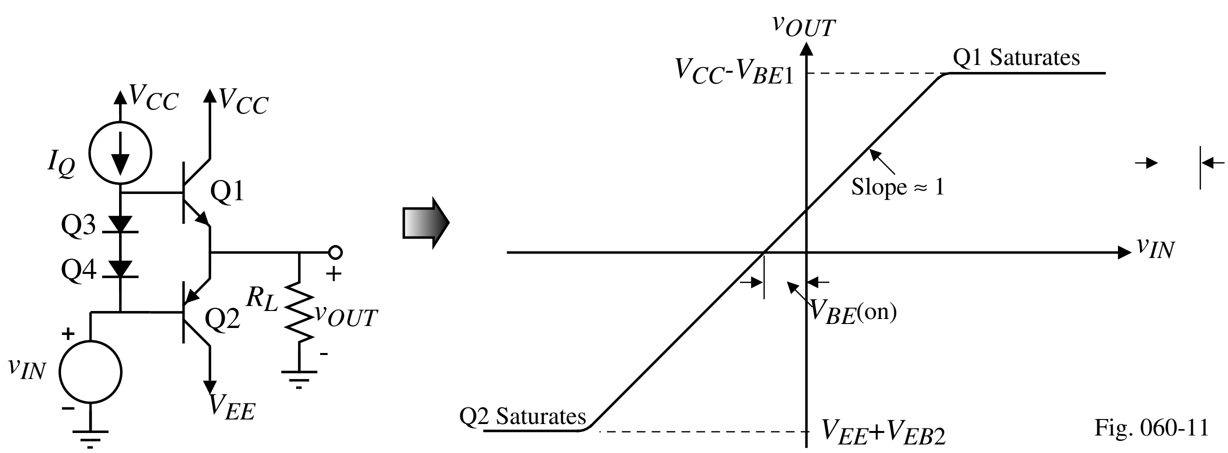


Fig. 060-11

I_Q sets up the bias current in Q1 and Q2 when there is no input signal.

Each transistor is biased so that there is a region in the middle where both are on (Class AB)

Power Considerations in the Class B Output Stage

Voltage and current waveforms for a Class B amplifier:

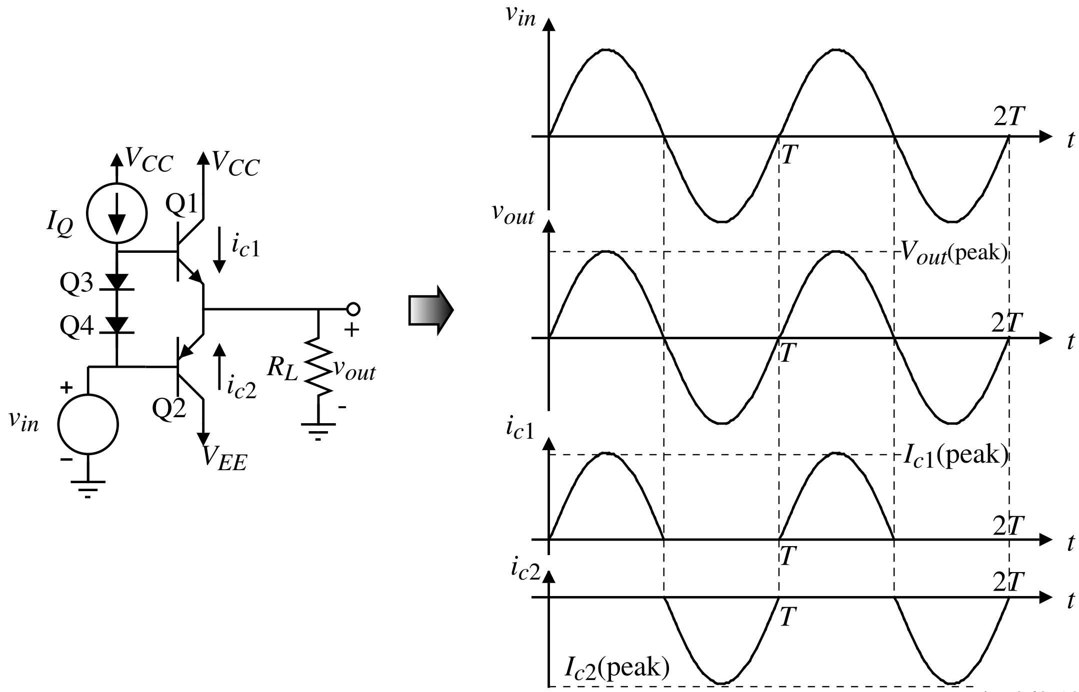


Fig. 060-12

Efficiency Considerations of the Class-B Push-Pull Output Stage

Load line for one device in a class-B stage:

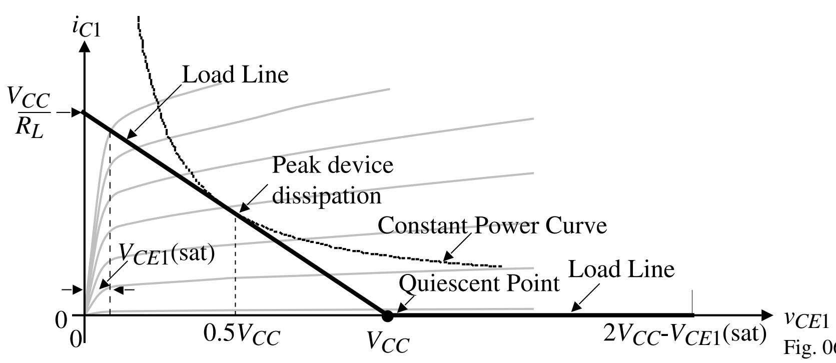


Fig. 060-13

Efficiency:

$$P_L = \frac{1}{2}\frac{[V_{out}(\text{peak})]^2}{R_L}$$

and $$P_{supply} = 2V_{CC}I_{supply} = 2V_{CC}\left(\frac{1}{T}\int_0^T i_C(t)dt\right) = 2V_{CC}\left(\frac{I_c(\text{peak})}{\pi}\right) = \frac{2}{\pi}\frac{V_{CC}}{R_L}V_{out}(\text{peak})$$

$$\therefore \ \eta = \frac{P_L}{P_{supply}} = \frac{\pi}{4}\frac{V_{out}(\text{peak})}{V_{CC}} \qquad \Rightarrow \qquad \eta_{max} = \frac{\pi}{4} = 78.6\%$$

Max. efficiency for the above class-B push-pull output stage is $\eta_{max} = \frac{\pi}{4}\frac{V_{CC} - V_{CE}(\text{sat})}{V_{CC}}$

709 Output Stage

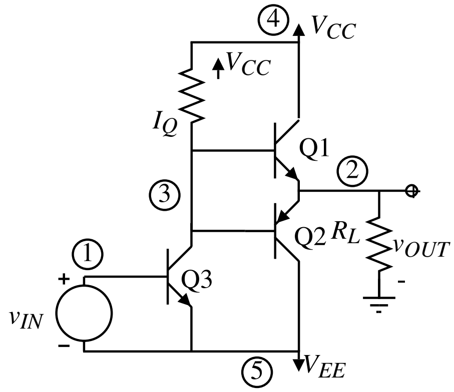
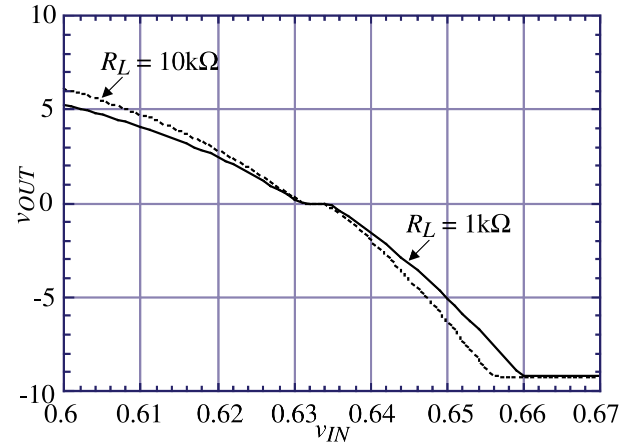


Fig. 060-14




```
709 Output Stage Voltage Transfer Function
.MODEL BJTN NPN IS=1E-14 BF=100 VAF=50
.MODEL BJTP PNP IS=1E-14 BF=50 VAF=50
Q1 4 3 2 BJTN
Q2 5 3 2 BJTP
Q3 3 1 5 BJTN
VCC 4 0 DC 10V
VEE 5 0 DC -10V
VIN 1 5
RL 2 0 1KILOHM
R1 4 3 20KILOHM
.DC VIN 0.60 0.67 0.001
.PRINT DC V(2)
.PROBE
.END
```

This stage assumes that feedback will be used around the amplifier which will linearize the nonlinearity of the output stage.

741 Output Stage

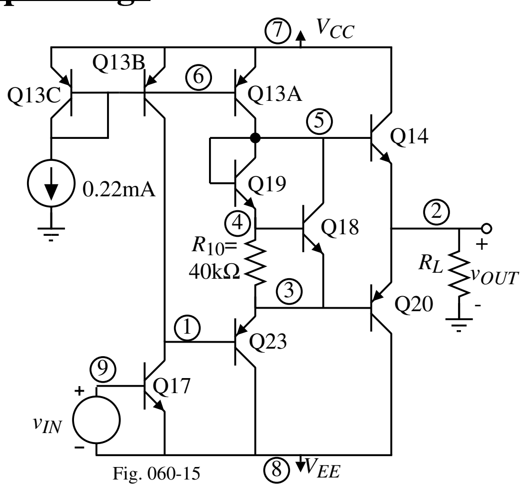
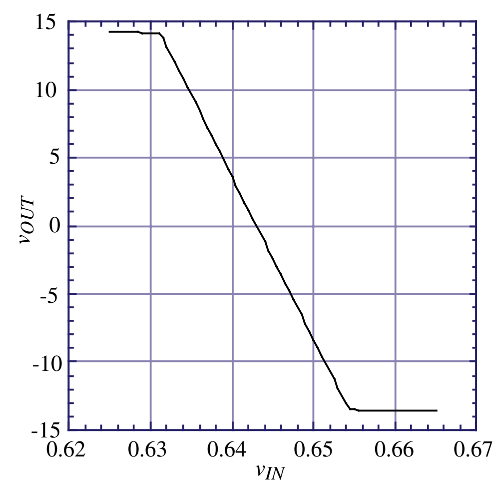


Fig. 060-15




```
741 Output Stage Voltage Transfer Function - RL =
1Kilohm
.MODEL BJTN NPN IS=1E-14 BF=100 VAF=50
.MODEL BJTP PNP IS=1E-14 BF=50 VAF=50
Q23 8 1 3 BJTP
Q20 8 3 2 BJTP
Q14 7 5 2 BJTN
Q17 1 9 8 BJTN
Q18 5 4 3 BJTN
Q19 5 5 4 BJTN
Q13A 5 6 7 BJTP
Q13B 1 6 7 BJTP 3.0
Q13C 6 6 7 BJTP
VCC 7 0 DC 15V
VEE 8 0 DC -15V
IBIAS 6 0 220UA
VIN 9 8 DC 0.645
R10 4 3 40KILOHM
RL 2 0 1KILOHM
.DC VIN 0.625 0.665 0.0005
.PRINT DC V(2)
.PROBE
.END
```


Quasi-Complementary Output Stages

Quasi-complementary connections are used to improve the performance of the PNP or PMOS transistor.

Composite connections:

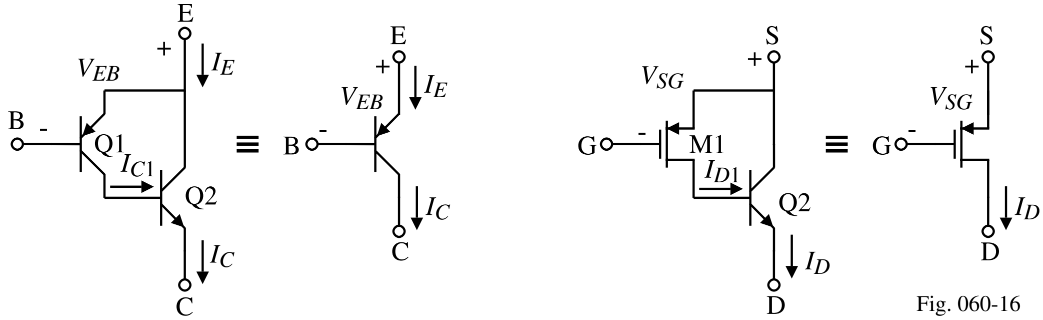


Fig. 060-16

PNP Equivalent:

$$I_C = (1+\beta_2)\, I_{C1} = (1+\beta_2)\, I_s \exp\left(\frac{V_{EB}}{V_t}\right)$$

∴ The composite has the beta of an NPN

PMOS Equivalent:

$$I_D = (1+\beta_2)\, I_{D1} = (1+\beta_2)\left(\frac{K_P' W_1}{2L_1}\right)(V_{GS}-V_T)^2$$

∴ The composite has an enhanced K'

Overload Protection

For circuits that can provide large amounts of output current, it is necessary to provide short-circuit current protection.

Example:

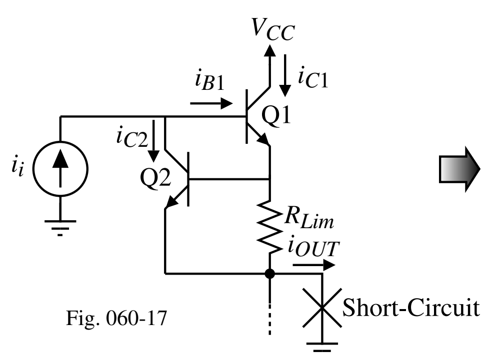
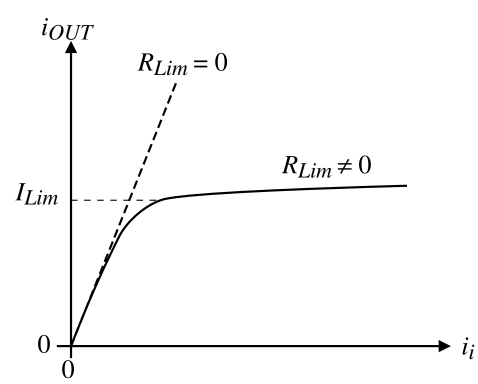


Fig. 060-17



$$i_{OUT} = i_{C1}+i_{C2} \approx i_{C1} \qquad \therefore \quad i_{OUT} = \beta_1 i_{B1} = \beta_1(i_i - i_{C2})$$

But $i_{C2} \approx I_{s2}\exp\left(\frac{v_{BE2}}{V_t}\right) \approx I_{s2}\exp\left(\frac{i_{C1}R_{Lim}}{V_t}\right)$

$$\therefore \quad i_{OUT} = \beta_1 i_i - I_{s2}\exp\left(\frac{i_{C1}R_{Lim}}{V_t}\right)$$

As i_{OUT} increases, Q2 turns on and pulls base current away from Q1 limiting the output current.

SUMMARY

Requirements of Output Stages

- The objectives are to provide output power in form of voltage and/or current.
- In addition, the output amplifier should be linear and be efficient.
- Low output resistance is required to provide power efficiently to a small load resistance.
- High source/sink currents are required to provide sufficient output voltage rate due to large load capacitances.
- Types of output stages considered:

  Class B or AB stage with push-pull (maximum efficiency was 78.6%)
- Quasi-complementary devices help improve the performance of the p-type devices
- Protection circuits prevent large currents from flowing in the output devices
- For large load capacitors all that is required from an output stage is large current, the output resistance does not have to be small

