LECTURE 430 – PHASE-LOCKED LOOPS
(READING: GHLM – 720-743)

Introduction

This section focuses on the applications of nonlinear analog circuits to perform the signal processing functions of phase locking.

Objective:

- Introduce the concepts of analog phase-locked loops
- Give examples of PLL implementation using IC technology

Outline

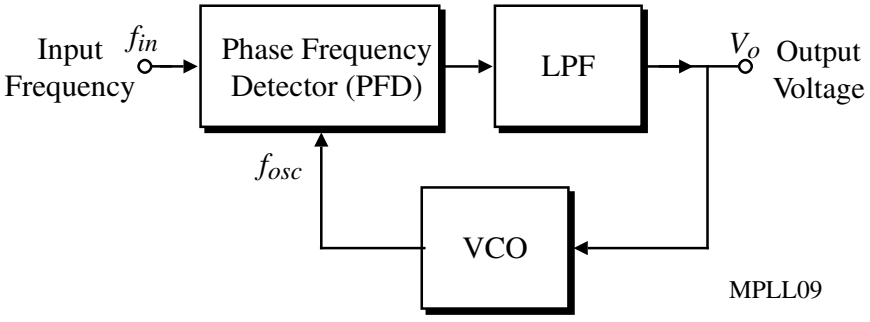
- Phase-locked loops
- Summary

PHASE-LOCKED LOOPS

Components of a Phase-Locked Loop

Function of a phase-locked loop is to lock the frequency of a VCO to an input frequency.

Block diagram:



Components:

- Phase/frequency detector outputs a signal that is proportional to the difference between the frequency/phase of two input periodic signals.
- The low-pass filter is use to reduce the phase noise and enhance the spectral purity of the output.
- The voltage-controlled oscillator takes the filtered output of the PFD and generates an output frequency which is controlled by the applied voltage.

Phase/Frequency Detectors

Types:

- Analog multipliers
- Exclusive OR gates
- Sequential phase detectors

Analog Multiplier as a Phase Detector

Diagram:

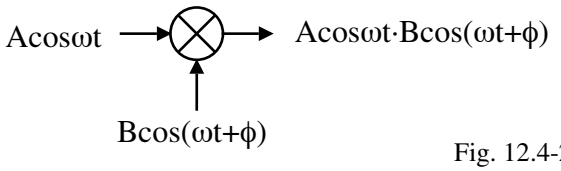


Fig. 12.4-2B

Note that

$$AB\cos(\omega t)\cos(\omega t+\phi) = \frac{AB}{2}\{\cos(\phi) - \cos(2\omega t+\phi)]$$

If we look only at the low frequency or dc component, the output of the multiplier is

$$V_{out} = \frac{AB}{2}\cos(\phi)$$

and is a phase detector.

Phase detector gain "constant" is given as

$$K_D = \frac{d}{dt}(V_{out}) = -\frac{AB}{2}\sin(\phi) \text{ (V/rad.)}$$

Note that K_D is zero when ϕ is zero and greatest when ϕ is ±90°. To maximize the useful phase range, the loop should be arranged to lock to a phase difference of 90°. This is a *quadrature* phase detector.

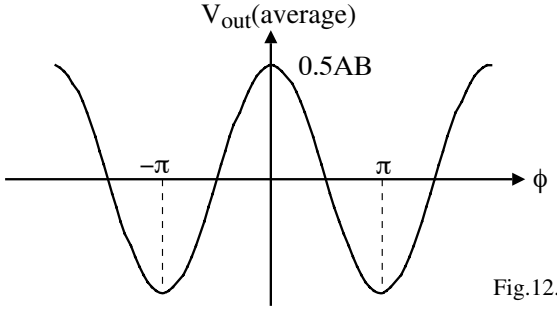


Fig.12.4-2C

Analog Modulator as a Phase Detector

Diagram:

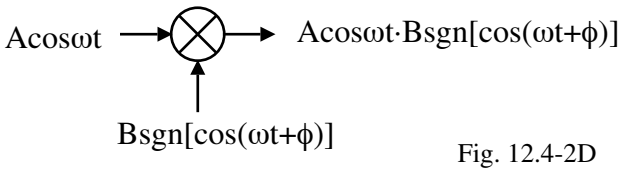


Fig. 12.4-2D

Note that $sgn(x) = 1$ if $x>0$ and -1 if $x<0$.

$$V_{out}(\text{average}) = \frac{4}{\pi}\frac{AB}{2}cos(\phi) = \frac{2}{\pi}ABcos(\phi)$$

Notice that the gain of this phase detector is $4/\pi$ larger than the multiplier phase detector.

Phase detector gain "constant" is given as

$$K_D = \frac{d}{dt}(V_{out})\Big|_{\phi=\pi/2} = -\frac{2}{\pi}AB$$

Comment:

Because the modulator phase detector has more than just the fundamental, it can lock on to a harmonic or subharmonic of the fundamental (which may be desirable or undesirable).

Exclusive-OR-gate as a Phase Detector

Waveforms:

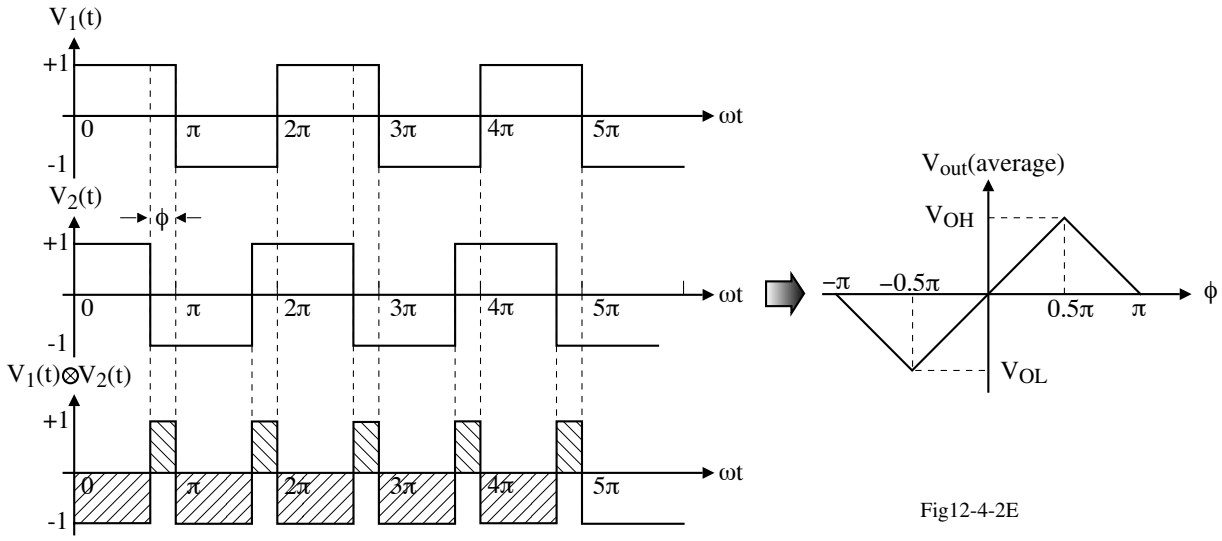


Fig12-4-2E

$$V_{out}(\text{average}) = V_{OL} + \frac{V_{OH} - V_{OL}}{\pi}\phi \quad \Rightarrow \quad K_D = \frac{V_{OH} - V_{OL}}{\pi}$$

Sequential Phase Detectors

Sequential phase detectors generate error voltages proportional to the phase difference by detecting the zero crossing of the input and VCO signals.

SR flip-flop implementation:

Positive going one sets the flip-flop, Negative going one resets it.

Average output voltage:

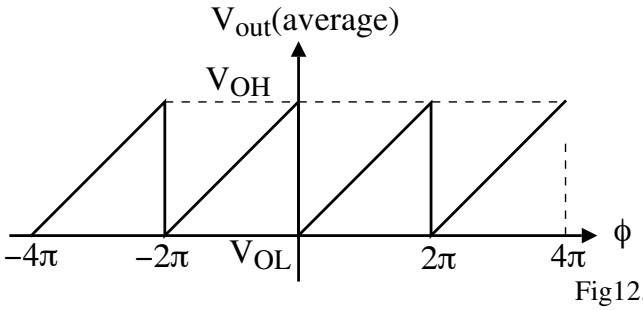


Fig12.4-2F

$$K_D = \frac{V_{OH} - V_{OL}}{2\pi}$$

Phase Detectors Versus Frequency Detectors

A frequency detector determines the difference between two frequencies.

Multiplier detectors cannot detect frequency differences.

Sequential phase detectors can detect both frequency and phase difference (PFD)

Example of an extended range phase-frequency detector:

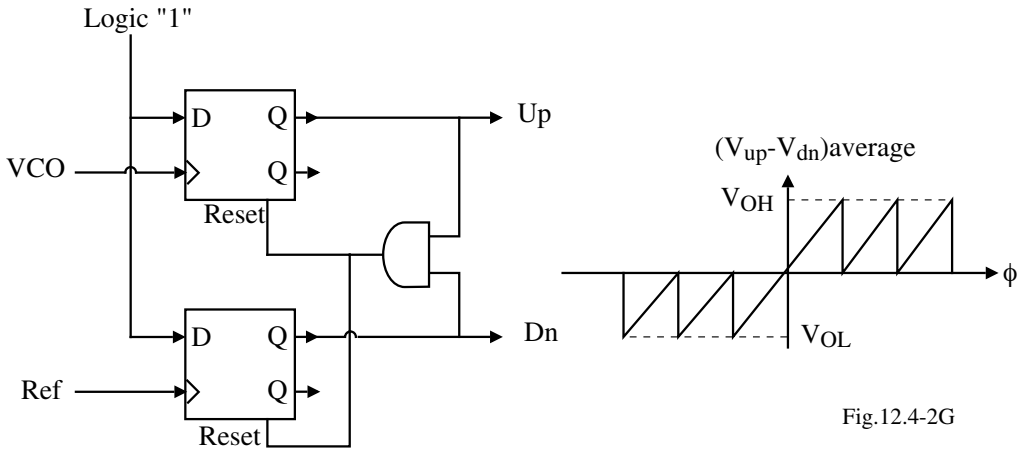


Fig.12.4-2G

Other PFD's[†]

[†] C.R. Hogge, "A Self-Correcting Clock Recovery Circuit," *J. Lightwave Technology*, vo. LT-3, no. 6, 1985, pp. 1312-14.

Capture Process of a Phase Locked Loop

In the unlocked condition, the VCO runs at the frequency corresponding to zero applied dc voltage at its input. This frequency is called the *free running frequency.*

The capture process is the means by which the loop goes from the unlocked, free-running condition to that of being locked on a signal.

Illustration:

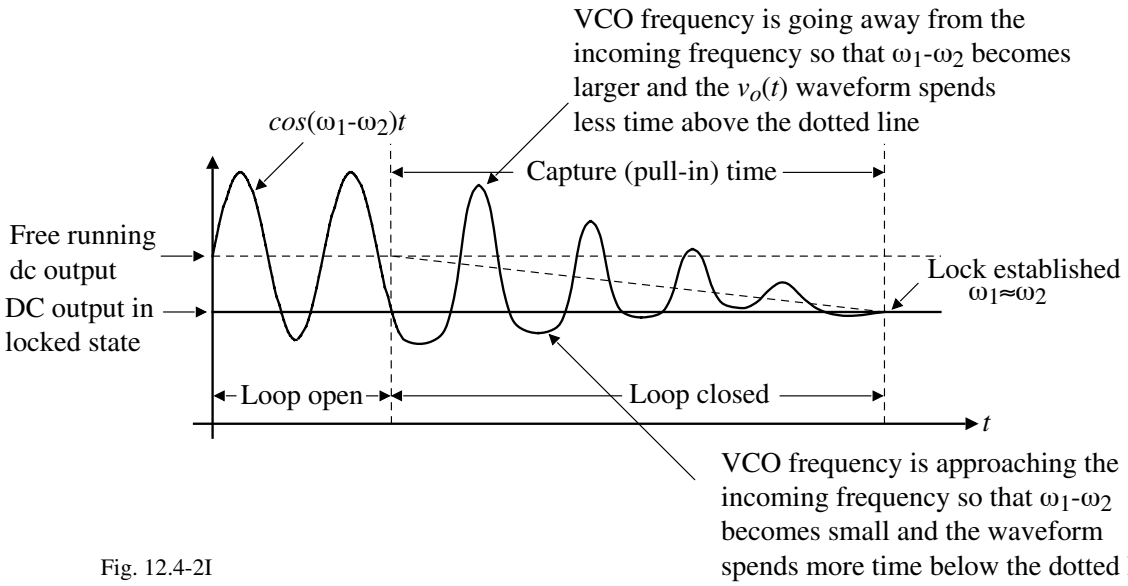


Fig. 12.4-2I

Loop Filters

Loop filter:

Used to reduce the unwanted components in the phase locked loop.

Consider a PLL under locked conditions:

Block diagram-

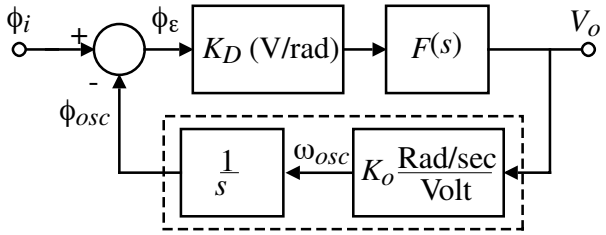


Fig. 12.4-2H

Define,

$$\omega_{osc} = \omega_o + K_o V_o \qquad \text{and} \qquad \omega_{osc} = \frac{d\phi_{osc}}{dt} \quad \rightarrow \quad \phi_{osc} = \frac{1}{s}\,\omega_{osc}$$

where

ω_o = free running frequency of the VCO

It can be shown that,

$$\frac{V_o}{\phi_i} = \frac{sK_D F(s)}{s + K_D K_o F(s)} \qquad \text{or} \qquad \frac{V_o}{\omega_i} = \frac{V_o}{s\phi_i} = \frac{K_D F(s)}{s + K_D K_o F(s)}$$

Loop Filters - Continued

Loop Filter removed:

$$\frac{V_o}{\omega_i} = \frac{1}{K_o}\left(\frac{K_v}{s + K_v}\right)$$

where,

$$K_v = \text{Loop bandwidth} = K_o K_D \left(\frac{\text{rad/sec}}{\text{volt}}\right)\left(\frac{\text{volt}}{\text{rad}}\right) = \frac{1}{\text{sec}}$$

Influences of a decrease in loop bandwidth:

1.) Capture process becomes slower and the capture time increases.

2.) Capture range decreases.

3.) Interference rejection properties of the PLL improve.

4.) Transient response of the loop is underdamped.

Frequency dynamics:

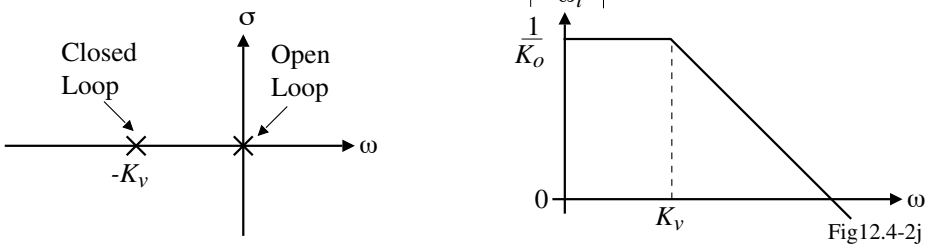


Fig12.4-2j

Loop Filters - Continued

Example:

If $K_o = 2\pi(1\text{kHz/Volt})$, $K_v = 500\ (\text{sec}^{-1})$ and $\omega_o = 1000\pi$ rads/sec ($f_o = 500$Hz),

(a.) Find V_o for $f_i = 250$Hz and 1000Hz.

(b.) What is the time constant of V_o for a step change between these two frequencies?

Solution

(a.) We know from the above that

$$\omega_{osc} = \omega_i = \omega_o + K_o V_o \qquad \rightarrow \qquad V_o = \frac{\omega_i - \omega_o}{K_o}$$

$$\therefore \qquad V_o(250\text{Hz}) = \frac{250\text{-}500}{1000} = -0.25\text{V}$$

$$V_o(1000\text{Hz}) = \frac{1000\text{-}500}{1000} = +0.5\text{V}$$

(b.) $\tau = \frac{1}{K_v} = 2\text{ms}$

Loop Filters - Continued

Example:

For the PLL of the previous example, find $v_o(t)$ if the input signal is frequency modulated so that

$$\omega_i(t) = 2\pi(500\text{Hz})[1+0.1\sin(2\pi\text{x}10^2)t].$$

Solution

Error!

$$|\omega_i(j\omega)| = 0.1(1000\pi) = 100\pi = 50(2\pi)$$

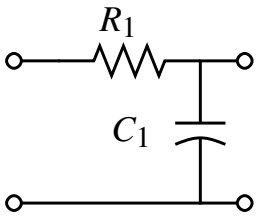
$$\therefore \quad V_o(j\omega) = \frac{50}{1000}(0.39\text{-}j0.48) = \frac{50}{1000}\,0.62\angle\text{-}51^\circ = 0.031\angle\text{-}51^\circ$$

or

$$v_o(t) = 0.031\,\sin[(2\pi\text{x}10^2)\text{-}51^\circ]$$

Higher Order Loop Filters

Let $F(s) = \dfrac{\omega_1}{s+\omega_1} = \dfrac{1}{1+\dfrac{s}{\omega_1}}$



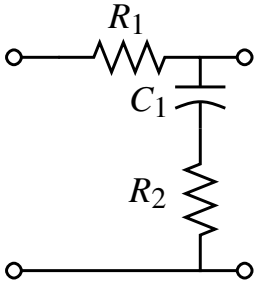


Fig.12.4-02L

$$\therefore \quad \frac{V_o(s)}{\omega_i} = \frac{K_D F(s)}{s + K_v F(s)}$$

$$= \frac{K_D}{s\left(1+\dfrac{s}{\omega_1}\right) + K_v} = \frac{1}{K_o}\left(\frac{\omega_1 K_v}{s^2+\omega_1 s+\omega_1 \cdot K_v}\right)$$

The poles are,

$$p_1,p_2 = -\frac{\omega_1}{2} \pm \frac{1}{2}\sqrt{\omega_1{}^2 - 4\omega_1 \cdot K_v} = -\frac{\omega_1}{2}\left(1 \pm \sqrt{1 - \frac{4K_v}{\omega_1}}\right)$$

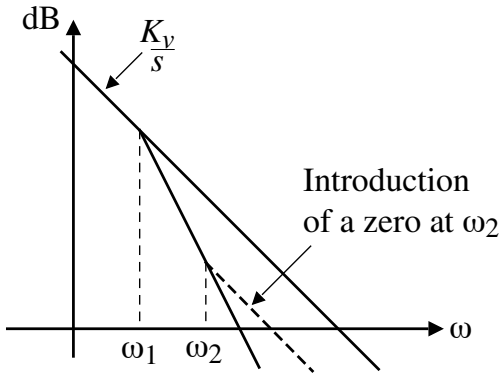
A standard second-order low-pass response form is

$$\frac{V_o(j\omega)}{\omega_i} = \frac{1}{K_o}\left(\frac{\omega_n{}^2}{s^2 + \zeta\omega_n s + \omega_n{}^2}\right) \qquad \text{where } \omega_n = \sqrt{K_v\omega_1} \quad \text{and} \quad \zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{K_v}}$$

A Butterworth response has ζ=0.707 which gives ω_1=2K_v. Therefore $\omega_{\text{-3dB}}=\omega_n=\sqrt{2}K_v$

Higher Order Loop Filters - Continued

Illustration:



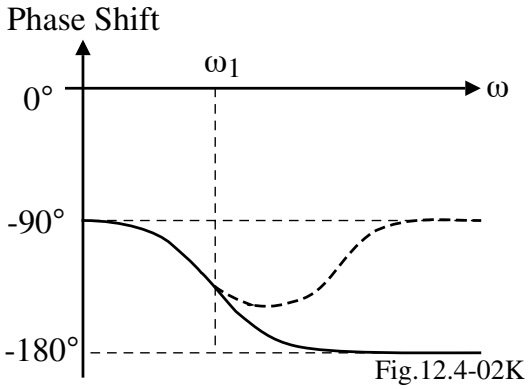


Fig.12.4-02K

Loop Lock Range

($\omega_i = \omega_{osc}$)

The loop lock range is the range of frequencies about ω_o for which the PLL maintains $\omega_i = \omega_{osc}$.

I.e.,

$$\omega_L = \pm\Delta\omega_{osc} = K_D K_o\left(\frac{\pm\pi}{2}\right) = \pm K_v\left(\frac{\pi}{2}\right)$$

where $\pm\pi/2$ is the phase detector limits.

Capture Range

The capture range, ω_C, is the range of input frequencies for which an initially unlocked loop will lock on an input signal of ω_i.

In general:

- If $F(s) = 1$, then $\omega_C \approx \omega_L$.
- If $F(s) = \dfrac{1}{1 + \dfrac{s}{\omega_1}}$, then $\omega_C < \omega_L$

Tracking characteristics:

Error Voltage = PLL output voltage for any f_i-PLL output voltage at $f_i = f_{osc} = f_o$

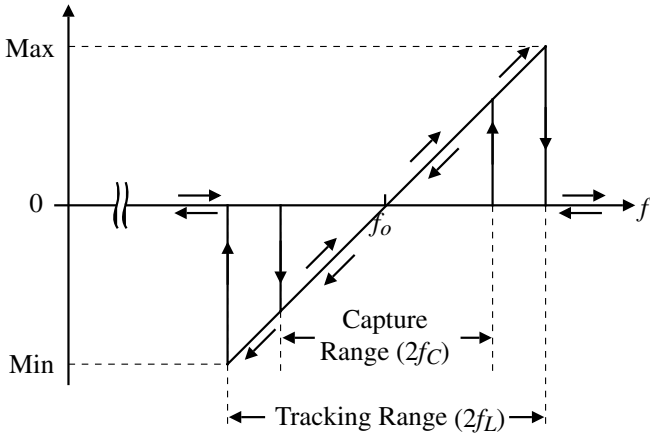


Fig12.4-2M

Charge Pumps[†]

In PLLs with a filter, the average value of the PFD output is obtained by depositing charge onto a capacitor during each phase/frequency comparison and allowing the charge to decay afterwards.

A ideal charge pump combined with the PFD provides an infinite dc gain with passive filters, which results in the unbounded pull-in range for second-order and higher-order PLLs.

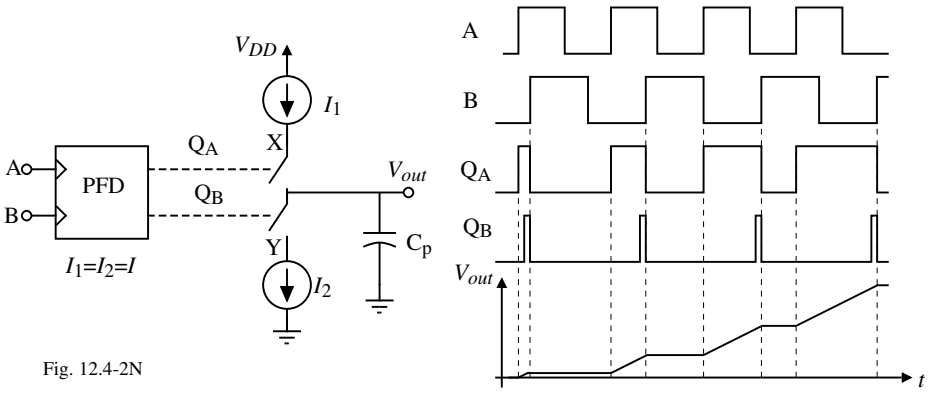


Fig. 12.4-2N

Q_A high deposits charge on C_p (A leads B).

Q_B high removes charge from C_p (B leads A).

Q_A and Q_B low V_{out} remains constant.

[†] B. Razavi, "Design of Monolithic Phase-Locked Loops and Clock Recovery Circuits-A Tutorial", *IEEE Press*.

Charge Pumps - Nonidealities[†]

Leakage current:

Small currents that flow when the switch is off.

Mismatches in the Charge Pump:

The up and down (charge and discharge) currents are unequal.

Timing Mismatch in PFD:

Any mismatch in the time at which the PFD provides the up and down outputs.

Types of Charge Pumps

- Conventional Tri-Stage
  Low power consumption, moderate speed, moderate clock skew
  Low power frequency synthesizers, digital clock generators
- Current Steering
  Static current consumption, high speed, moderate clock skew
  High speed PLL (>100MHz), translation loop, digital clock generators
- Differential input with Single-Ended output
  Medium power, moderate speed, low clock skew
  Low-skew digital clock generators, frequency synthesizers
- Fully Differential
  Static current consumption, high speed (>100MHz)
  Digital clock generators, translation loop, frequency synthesizer (with on-chip filter)

[†] Woogeun Rhee, "Design of High-Performance CMOS Charge Pumps in Phase-Locked Loops," *Proc. of 1999 ISCAS*, pp. II-545-II548, May 1999.

Charge Pumps

The low pass filter in the PLL can be implemented by:

1.) Active filters which require an op amp

2.) Passive filters and a charge pump.

The advantages of a charge pump are:

- Reduced noise
- Reduced power consumption
- No offset voltage

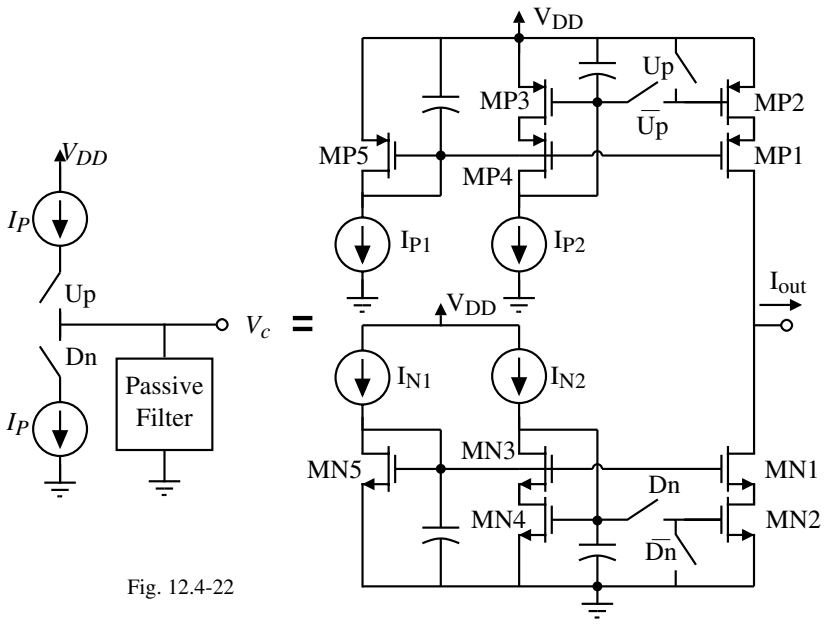


Fig. 12.4-22

SUMMARY

Phase-Locked Loops

- Phase/frequency detectors
- Loop filters
- Charge pumps
- Capture and lock ranges