COURSE DETAILS AND INFORMATION FOR ECE6412 – ANALOG INTEGRATED CIRCUIT DESIGN II

Instructors: Dr. Phillip E. Allen, Room 292B, Van Leer, 894-6251 (office), (404) 603-9374 (home), pallen@ece.gatech.edu

Dr. Gabriel Rincon-Mora, Room 262, Van Leer, 385-2768 (office)

Lecture: Monday, Wednesday, and Friday, 10:05am to 10:55am, Room C341, Van Leer

Office Hours: Allen: 2-3pm, MW, 2-3pm F or by e-mail <pallen@ece.gatech.edu>.

Rincon-Mora: 10-11am Th and 1-2pm F in Room 308, Van Leer

Electronic Copies of Class Handouts: You may download pdf copies of all classroom material at the following web site: http://users.ece.gatech.edu/~pallen/Academic/ Other resources are available at: http://rincon-mora.com/classes/resources.htm

Prerequisite: EE 4430 Analog Integrated Circuit Design I or permission of instructor.

Texts:

Analysis and Design of Analog Integrated Circuits – Fourth Edition, Paul Gray, Paul Hurst, Steve Lewis and Robert Meyer, John Wiley and Sons, Inc., 2001

CMOS Analog Circuit Design – Second Edition, P.E. Allen and D.R. Holberg, Oxford University Press, 2002.

Objectives: The purpose of this course is to enable the student to model, analyze and design analog integrated circuits using bipolar and/or MOS technologies. At the conclusion of the course, the student should be able to successfully perform the electrical and physical design of an op amp or analog circuit of similar complexity in an industrial environment.

Examinations: There will be three, closed book midterm examinations each of 50 minute duration and a 3 hour final examination. The final examination will be given during the regularly scheduled time for the final exam. All grades become final one week after they are returned in class.

Final Exam: The final exam is on Tuesday, April 27, 2004, from 2:50pm to 5:40pm.

Homework: Homework will be assigned and will be graded.

Course Grading Policy: Your grade will be determined using the following scheme:

Three midterm exams……..	60%
Homework……	10%
Final Exam……	30%

Grades will be assigned on a curve and will not necessarily be consistent with 100>A>90, 90>B>80, etc..

Computer Usage: You are expected to be able to use HSPICE or PSPICE for classroom assignments. Most assignments using the computer will work on the student version of PSPICE. The educational version of PSpice for the PC is free and downloadable from:

http://www.orcad.com/products/pspice/eval_f.htm

Attendance: You are responsible for all course materials, announcements, notes, etc. made during our regular class meeting times. Prompt arrival to class is appreciated.

Academic Honesty: It is the responsibility of the instructor to encourage an environment where you can learn and your accomplishments will be rewarded fairly. Any behavior that compromises the basic rules of academic honesty as described in the General Catalog will not be tolerated.

Classroom Behavior: Smoking, drinking and eating is prohibited in the classroom by Institute rules.

Weekly Coverage of Topics for ECE6412

Week	Date	Lect. #	Topic	GHLM	AH
	1/5	010A	Introduction, ECE 4430 Review	1-75	-
1	1/7	020A	ECE 4430 Review, Continued	78-154	-
	1/9	030A	ECE 4430 Review, Continued	170-336	-
	1/12	040A	Common source, common emitter	384-398	218-221
2	1/14	050A	Followers	344-362	221-226
	1/16	060A	Push-pull output stages	362-384	226-229
	1/19		Holiday		
3	1/21	070A	Frequency response, single stage I	488-504	-
	1/23	080A	Frequency response, single stage II	504-516	-
	1/26	090R	Multiple-atage frequency response I	516-527	-
4	1/28	100R	Multiple-stage frequency response II	527-537	-
	1/30	110R	Introduction and characterization of the op amp	404-424	243-249
	2/2	120A	Compensation of Two-Stage Op Amps	425-434	249-260
5	2/4	130A	Compensation of Two-Stage Op Amps	638-652	260-269
	2/6	140A	Simple CMOS op amps	425-434	249-253
	2/9		Examination No. 1		
6	2/11	150A	Simple BJT op amps	425-434 453-454	249-253
	2/13	160A	MOSFET Op Amp Design	472-480	269-286
	2/16	170R	Intuitive analysis of analog circuits	472-480	269-286
7	2/18	180R	Power supply rejection ratio	-	286-293
	2/20	190R	Cascode op amps-I	434-439	293-309
	2/23	200R	Cascode op amps-II	443-453	293-309
8	2/25	210R	DC analysis of the 741 op amp	454-462	-
	2/27	220R	AC analysis of the 741 op amp	462-472	-
	3/1	230R	741 frequency response	537-544	-
9	3/3	240R	Simulation and measurement of op amps	579-587	310-323
	3/5	250R	Introduction to feedback concepts	553-563	-
	3/8- 3/12		Spring Break		
	3/15		Examination No. 2		
11	3/17	260R	Shunt-shunt feedback	563-569	-
	3/19	270R	Series-series feedback	569-579	-
	3/22	280R	Series-shunt and shunt-series feedback	579-587	-
12	3/24	290R	Feedback circuit analysis using return ratio	599-613	-
	3/26	300A	Buffered op amps	-	384-393
	3/29	310A	High speed/frequency op amps	-	368-384
13	3/31	320A	Differential output op amps	808-857	384-393
	4/2	330A	Low power op amps	-	393-402
	4/5	340A	Low noise op amps	788-798	402-414
14	4/9	350A	Low voltage op amps	-	415-432
	4/9	360A	Characterization of comparators		439-444
	4/12		Examination No. 3		
15	4/14	370R	Two-stage, open-loop comparators-I	-	445-461
	4/16	380R	Two-stage, open-loop comparators-II	-	445-461
	4/19	390R	Open-loop comparators	-	461-475
16	4/21	400R	Discrete-time comparators	-	475-483
	4/23	410R	High-speed comparators	-	483-488
The final exam is scheduled for Tuesday, April 27, 2004, from 2:50pm to 5:40pm.					