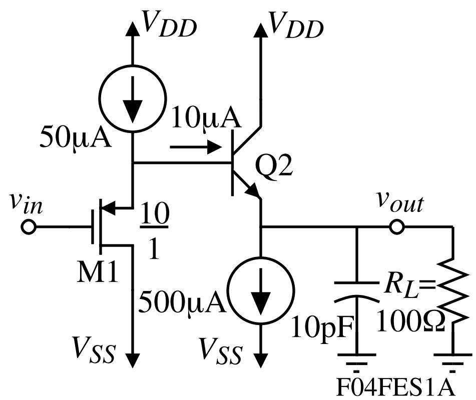
FINAL EXAMINATION - SOLUTIONS

(Average score = 81/100)

Problem 1 - (20 points - This problem is required)

An output stage is shown. Assume the parameters of the NMOS transistors are K_N'=110μA^2/V, V_{TN} = 0.7V, λ_N=0.04V^{-1}, the PMOS transistors are K_P'=50V/μA^2, V_{TP} = -0.7V, λ_P=0.05V^{-1} and the lateral npn BJT has a current gain of β_F = 50 and V_t = 25mV. Find the small-signal output resistance (not including R_L), the small-signal voltage gain (ignore the bulk effect on M1), and the large signal slew rate (plus and minus) if a 10pF capacitor is connected to the output.



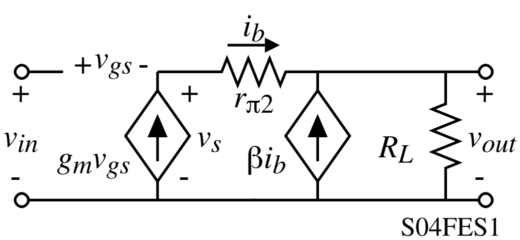
Solution

Model parameters:

M1: $g_{m1} = \sqrt{2\cdot 40\cdot 10\cdot 50} = 0.2\text{mS}$

Q2: $g_{m2} = \dfrac{500\mu\text{A}}{25\text{mV}} = 20\text{mS}$ and $r_{\pi 2} = \dfrac{51}{20\text{mS}} = 2.55\text{k}\Omega$

Small-signal model:



$$R_{out} = \frac{r_{\pi 2}+(1/g_{m1})}{1+\beta} = \frac{2.55\text{K}+5\text{K}}{51} = \underline{148\Omega}$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_{out}}{i_b}\right)\left(\frac{i_b}{v_{gs}}\right)\left(\frac{v_{gs}}{v_{in}}\right)$$

$$= [(1+\beta)R_L](g_{m1})\left(\frac{1}{1+g_{m1}[r_{\pi 2}+(1+\beta)R_L]}\right)$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}[(1+\beta)R_L]}{1+g_{m1}[r_{\pi 2}+(1+\beta)R_L]}\right) = \frac{0.2\text{mS}\cdot 101\cdot 100\Omega}{1+0.2\text{mS}(2.55\text{k}\Omega+5.1\text{k}\Omega)} = \frac{1.20}{2.53} = \underline{0.403\text{V/V}}$$

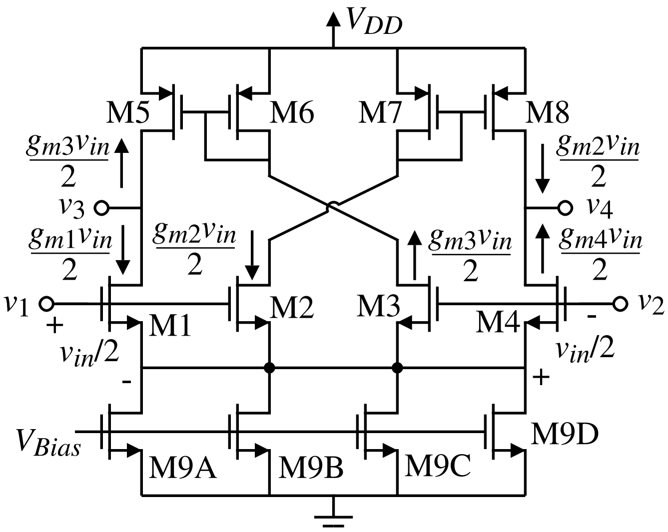
Slew rates:

$$SR^+ = \frac{50\mu\text{A}(51) - 50\mu\text{A}}{10\text{pF}} = \underline{205\text{ V}/\mu\text{s}}$$

$$SR^- = \frac{500\mu\text{A}}{10\text{pF}} = \underline{-50\text{ V}/\mu\text{s}}$$

Problem 2 - (20 points - This problem is optional)

A differential-in, differential-out amplifier is shown that eliminates the need for matching sinks and sources. Assume that all W/L values are equal and that each transistor has approximately the same current flowing through it. If all transistors are in the saturation region, find an algebraic expression for the voltage gain, v_{out}/v_{in}, and the differential output resistance, R_{out}, where $v_{out} = v_3 - v_4$ and $v_{in} = v_1 - v_2$. R_{out} is the resistance seen between the output terminals.



Solution

Using the schematic approach to small signal analysis, we apply $v_{in}/2$ positively to M1 (M2) and negatively to M4 (M3). The resulting ac currents are shown on the schematic. At node, v_3, these currents flow out of a resistance whose value is $r_{ds1}||r_{ds5}$ to give v_3 as

$$v_3 = -\left(\frac{g_{m1}+g_{m3}}{2(g_{ds1}+g_{ds5})}\right) v_{in} = \frac{-g_{m1}v_{in}}{g_{ds1}+g_{ds5}}$$

Similarly for v_4, we get

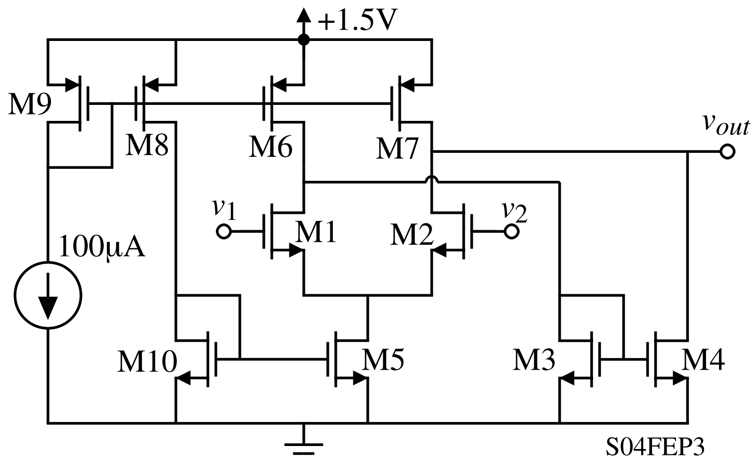
$$v_4 = \left(\frac{g_{m2}+g_{m4}}{2(g_{ds2}+g_{ds8})}\right) v_{in} = \frac{g_{m2}v_{in}}{g_{ds2}+g_{ds8}} \Rightarrow \boxed{\frac{v_{out}}{v_{in}} = -\frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds5}} = -\frac{g_{m1}+g_{m2}}{g_{ds4}+g_{ds8}}}$$

The output resistance seen differentially is the sum of the resistances seen to ground which is

$$\boxed{R_{out} = \frac{1}{g_{ds1}+g_{ds5}} + \frac{1}{g_{ds4}+g_{ds8}} = r_{ds1}||r_{ds5} + r_{ds4}||r_{ds8}}$$

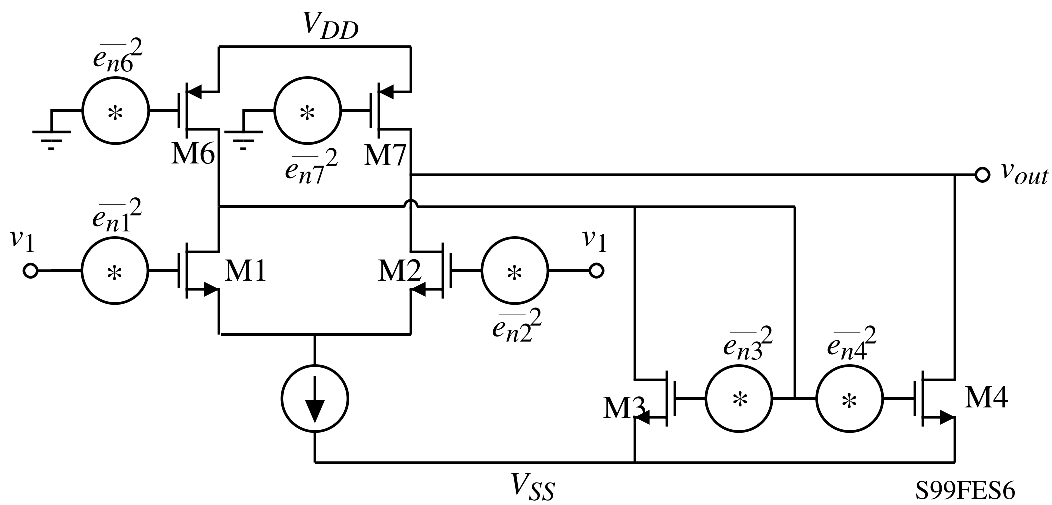
<u>Problem 3 - (20 points - This problem is optional)</u>

Find an expression for the equivalent input noise voltage of the circuit in the previous problem, $\overline{e_{eq}^2}$, in terms of the small signal model parameters and the individual equivalent input noise voltages, $\overline{e_{ni}^2}$, of each of the transistors (i = 1 through 7). Assume M1 and M2, M3 and M4, and M6 and M7 are matched.



<u>Solution</u>

Equivalent noise circuit:



$$\overline{e_{out}^2} = (g_{m1}^2\overline{e_{n1}^2} + g_{m2}^2\overline{e_{n2}^2} + g_{m3}^2\overline{e_{n3}^2} + g_{m4}^2\overline{e_{n4}^2} + g_{m5}^2\overline{e_{n6}^2} + g_{m6}^2\overline{e_{n7}^2})R_{out}^2$$

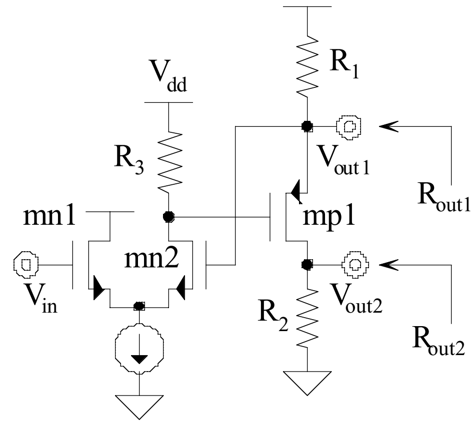
$$\overline{e_{eq}^2} = \frac{\overline{e_{out}^2}}{(g_{m1}R_{out})^2} = \overline{e_{n1}^2} + \overline{e_{n2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2(\overline{e_{n3}^2} + \overline{e_{n4}^2}) + \left(\frac{g_{m6}}{g_{m1}}\right)^2(\overline{e_{n6}^2} + \overline{e_{n7}^2})$$

If M1 through M2 are matched then $g_{m1} = g_{m2}$ and we get

$$\overline{e_{eq}^2} = 2\,\overline{e_{n1}^2} + 2\left(\frac{g_{m3}}{g_{m3}}\right)^2\overline{e_{n3}^2} + 2\left(\frac{g_{m6}}{g_{m1}}\right)^2\overline{e_{n6}^2}$$

Problem 4 - (20 points - This problem is optional)

Assuming the transconductance and output resistance of mp1, mn1, and mn2 are g_{mp1}, g_{mn1}, g_{mn2}, r_{sdp1}, r_{dsn1}, and r_{dsn2}, respectively, and that R_1, R_2, and R_3 are much smaller than r_{ds1}, r_{ds2}, and r_{ds3}, answer the following questions:



(a) Determine the type of mixing being employed by the circuit.

(b) Determine the type of sampling being employed at V_{out1}.

(c) Determine the type of sampling being employed at V_{out2}.

(d) Determine the loop gain of the circuit.

(e) Determine the open-loop resistance at V_{out1}.

(f) Determine the open-loop resistance at V_{out2}.

(g) Assuming the loop gain is infinite, what is the closed-loop gain from V_{in} to V_{out2}?

Solution

(a) Series

(b) Shunt

(c) Series

(d) Open loop at inverting input of Op-Amp (gate of mn2):

$$LG = \frac{-g_{mn2}R_3}{2} * \frac{g_{mp1}R_1}{1 + g_{mp1}R_1}$$

(e) $R_{out1\_ol} = R_1 \parallel (1/g_{mp1}) \approx 1/g_{mp1}$

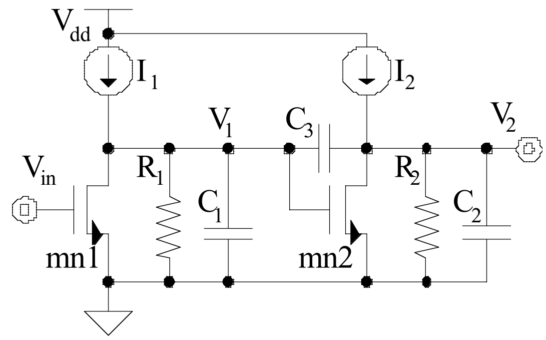
(f) $R_{out2\_ol} = R_2 \parallel R_x = R_2 \parallel \{r_{ds1}\,(g_{mp1}R_1 + 1) + R_1\} \approx R_2 \parallel (r_{ds1}g_{mp1}R_1)$

(g) $V_+ \approx V_- = v_{gn1} = v_{gn2} = v_{in}$ & remembering that V_{dd} = ac ground,

$\rightarrow v_{out2} / v_{in} = (v_{out2} / i_{R1})\,(i_{R1} / v_{gn1})\,(v_{gn1} / v_{in}) \approx (v_{out2} / i_{R1})\,(i_{R1} / v_{gn1})\,(\,1\,)$

$= (-R_2)\,(1/R_1)$

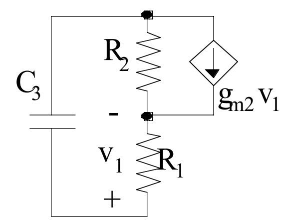
Problem 5 - (20 points - This problem is optional)



Assuming mn1, mn2, I_1, and I_2 are ideal (r_{out} and r_{ds} → ∞, and C_{gs}, C_{dg}, and C_{db} are all negligible), use either the Short-Circuit or the Open-Circuit Time-Constant test to determine (a) the dominant pole of the circuit (lowest, high-frequency pole) and (b) the second dominant pole. In doing part (b), state which capacitor determines the second dominant pole (intuitively), then derive it. Also assume R_1 = R_2 = 1M_, C_3 = C_2 = 10pF, C_1 = 0.1pF, and g_{m1} = g_{m2} = 10µS. Do NOT use any other means to determine the answer and show your work.

Solution

(a) Open-Circuit Time Constant Test



$R_3'C_3$ → $R_3' = R_2(1 + g_{m2}R_1) + R_1 \approx R_2R_1g_{m2}$ = 10M_

R_3C_3 = 100µs → W = 10k rad/s → f = 1.59kHz

$R_2'C_2 = R_2C_2$ = 10µs → W = 100k rad/s → f = 15.9kHz

$R_1'C_1 = R_1C_1$ = 0.1µs → W = 10M rad/s → f = 1.59MHz

Thus, $W_{dominant}$ = 10k rad/s or $f_{dominant}$ = 1.59kHz

(b) Short-Circuit Time Constant Test

Neglect C_1 since it is much smaller than C_2 → 2nd pole is determined by C_2.

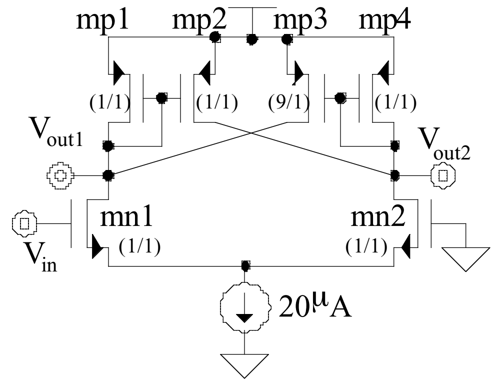
$R_3'C_3 = R_1C_3$ = 10µs → W = 100k rad/s → f = 15.9kHz

$R_2'C_2 = \{(1/g_{m2})||R_2\}C_2 \approx C_2/g_{m2}$ = 1µs → W = 1M rad/s → f = 159kHz

Thus, $W_{2\text{-}dominant}$ = 1M rad/s or $f_{2\text{-}dominant}$ = 159kHz

Problem 6 - (20 points - This problem is optional)

Assuming transconductance parameter K', small-signal output resistance r_{ds}, and threshold voltage V_T of all transistors are $100\mu A/V^2$, ∞, and 0.6V, respectively, answer the following questions (ignore bulk effects):



(a) Identify the transistors in the ac-signal path of the positive feedback loop.

(b) What type of sampling is being employed at V_{out1} and V_{out2}?

(c) Based on the answers of (a) and (b), is the feedback circuit increasing or decreasing the effective output resistance at V_{out1} and V_{out2}?

(d) Determine the rising threshold voltage (V_{th+}) of the circuit.

(e) Determine the falling threshold voltage (V_{th-}) of the circuit.

Solution

(a) mp1, mp2, mp4, and mp3.

(b) Shunt and Shunt.

(c) Since it is shunt + fb, V_{out1} and V_{out2} are both increased.

(d) Rising → $i_{mn1} = i_{mp3} = 9i_{mn2}$ & $i_{mn1} + i_{mn2} = 20\mu A$ → $i_{mn2} = 2\mu A$ and $i_{mn1} = 18\mu A$

$V_{th+} - V_{gs1} + V_{gs2} = 0$ → $V_{th+} = V_{gs1} - V_{gs2} = \text{sqrt}(2i_{mn1} / K') - \text{sqrt}(2i_{mn2} / K')$

$= \text{sqrt}(36/100) - \text{sqrt}(4/100) = 0.4V$

(e) Falling → $i_{mn2} = i_{mp2} = i_{mn1}$ & $i_{mn1} + i_{mn2} = 20\mu A$ → $i_{mn2} = 10\mu A$ and $i_{mn1} = 10\mu A$

Since the currents equal, their V_{gs}'s also equal and $V_{th-} = 0V$