FINAL EXAMINATION

NAME_____SCORE_____/100

Problem	①	2	3	④	5	6	7	Total Points
Score								

INSTRUCTIONS: This exam is closed book with four sheets of notes permitted. Your four sheets of notes should not contain any previous ECE 6412 exam or final exam problems. The exam consists of 7, 20-point problems of which you are to work only 5 for a total of 100 points. You must attempt problems 1 and 4. All other problems are optional. **Please circle the number in the table above of the remaining three problems you wish graded.** If you do not indicate the problems to be graded, then problems 1 through 6 will be graded regardless of whether they are worked or not. Be sure to turn in only the 6 problems you wish graded in proper numerical order. Please show your work leading to your answers so that maximum partial credit may be given where appropriate.
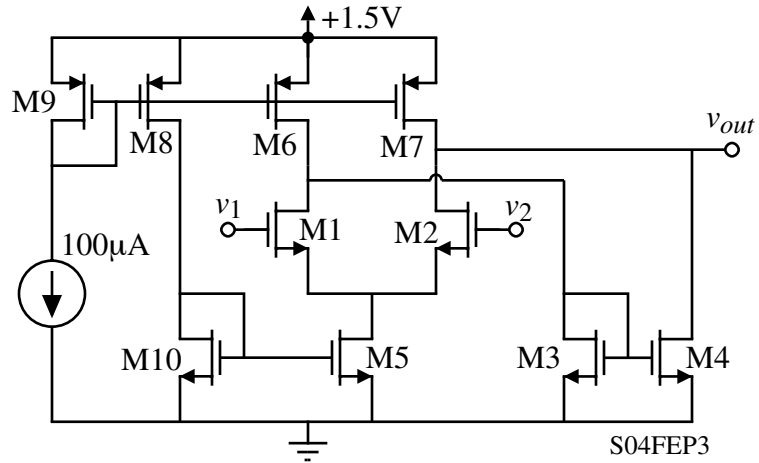
Problem 1 - (20 points - This problem is required)

An output stage is shown. Assume the parameters of the NMOS transistors are K_N'=110V/μA^2, V_{TN} = 0.7V, λ_N=0.04V^{-1}, the PMOS transistors are K_P'=50V/μA^2, V_{TP} = -0.7V, λ_P=0.05V^{-1} and the lateral npn BJT has a current gain of β_F = 50 and V_t = 25mV. Find the small-signal output resistance (not including R_L), the small-signal voltage gain (ignore the bulk effect on M1), and the large signal slew rate (plus and minus) if a 10pF capacitor is connected to the output.

Problem 2 - (20 points - This problem is optional)

A differential-in, differential-out amplifier is shown that eliminates the need for matching sinks and sources. Assume that all W/L values are equal and that each transistor has approximately the same current flowing through it. If all transistors are in the saturation region, find an algebraic expression for the voltage gain, v_{out}/v_{in}, and the differential output resistance, R_{out}, where $v_{out} = v_3 - v_4$ and $v_{in} = v_1 - v_2$. R_{out} is the resistance seen between the output terminals.

S04FEP2

Problem 3 - (20 points - This problem is optional)

Find an expression for the equivalent input noise voltage of the circuit in the previous problem, $\overline{e}^2_{eq}$, in terms of the small signal model parameters and the individual equivalent input noise voltages, $\overline{e}^2_{ni}$, of each of the transistors (i = 1 through 7). Assume M1 and M2, M3 and M4, and M6 and M7 are matched.

S04FEP3

Problem 4 - (20 points - This problem is required)

Assuming the transconductance and output resistance of mp1, mn1, and mn2 are g_{mp1}, g_{mn1}, g_{mn2}, r_{sdp1}, r_{dsn1}, and r_{dsn2}, respectively, and that R_1, R_2, and R_3 are much smaller than r_{ds1}, r_{ds2}, and r_{ds3}, answer the following questions:

(a) Determine the type of mixing being employed by the circuit.

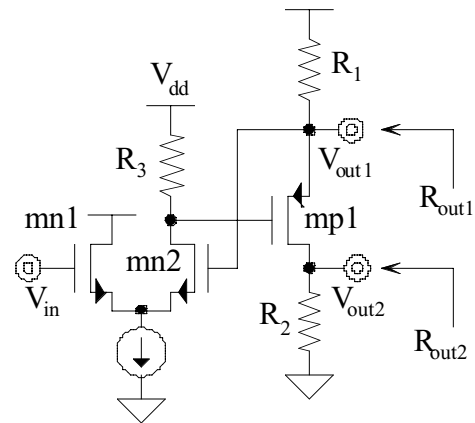(b) Determine the type of sampling being employed at V_{out1}.

(c) Determine the type of sampling being employed at V_{out2}.

(d) Determine the loop gain of the circuit.

(e) Determine the open-loop resistance at V_{out1}.

(f) Determine the open-loop resistance at V_{out2}.

(g) Assuming the loop gain is infinite, what is the closed-loop gain from V_{in} to V_{out2}?

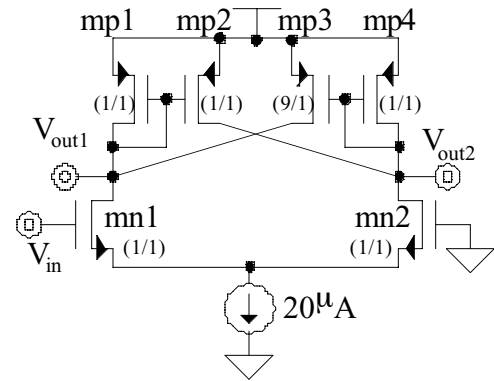## Problem 5 - (20 points - This problem is optional)

Assuming mn1, mn2, I_1, and I_2 are ideal (r_{out} and $r_{ds} \rightarrow \infty$, and C_{gs}, C_{dg}, and C_{db} are all negligible), use either the Short-Circuit or the Open-Circuit Time-Constant test to determine (a) the dominant pole of the circuit (lowest, high-frequency pole) and (b) the second dominant pole. In doing part (b), state which capacitor determines the second dominant pole (intuitively), then derive it. Also assume $R_1 = R_2 = 1M\_$, $C_3 = C_2 = 10pF$, $C_1 = 0.1pF$, and $g_{m1} = g_{m2} = 10\mu S$. Do NOT use any other means to determine the answer and show your work.
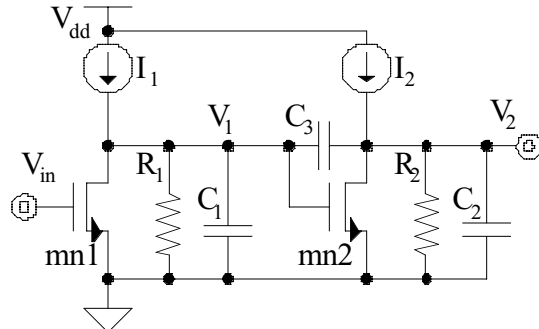
Problem 6 - (20 points - This problem is optional)

Assuming transconductance parameter K', small-signal output resistance r_{ds}, and threshold voltage V_T of all transistors are $100\mu A/V^2$, ∞, and 0.6V, respectively, answer the following questions (ignore bulk effects):

(a) Identify the transistors in the ac-signal path of the positive feedback loop.

(b) What type of sampling is being employed at V_{out1} and V_{out2}?

(c) Based on the answers of (a) and (b), is the feedback circuit increasing or decreasing the effective output resistance at V_{out1} and V_{out2}?

(d) Determine the rising threshold voltage (V_{th+}) of the circuit.

(e) Determine the falling threshold voltage (V_{th-}) of the circuit.

Problem 7 – (20 points – This problem is optional)

On Thursday evening, April 22, 2004, Professor Richard Jaeger gave a presentation to the IEEE Solid-State Circuits/Circuits and Systems Joint Chapter on the Georgia Tech campus. Describe the primary thing that you learned from this lecture.

Extra Page