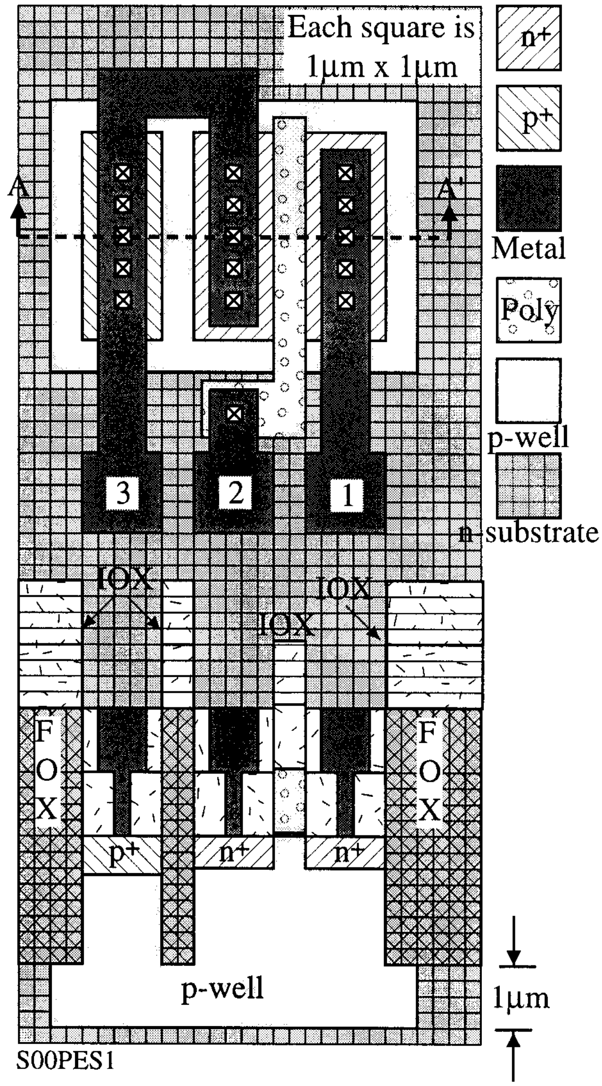
Homework No. 1 - Solutions

Problem 1 - (10 points)

A top view of a MOS transistor is shown. (a) Identify the type of transistor (NMOS or PMOS) and its value of W and L.

(b.) Draw the cross-section A-A' approxi- mately to scale.

(c) Assume that dc voltage of terminal 1 is 5V, terminal 2 is 3V and terminal 3 is 0V. Find the numerical value of the capacitance between terminals 1 and 2, 2 and 3, and 1 and 3. Assume that the dc value of the output voltage is 2.5V and that the voltage dependence for pn junction capacitances is for both transistors is -0.5 (this is called MJ in SPICE).



S00PES1

Solution

(a.) This transistor is an NMOS transistor with the drain as terminal 1, the gate as terminal 2, and the bulk and source connected together to terminal 3. The $W = 13\mu m$ and $L = 2\mu m$.

(b.) The approximate cross-section is shown (vertical scale is magnified by 4 times).

(c.)With $V_{DS} = 5V$, $V_{GS} = 3V$ and $V_T = 0.75V$, the transistor is in saturation. Therefore, the capacitors are:

$$C_{12} = C_{GD} = \text{LD(NMOS)x}W\text{x}C_{ox}$$

$$= 0.45\mu m \cdot 13\mu m \cdot 0.7fF/\mu m2 = \underline{\underline{4.095fF}}$$

$$C_{23} = C_{GS} = \text{LD(NMOS)x}W\text{x}C_{ox} + 0.67(W\text{x}L)\text{X } C_{ox} = 4.095fF + 12.133fF$$

$$= \underline{\underline{16.228fF}}$$

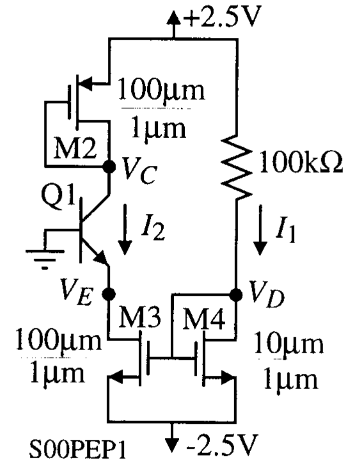
C_{13} requires the area of the drain (AD) and the perimeter of the drain (PD). These values are AD = 13μmx5μm = 65μm^2 and PD = 2(5+13) = 36μm.

$$C_{13} = CBD = \frac{[AD \cdot 0.33fF/m^2 + PD \cdot 0.9fF/\mu m]}{\sqrt{1+\frac{5}{0.6}}} = \frac{[65\mu m^2 \cdot 0.33fF/m^2 + 36\mu m \cdot 0.9fF/\mu m]}{\sqrt{1+\frac{5}{0.6}}}$$

$$= \underline{\underline{17.63fF}}$$

Problem 2 - (10 points)

Find the numerical values of I_1, I_2, V_D, V_E, and V_C to within ±5% accuracy.



Solution

First find I_1. This is done by solving the equations $I_1 = \frac{K'W}{2L}(V_{GS4}-V_T)^2$

and $5\text{V} = I_1 100\text{k}\Omega + V_{GS4}$

Solving quadratically gives

$$V_{GS4}^2 - V_{GS4}\left(2V_T - \frac{1}{12}\right) + \left(V_T^2 - \frac{5}{12}\right) = 0$$

$$V_{GS}^2 - 1.41667V_{GS} + 0.145833 = 0$$

This gives $V_{GS} = 0.708335 \pm 0.5965 = 1.305\text{V}$ $\quad\therefore\ V_D = -2.5+1.305 = \underline{\underline{-1.195\text{V}}}$

This value of V_{GS} gives $I_1 = \frac{5-1.195}{100\text{k}\Omega} = \underline{\underline{36.95\mu\text{A}}}$

Neglecting the lambda effects, let $I_2 = 10I_1 = \underline{\underline{369.5\mu\text{A}}}$

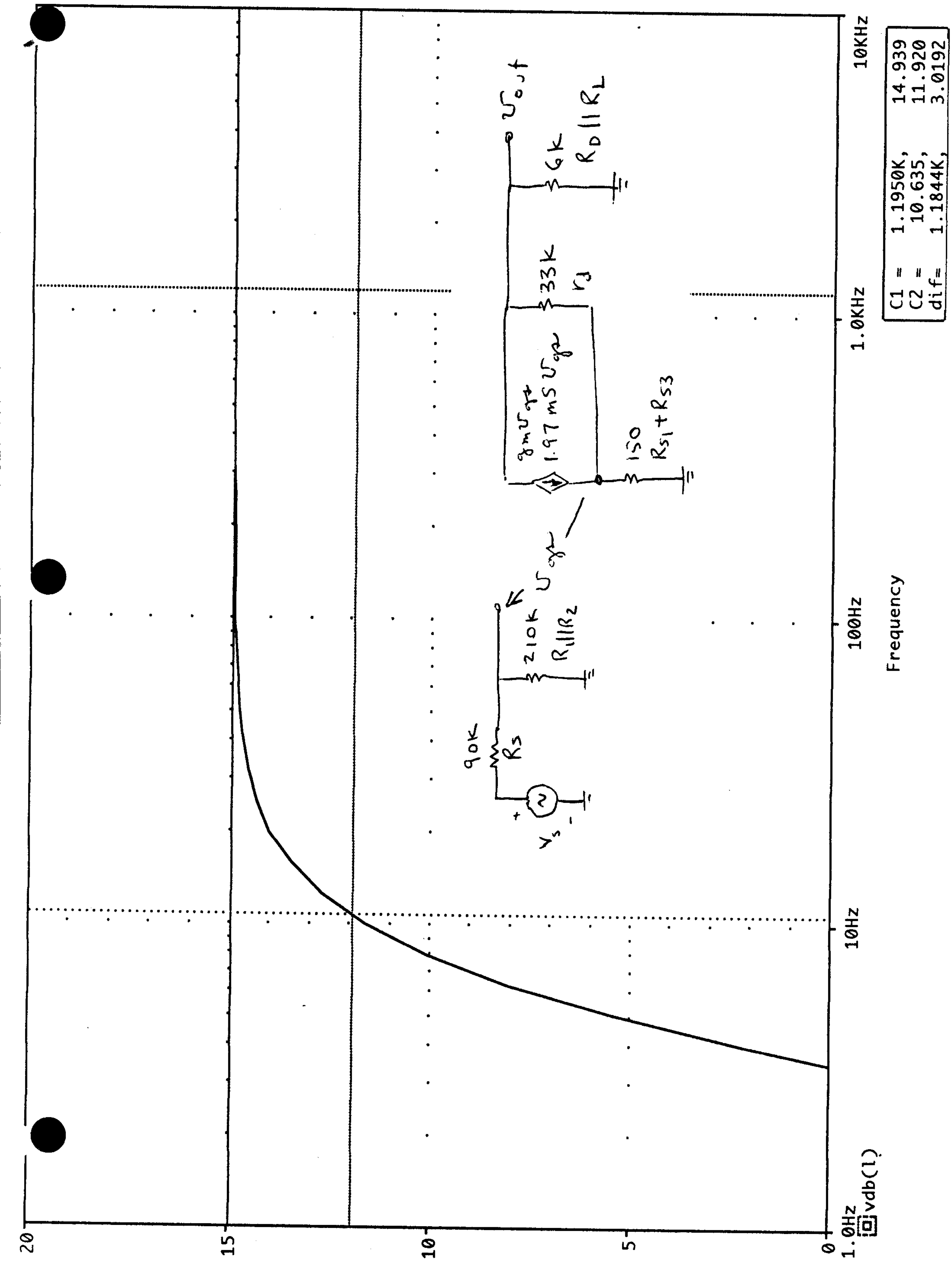
The base-emitter voltage of Q1 is found as

$$V_E = -V_{BE1} = -V_T\ln\left(\frac{I_2}{I_s}\right) = -0.026\ln\left(\frac{369.5\mu\text{A}}{10\text{fA}}\right) = \underline{\underline{-0.633\text{V}}}$$

Finally, the value of $V_{GS2} = \sqrt{\frac{2I_2}{K'W_2/L_2}} + V_T = \sqrt{\frac{2\cdot 369.5}{800}} + 0.75 = 1.711\text{V}$

$\therefore\ V_C = 2.5\text{V} - 1.711\text{V} = \underline{\underline{+0.7889\text{V}}}$

Problem 3



C1 = 1.1950K, 14.939
C2 = 10.635, 11.920
dif= 1.1844K, 3.0192
Frequency
vdb(1)
1.0Hz
10Hz
100Hz
1.0KHz
10KHz
0
5
10
15
20
v_s
90K
R_s
210K
$R_1 \| R_2$
v_{gs}
$g_m v_{gs}$
1.97 mS v_{gs}
150
$R_{S1} + R_{S3}$
33K
r_d
6K
$R_D \| R_L$
v_{out}

Problem 4

$I_C := .5\cdot 10^{-3}$ $\beta := 150$ $R_C := 10\cdot 10^3$ $R_E := 100\cdot 10^3$ $V_T := .026$

$r_\pi := \frac{\beta}{I_C}\cdot V_T$

$R_B := 3\cdot 10^3$ $C := 100\cdot 10^{-12}$

$r_\pi = 7.8\cdot 10^3$

$A_2 := \frac{-\beta\cdot R_C}{r_\pi + (\beta + 1)\cdot 2\cdot R_E}$

$A_1 := \frac{-\beta\cdot R_C}{r_\pi}$

$A_2 = -0.05$

$A_1 = -192.308$

$A_{DM} := A_1\cdot\frac{r_\pi}{r_\pi + R_B}$

$A_{CM} := A_2\cdot\frac{r_\pi + (\beta + 1)\cdot 2\cdot R_E}{r_\pi + (\beta + 1)\cdot 2\cdot R_E + R_B}$

$A_{CM} = -0.05$

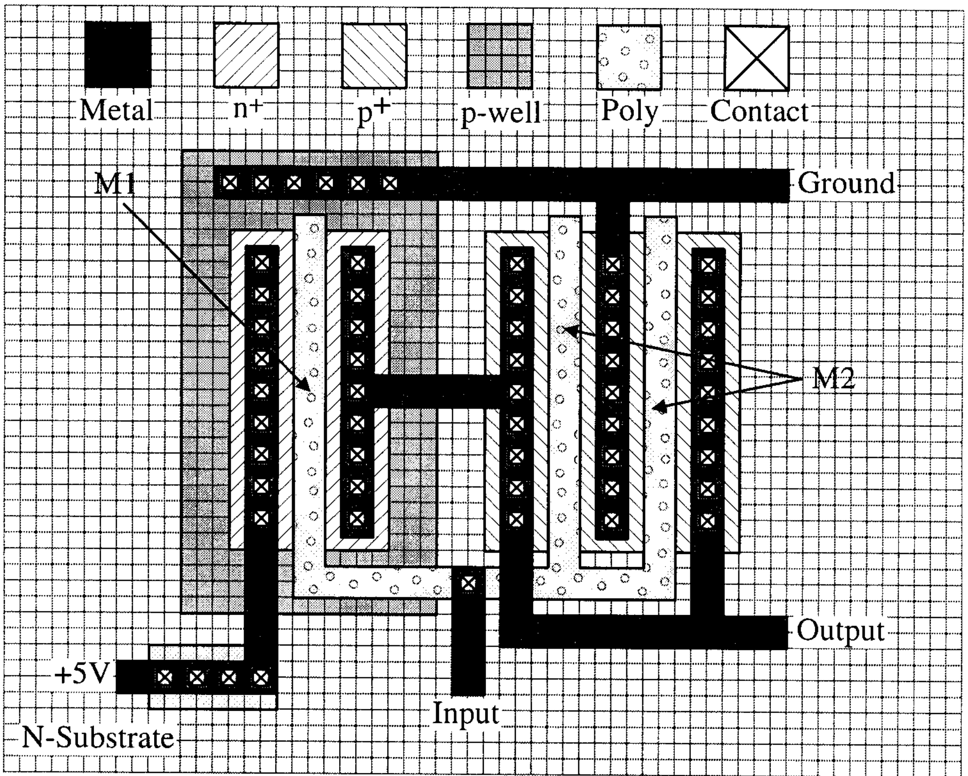
$A_{DM} = -138.889$

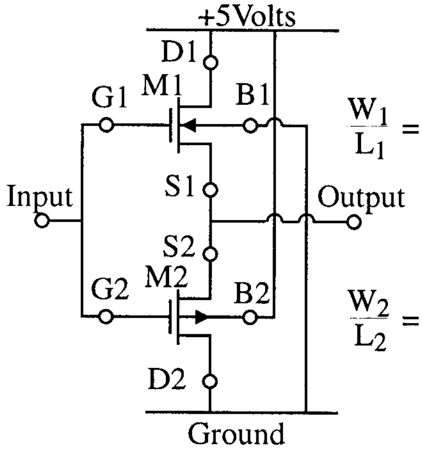
$f_{3dB} := \frac{1}{2\cdot\pi\cdot 2\cdot R_C\cdot C}$

$f_{3dB} = 7.958\cdot 10^4$

Problem 5

Draw the electrical schematic using the proper symbols for the transistors. Identify on your schematic the terminals which are +5V, ground, input, and output. Label the transistors on the layout as M1, M2, etc. and determine their W/L values. Assume each square in the layout is 1 micron by 1 micron. Find the area in square microns and periphery in microns for the source and drain of each transistor.





$\frac{W_1}{L_1} = 10$

$A_{S1} = A_{D1} = 20x4 = 80\mu m^2$

$P_{S1} = P_{D1} = 4+4+20+20 = 48\mu m^2$

$\frac{W_2}{L_2} = 20$

$A_{S2} = 2A_{S1} = 160\mu m^2$

$A_{D2} = A_{D1} = 80\mu m^2$

$P_{S2} = 2P_{S1} = 96\mu m^2$

$P_{D2} = P_{D1} = 48\mu m^2$

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