Problem 6.4-04

In Fig. P6.4-4, find v_{out}/v_{ground} and identify the low-frequency gain and the roots. This represents the case where a noisy ac ground can influence the noise performance of the two-stage op amp.

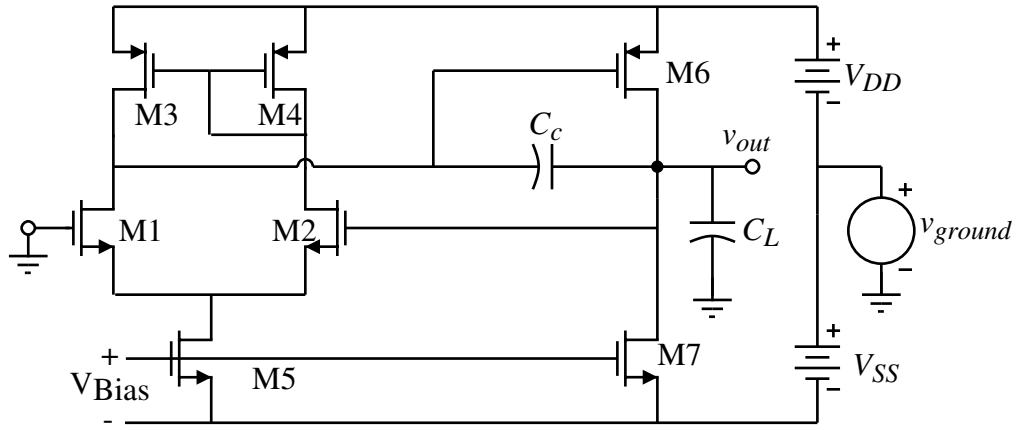


Figure P6.4-4

Solution

Let, $v_{dd} = -v_{ss} = \dfrac{v_{ground}}{2}$ and, v_5 be the small-signal ac voltage at the drain of M_5.

Applying nodal analysis

$$\left(g_{m2}\left(v_{out} - v_5\right) + g_{m5}v_{ss} + g_{ds2}\left(v_{dd} - v_5\right) - g_{m1}v_5 + g_{ds1}\left(v_1 - v_5\right)\right)r_{ds5} = v_5$$

or, $$v_5 = \frac{\left(g_{m2}v_{out} + g_{ds2}v_{dd} + g_{m5}v_{ss}\right)}{\left(g_{m1} + g_{m2}\right)} \qquad (1)$$

Now,

$$\left(g_{m2}\left(v_{out} - v_5\right) + g_{ds2}\left(v_{dd} - v_5\right) + g_{m1}v_5 + g_{ds3}\left(v_{dd} - v_1\right)\right) = \left(g_{ds1}\left(v_1 - v_5\right) + sC_C\left(v_1 - v_{out}\right)\right)$$

or, $$\left(g_{m2} + sC_C\right)v_{out} + \left(g_{ds2} + g_{ds3}\right)v_{dd} = \left(g_{ds1} + g_{ds3} + sC_C\right)v_1 \qquad (2)$$

Also,

$$\left(sC_C\left(v_1 - v_{out}\right) + g_{m7}v_{ss}\right) = \left(g_{ds6}\left(v_{out} - v_{dd}\right) + g_{ds7}\left(v_{out} - v_{ss}\right) + sC_Lv_{out} + g_{m6}\left(v_1 - v_{dd}\right)\right)$$

Using $v_{dd} = -v_{ss}$, we get

$$\left(g_{m6} - g_{m7} + g_{ds6} - g_{ds7}\right)v_{dd} = \left(g_{ds6} + g_{ds7} + s\left(C_C + C_L\right)\right)v_{out} + \left(g_{m6} - sC_C\right)v_1 \qquad (3)$$

Using Equations (2) and (3) gives the low frequency PSRR as

$$\frac{v_{out}}{v_{ground}} = \left\lceil \frac{2g_{mI}g_{mII}}{G_I\left(g_{ds6} - g_{ds7} - g_{m7}\right)} \right\rceil^{-1}$$

The zero is

$$z_1 \cong -\frac{G_I\left(g_{ds6} - g_{ds7} - g_{m7}\right)}{C_C\left(G_I + g_{m6} - g_{m7} + g_{ds6} - g_{ds7}\right)}$$

The two poles are same as given by the zeros of Equation (6.4-14) in the text.

Problem 6.5-01

Assume that in Fig. 6.5-1(a) that the currents in M1 and M2 are 50μA and the W/L values of the NMOS transistors are 10 and of the PMOS transistors are 5. What is the value of V_{Bias} that will cause the drain-source voltage of M1 and M2 to be equal to V_{ds}(sat)? Design the value of *R*. to keep the source-drain voltage of M3 and M4 equal to V_{sd}(sat). Find an expression for the small-signal voltage gain of v_{o1}/v_{in} for Fig. 6.5-1(a).

Solution

$$V_{BIAS} = V_{T,MC1} + V_{dsat,MC1} + V_{dsat,M1}$$

or, $$V_{BIAS} = V_{T,MC1} + \sqrt{\frac{2I_1}{K_N'\left(\frac{W}{L}\right)_{C1}}} + \sqrt{\frac{2I_1}{K_N'\left(\frac{W}{L}\right)_{1}}}$$

Ignoring bulk effects

$$V_{BIAS} = \underline{\underline{1.3\text{V}}}$$

Now,

$$V_{G,C3} = V_{T,C3} + V_{dsat,C3} + V_{dsat3}$$

$$V_{G3} = V_{T3} + V_{dsat3}$$

And, $$IR = V_{G,C3} - V_{G3} = V_{dsat,C3}$$

or, $$R = \sqrt{\frac{2}{IK_P'\left(\frac{W}{L}\right)_{C3}}} = \underline{\underline{12.65\text{k}\Omega}}$$

The output impedance is given by

$$R_{out} = \left[g_{m,C4} r_{ds,C4} r_{ds4}\right] \| \left[g_{m,C2} r_{ds,C2} r_{ds2}\right]$$

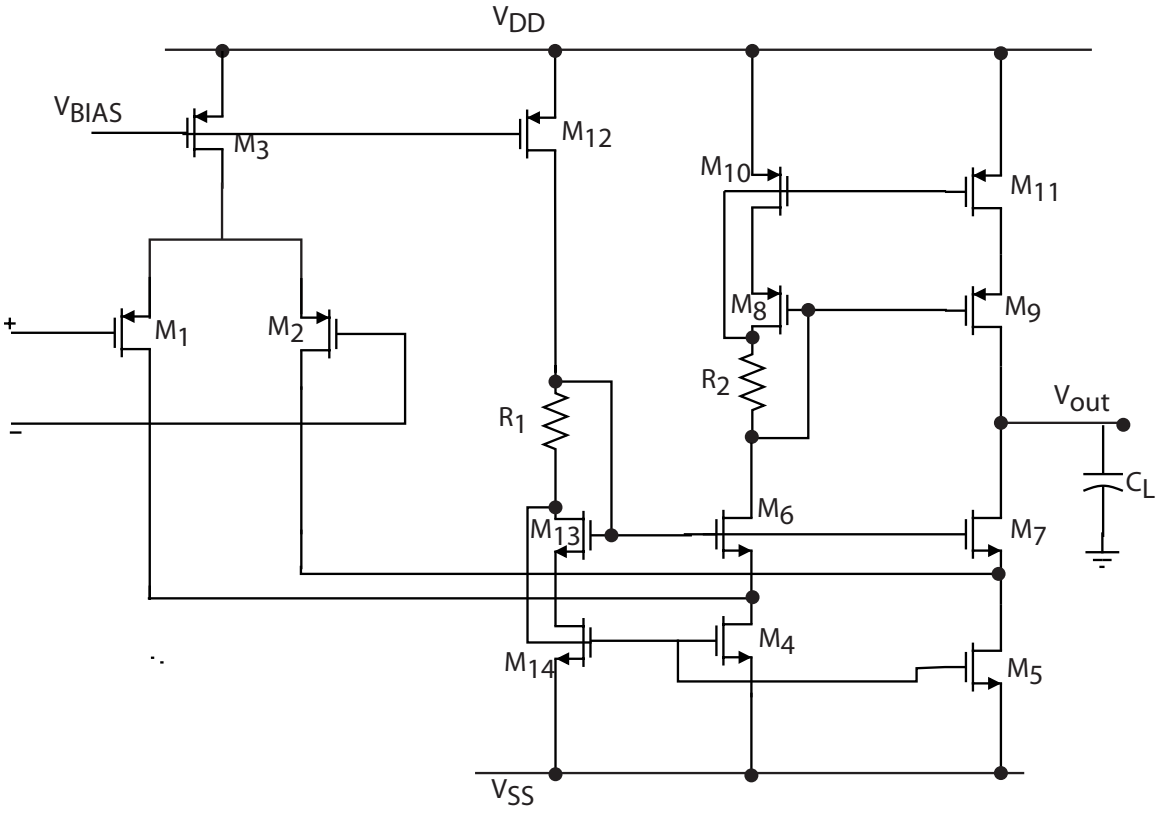
$$R_{out} = 19.38 \quad M\Omega$$

The small-signal voltage gain is given by

$$A_v = -g_{m,C2} R_{out} = \underline{\underline{-6248\ \text{V/V}}}$$

Problem 6.5-14

Repeat Example 6.5-3 if the differential input pair are PMOS transistors (i.e. all NMOS transistors become PMOS and all PMOS transistors become NMOS and the power supplies are reversed).



Solution

$I_3 = 100\ \mu A$ and, $I_4 = I_5 = 125\ \mu A$

Given, $V_{out}(\max) = 2$ V $\rightarrow$ $V_{dsat9} = V_{dsat11} = 0.25$ V

Considering worst-case peak sourcing current of 125 μA

$$\boxed{S_8 = S_9 = S_{10} = S_{11} = 80}$$

Given, $V_{out}(\min) = -2$ V $\rightarrow$ $V_{dsat7} = V_{dsat5} = 0.25$ V

Considering worst-case peak sinking current of 125 μA

$I_5 = 125\ \mu A$ and $I_7 = 25\ \mu A$

$$\boxed{S_6 = S_7 = S_{13} = 7.3}$$

And, $$\boxed{S_4 = S_5 = S_{14} = 36.4}$$

$$R_1 = \frac{V_{dsat7}}{I_{14}} = 2\ K\Omega \qquad \text{and} \qquad R_2 = \frac{V_{dsat9}}{I_{10}} = 2\ K\Omega$$

From gain-bandwidth

$$\boxed{S_1 = S_2 = \frac{(GB)^2 C_L^2}{K_P' I_3} = 79}$$

Problem 6.5-14 - Continued

Considering $V_{in}(\max) = 1$ V

$$V_{dsat3} = 0.43 \text{ V} \qquad \rightarrow \qquad \boxed{S_3 = 21.6}$$

The minimum input common-mode voltage is

$$V_{in}(\min) = V_{SS} - |V_{T1}(\min)| + V_{dsat4} = -2.8 \text{ V}$$

Finally, $\boxed{S_{12} = 1.25 S_3 = 27}$

The small-signal gain is

$$A_v = \frac{(2+k)}{(2+2k)} g_{mI} R_{II}$$

$$k = \frac{R_9 (g_{ds2} + g_{ds4})}{(g_{m7} r_{ds7})}$$

where, $R_9 = 55 \text{ M}\Omega$

$g_{mI} = 628.3 \text{ } \mu S$, $g_{m7} = 347 \text{ } \mu S$, $g_{ds7} = 3 \text{ } \mu S$, $g_{ds4} = 5 \text{ } \mu S$, $g_{ds2} = 2.5 \text{ } \mu S$

So, $k = 3.96$

$R_{II} = 12 \text{ M}\Omega$

or, $A_v = 4364$ V/V

6.15

$200\ \mu A = |I_{D8}| = |I_{D5}| = |I_{D7}| = I_{D6}$

$100\ \mu A = I_{D1} = I_{D2} = I_{D3} = I_{D4}$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9\,(8.85\times10^{-14}\ F/cm)}{80\ \text{Å}}$$

$$= 431\ nF/cm^2$$

$$\mu_n C_{ox} = 450\ \frac{cm^2}{V.s}\ 431\ \frac{nF}{cm^2}$$

$$= 194\ \mu A/V^2$$

$$\mathcal{K}_n' = 194\ \mu A/V^2$$

$$\mathcal{K}_p' = 64.7\ \mu A/V^2$$

$$\frac{v_o}{v_i} = -g_{m_2}(r_{o2} \| r_{o4})\, g_{m_6}(r_{o6} \| r_{o7})$$

$$\frac{1}{r_{o2}} = \frac{I_{D_2}}{L_{eff}}\frac{dX_d}{dV_{DS}} = \frac{100\ \mu A}{0.72\ \mu m}(0.04\ \mu) = 5.56\ \mu$$

$r_{o2} = 180\ k\Omega = r_{o4}$

$r_{o6} = 90\ k\Omega = r_{o7}$

$$L_{eff} = L - X_d - 2L_d$$

$$= 1 - 0.1 - 2(0.09)$$

$$= 0.72\ \mu m$$

$$g_{m_2} = \sqrt{2\mathcal{K}_p'\frac{W}{L_{eff}}I_{D_2}}$$

$$= \sqrt{2(64.7\ \mu)\left(\frac{150}{0.72}\right)(100\ \mu)}$$

$$= 1640\ \mu A/V$$

$$g_{m_6} = \sqrt{2(194\ \mu)\left(\frac{100}{0.72}\right)(200\ \mu)}$$

$$= 3280\ \mu A/V$$

$$\frac{v_o}{v_i} = -(1.64\ m)(90\ k)(3.28\ m)(45\ k)$$

$$= -2.18\times10^4$$

common mode range:

From (6.75),

$$V_{IC} > V_{t_1} + V_{t_3} + V_{OV_3} - V_{SS}$$

$$V_{OV_3} = \sqrt{\frac{2(100)}{194\,(50/0.72)}} = 0.12\ V$$

$$V_{IC} > -0.8 + 0.6 + 0.12 - 1.5$$

$$V_{IC} > -1.58\ V$$

From (6.77),

$$V_{IC} < V_{t_1} + V_{OV_1} + V_{OV_5} + V_{DD}$$

$$V_{OV_5} = -\sqrt{\frac{2(200)}{64.7\,(150/0.72)}} = -0.17\ V$$

$$V_{OV_1} = -\sqrt{\frac{2(100)}{64.7\,(150/0.72)}} = -0.12\ V$$

$$V_{IC} < -0.8 - 0.12 - 0.17 + 1.5$$

$$V_{IC} < 0.41\ V$$

From (6.86),

$$\frac{v_o}{v_{dd}} \cong 0$$

From (6.87),

$$\frac{v_o}{v_{ss}} = \frac{r_{o7}}{r_{o6} + r_{o7}} = 0.5$$

```
TWO-STAGE CMOS AMPLIFIER
******
VDD 100  0  1.5
VSS 200  0  -1.5
M1    7  5    4   4   PMOS W=150U  L=1U
M2    8  6    4   4   PMOS W=150U  L=1U
M3    7  7    200 200 NMOS W=50U   L=1U
M4    8  7    200 200 NMOS W=50U   L=1U
M5    4  3    100 100 PMOS W=150U  L=1U
M6    9  8    200 200 NMOS W=100U  L=1U
M7    9  3    100 100 PMOS W=150U  L=1U
M8    3  3    100 100 PMOS W=150U  L=1U
IBIAS 3  200  200U
* THE DC OFFSET IS ADJUSTED BY TRIAL AND ERROR
* TO SET THE OUTPUT TO ZERO.
VI1   5  2  4.6U
VI2   6  2  0
VIC   2  0  0
*LEFF = LDRAWN - 2LD -XD = 1 - 2(0.09) - 0.1 = 0.72 UM
*LAMBDA=(DXD/DVDS)/LEFF = 0.04U/0.72U = 0.0555
.MODEL NMOS NMOS LEVEL=1 KP=194U  VTO=0.6  LAMBDA=0.0555
.MODEL PMOS PMOS LEVEL=1 KP=64.7U VTO=-0.8 LAMBDA=0.0555
.OPTIONS NOPAGE NOMOD
.WIDTH OUT=80
.OPTIONS VNTOL=1N ABSTOL=1F RELTOL=1U
.OP
.TF   V(9) VI1
.END

 ****  OPERATING POINT INFORMATION     TNOM=  27.000 TEMP=  27.000
   NODE    =VOLTAGE      NODE    =VOLTAGE      NODE    =VOLTAGE
+0:2       =   0.      0:3       = 5.024E-01 0:4       = 9.357E-01
+0:5       = 4.600E-06 0:6       =   0.      0:7       =-7.609E-01
+0:8       =-7.602E-01 0:9       = 3.026E-04 0:100     = 1.500E+00
+0:200     =-1.500E+00

SUBCKT
ELEMENT  0:M1       0:M2       0:M3       0:M4
MODEL    0:PMOS     0:PMOS     0:NMOS     0:NMOS
 ID      -9.772E-05 -9.772E-05  9.772E-05  9.772E-05
 IBS       0.         0.         0.
 IBD      1.697E-14  1.696E-14 -7.391E-15 -7.398E-15
 VGS     -9.357E-01 -9.357E-01  7.391E-01  7.391E-01
 VDS     -1.696E+00 -1.695E+00  7.391E-01  7.398E-01
 VBS       0.         0.         0.         0.
 VTH     -8.000E-01 -8.000E-01  6.000E-01  6.000E-01
 VDSAT   -1.357E-01 -1.357E-01  1.391E-01  1.391E-01
 BETA     1.062E-02  1.062E-02  1.010E-02  1.010E-02
 GAM EFF   0.         0.         0.         0.
 GM       1.441E-03  1.441E-03  1.405E-03  1.405E-03
 GDS      4.957E-06  4.957E-06  5.210E-06  5.210E-06
 GMB       0.         0.         0.         0.

SUBCKT
ELEMENT  0:M5       0:M6       0:M7       0:M8
MODEL    0:PMOS     0:NMOS     0:PMOS     0:PMOS
 ID      -1.954E-04  2.053E-04 -2.053E-04 -2.000E-04
 IBS       0.         0.         0.         0.
 IBD      5.643E-15 -1.500E-14  1.500E-14  9.976E-15
 VGS     -9.976E-01  7.398E-01 -9.976E-01 -9.976E-01
 VDS     -5.643E-01  1.500E+00 -1.499E+00 -9.976E-01
 VBS       0.         0.         0.         0.
 VTH     -8.000E-01  6.000E-01 -8.000E-01 -8.000E-01
 VDSAT   -1.976E-01  1.398E-01 -1.976E-01 -1.976E-01
 BETA     1.001E-02  2.102E-02  1.051E-02  1.024E-02
 GAM EFF   0.         0.         0.         0.
 GM       1.978E-03  2.937E-03  2.078E-03  2.024E-03
 GDS      1.052E-05  1.052E-05  1.052E-05  1.052E-05
 GMB       0.         0.         0.         0.

****     SMALL-SIGNAL TRANSFER CHARACTERISTICS

V(9)/VI1                                = -1.975E+04
INPUT RESISTANCE AT         VI1         =  1.000E+20
OUTPUT RESISTANCE AT V(9)               =  4.754E+04
```

```
TWO-STAGE CMOS AMPLIFIER (MAXIMUM COMMON-MODE INPUT VOLTAGE)
******
VDD 100  0  1.5
VSS 200  0  -1.5
M1    7  5    4   4   PMOS W=150U  L=1U
M2    8  6    4   4   PMOS W=150U  L=1U
M3    7  7    200 200 NMOS W=50U   L=1U
M4    8  7    200 200 NMOS W=50U   L=1U
M5    4  3    100 100 PMOS W=150U  L=1U
M6    9  8    200 200 NMOS W=100U  L=1U
M7    9  3    100 100 PMOS W=150U  L=1U
M8    3  3    100 100 PMOS W=150U  L=1U
IBIAS 3  200  200U
* THE DC OFFSET IS ADJUSTED BY TRIAL AND ERROR
* TO SET THE OUTPUT TO ZERO.
VI1   5  2  13.7U
VI2   6  2  0
* THE MAXIMUM VALUE OF VIC IS ADJUSTED BY TRIAL AND ERROR
* UNTIL M5 BARELY OPERATES IN THE ACTIVE REGION
* (WHERE |VDS| > |VDSAT| FOR M5)
VIC   2  0  0.36
*LEFF = LDRAWN - 2LD -XD = 1 - 2(0.09) - 0.1 = 0.72 UM
*LAMBDA=(DXD/DVDS)/LEFF = 0.04U/0.72U = 0.0555
.MODEL NMOS NMOS LEVEL=1 KP=194U  VTO=0.6  LAMBDA=0.0555
.MODEL PMOS PMOS LEVEL=1 KP=64.7U VTO=-0.8 LAMBDA=0.0555
.OPTIONS NOPAGE NOMOD
.WIDTH OUT=80
.OPTIONS VNTOL=1N ABSTOL=1F RELTOL=1U
.OP
.TF   V(9) VI1
.END

 ****  OPERATING POINT INFORMATION     TNOM=  27.000 TEMP=  27.000
   NODE    =VOLTAGE      NODE    =VOLTAGE      NODE    =VOLTAGE
+0:2       = 3.600E-01 0:3       = 5.024E-01 0:4       = 1.293E+00
+0:5       = 3.600E-01 0:6       = 3.600E-01 0:7       =-7.622E-01
+0:8       =-7.602E-01 0:9       = 1.329E-04 0:100     = 1.500E+00
+0:200     =-1.500E+00

**** MOSFETS
SUBCKT
ELEMENT  0:M1       0:M2       0:M3       0:M4
MODEL    0:PMOS     0:PMOS     0:NMOS     0:NMOS
 ID      -9.584E-05 -9.585E-05  9.584E-05  9.585E-05
 IBS       0.         0.         0.         0.
 IBD      2.055E-14  2.053E-14 -7.378E-15 -7.398E-15
 VGS     -9.331E-01 -9.332E-01  7.378E-01  7.378E-01
 VDS     -2.055E+00 -2.053E+00  7.378E-01  7.398E-01
 VBS       0.         0.         0.         0.
 VTH     -8.000E-01 -8.000E-01  6.000E-01  6.000E-01
 VDSAT   -1.331E-01 -1.332E-01  1.378E-01  1.378E-01
 BETA     1.081E-02  1.081E-02  1.010E-02  1.010E-02
 GAM EFF   0.         0.         0.         0.
 GM       1.440E-03  1.440E-03  1.391E-03  1.391E-03
 GDS      4.774E-06  4.775E-06  5.110E-06  5.110E-06
 GMB       0.         0.         0.         0.

SUBCKT
ELEMENT  0:M5       0:M6       0:M7       0:M8
MODEL    0:PMOS     0:NMOS     0:PMOS     0:PMOS
 ID      -1.917E-04  2.053E-04 -2.053E-04 -2.000E-04
 IBS       0.         0.         0.         0.
 IBD      2.068E-15 -1.500E-14  1.500E-14  9.976E-15
 VGS     -9.976E-01  7.398E-01 -9.976E-01 -9.976E-01
 VDS     -2.068E-01  1.500E+00 -1.499E+00 -9.976E-01
 VBS       0.         0.         0.         0.
 VTH     -8.000E-01  6.000E-01 -8.000E-01 -8.000E-01
 VDSAT   -1.976E-01  1.398E-01 -1.976E-01 -1.976E-01
 BETA     9.816E-03  2.102E-02  1.051E-02  1.024E-02
 GAM EFF   0.         0.         0.         0.
 GM       1.940E-03  2.937E-03  2.078E-03  2.024E-03
 GDS      1.052E-05  1.052E-05  1.052E-05  1.052E-05
 GMB       0.         0.         0.         0.

****     SMALL-SIGNAL TRANSFER CHARACTERISTICS

V(9)/VI1                                = -2.029E+04
INPUT RESISTANCE AT         VI1         =  1.000E+20
OUTPUT RESISTANCE AT V(9)               =  4.753E+04
```

```
TWO-STAGE CMOS AMPLIFIER (MINIMUM COMMON-MODE INPUT VOLTAGE)
******
VDD 100  0  1.5
VSS 200  0  -1.5
M1    7  5    4   4   PMOS W=150U  L=1U
M2    8  6    4   4   PMOS W=150U  L=1U
M3    7  7    200 200 NMOS W=50U   L=1U
M4    8  7    200 200 NMOS W=50U   L=1U
M5    4  3    100 100 PMOS W=150U  L=1U
M6    9  8    200 200 NMOS W=100U  L=1U
M7    9  3    100 100 PMOS W=150U  L=1U
M8    3  3    100 100 PMOS W=150U  L=1U
IBIAS 3  200  200U
* THE DC OFFSET IS ADJUSTED BY TRIAL AND ERROR
* TO SET THE OUTPUT TO ZERO.
VI1   5  2  -39.7U
VI2   6  2  0
* THE MINIMUM VALUE OF VIC IS ADJUSTED BY TRIAL AND ERROR
* UNTIL M1 BARELY OPERATES IN THE ACTIVE REGION
* (WHERE |VDS| > |VDSAT| FOR M1)
VIC   2  0  -1.55
*LEFF = LDRAWN - 2LD -XD = 1 - 2(0.09) - 0.1 = 0.72 UM
*LAMBDA=(DXD/DVDS)/LEFF = 0.04U/0.72U = 0.0555
.MODEL NMOS NMOS LEVEL=1 KP=194U  VTO=0.6  LAMBDA=0.0555
.MODEL PMOS PMOS LEVEL=1 KP=64.7U VTO=-0.8 LAMBDA=0.0555
.OPTIONS NOPAGE NOMOD
.WIDTH OUT=80
.OPTIONS VNTOL=1N ABSTOL=1F RELTOL=1U
.OP
.TF   V(9) VI1
.END

 ****  OPERATING POINT INFORMATION     TNOM=  27.000 TEMP=  27.000
   NODE    =VOLTAGE      NODE    =VOLTAGE      NODE    =VOLTAGE
+0:2       =-1.550E+00 0:3       = 5.024E-01 0:4       =-6.030E-01
+0:5       =-1.550E+00 0:6       =-1.550E+00 0:7       =-7.552E-01
+0:8       =-7.602E-01 0:9       = 6.068E-04 0:100     = 1.500E+00
+0:200     =-1.500E+00

**** MOSFETS
SUBCKT
ELEMENT  0:M1       0:M2       0:M3       0:M4
MODEL    0:PMOS     0:PMOS     0:NMOS     0:NMOS
 ID      -1.058E-04 -1.058E-04  1.058E-04  1.058E-04
 IBS        0.         0.         0.         0.
 IBD      1.523E-15  1.572E-15 -7.448E-15 -7.398E-15
 VGS     -9.471E-01 -9.470E-01  7.448E-01  7.448E-01
 VDS     -1.523E-01 -1.572E-01  7.448E-01  7.398E-01
 VBS        0.         0.         0.         0.
 VTH     -8.000E-01 -8.000E-01  6.000E-01  6.000E-01
 VDSAT   -1.471E-01 -1.470E-01  1.448E-01  1.448E-01
 BETA     9.787E-03  9.790E-03  1.010E-02  1.010E-02
 GAM EFF    0.         0.         0.         0.
 GM       1.439E-03  1.439E-03  1.462E-03  1.462E-03
 GDS      5.824E-06  5.821E-06  5.640E-06  5.640E-06
 GMB        0.         0.         0.         0.

SUBCKT
ELEMENT  0:M5       0:M6       0:M7       0:M8
MODEL    0:PMOS     0:NMOS     0:PMOS     0:PMOS
 ID      -2.116E-04  2.053E-04 -2.053E-04 -2.000E-04
 IBS        0.         0.         0.         0.
 IBD      2.103E-14 -1.501E-14  1.499E-14  9.976E-15
 VGS     -9.976E-01  7.398E-01 -9.976E-01 -9.976E-01
 VDS     -2.103E+00  1.500E+00 -1.499E+00 -9.976E-01
 VBS        0.         0.         0.         0.
 VTH     -8.000E-01  6.000E-01 -8.000E-01 -8.000E-01
 VDSAT   -1.976E-01  1.398E-01 -1.976E-01 -1.976E-01
 BETA     1.084E-02  2.102E-02  1.051E-02  1.024E-02
 GAM EFF    0.         0.         0.         0.
 GM       2.142E-03  2.937E-03  2.077E-03  2.024E-03
 GDS      1.052E-05  1.052E-05  1.052E-05  1.052E-05
 GMB        0.         0.         0.         0.

****     SMALL-SIGNAL TRANSFER CHARACTERISTICS

V(9)/VI1                              = -1.750E+04
INPUT RESISTANCE AT         VI1       =  1.000E+20
OUTPUT RESISTANCE AT V(9)             =  4.754E+04
```

```
TWO-STAGE CMOS AMPLIFIER (GAIN FROM VDD)
******
VDD 100  0  1.5
VSS 200  0  -1.5
M1    7  5    4   4   PMOS W=150U  L=1U
M2    8  6    4   4   PMOS W=150U  L=1U
M3    7  7    200 200 NMOS W=50U   L=1U
M4    8  7    200 200 NMOS W=50U   L=1U
M5    4  3    100 100 PMOS W=150U  L=1U
M6    9  8    200 200 NMOS W=100U  L=1U
M7    9  3    100 100 PMOS W=150U  L=1U
M8    3  3    100 100 PMOS W=150U  L=1U
IBIAS 3  200  200U
* THE DC OFFSET IS ADJUSTED BY TRIAL AND ERROR
* TO SET THE OUTPUT TO ZERO.
VI1   5  2  4.6U
VI2   6  2  0
VIC   2  0  0
*LEFF = LDRAWN - 2LD -XD = 1 - 2(0.09) - 0.1 = 0.72 UM
*LAMBDA=(DXD/DVDS)/LEFF = 0.04U/0.72U = 0.0555
.MODEL NMOS NMOS LEVEL=1 KP=194U  VTO=0.6  LAMBDA=0.0555
.MODEL PMOS PMOS LEVEL=1 KP=64.7U VTO=-0.8 LAMBDA=0.0555
.OPTIONS NOPAGE NOMOD
.WIDTH OUT=80
.OPTIONS VNTOL=1N ABSTOL=1F RELTOL=1U
.OP
.TF   V(9) VDD
.END
 ****  OPERATING POINT INFORMATION     TNOM=  27.000 TEMP=  27.000
   NODE    =VOLTAGE      NODE    =VOLTAGE      NODE    =VOLTAGE
+0:2       =  0.       0:3       = 5.024E-01 0:4       = 9.357E-01
+0:5       = 4.600E-06 0:6       =  0.       0:7       =-7.609E-01
+0:8       =-7.602E-01 0:9       = 3.026E-04 0:100     = 1.500E+00
+0:200     =-1.500E+00
****     SMALL-SIGNAL TRANSFER CHARACTERISTICS
V(9)/VDD                              = -1.647E-02
INPUT RESISTANCE AT         VDD       =  4.723E+04
OUTPUT RESISTANCE AT V(9)             =  4.754E+04
```

```
TWO-STAGE CMOS AMPLIFIER (GAIN FROM VSS)
******
VDD 100  0  1.5
VSS 200  0  -1.5
M1    7  5    4   4   PMOS W=150U  L=1U
M2    8  6    4   4   PMOS W=150U  L=1U
M3    7  7    200 200 NMOS W=50U   L=1U
M4    8  7    200 200 NMOS W=50U   L=1U
M5    4  3    100 100 PMOS W=150U  L=1U
M6    9  8    200 200 NMOS W=100U  L=1U
M7    9  3    100 100 PMOS W=150U  L=1U
M8    3  3    100 100 PMOS W=150U  L=1U
IBIAS 3  200  200U
* THE DC OFFSET IS ADJUSTED BY TRIAL AND ERROR
* TO SET THE OUTPUT TO ZERO.
VI1   5  2  4.6U
VI2   6  2  0
VIC   2  0  0
*LEFF = LDRAWN - 2LD -XD = 1 - 2(0.09) - 0.1 = 0.72 UM
*LAMBDA=(DXD/DVDS)/LEFF = 0.04U/0.72U = 0.0555
.MODEL NMOS NMOS LEVEL=1 KP=194U  VTO=0.6  LAMBDA=0.0555
.MODEL PMOS PMOS LEVEL=1 KP=64.7U VTO=-0.8 LAMBDA=0.0555
.OPTIONS NOPAGE NOMOD
.WIDTH OUT=80
.OPTIONS VNTOL=1N ABSTOL=1F RELTOL=1U
.OP
.TF   V(9) VSS
.END
 ****  OPERATING POINT INFORMATION     TNOM=  27.000 TEMP=  27.000
   NODE    =VOLTAGE      NODE    =VOLTAGE      NODE    =VOLTAGE
+0:2       =  0.       0:3       = 5.024E-01 0:4       = 9.357E-01
+0:5       = 4.600E-06 0:6       =  0.       0:7       =-7.609E-01
+0:8       =-7.602E-01 0:9       = 3.026E-04 0:100     = 1.500E+00
+0:200     =-1.500E+00
****     SMALL-SIGNAL TRANSFER CHARACTERISTICS
V(9)/VSS                              =  5.063E-01
INPUT RESISTANCE AT         VSS       =  1.865E+05
OUTPUT RESISTANCE AT V(9)             =  4.754E+04
```