

## **LECTURE 030 – ECE 4430 REVIEW III**

### **(READING: GHLM - Chaps. 3 and 4)**

#### **Objective**

The objective of this presentation is:

- 1.) Identify the prerequisite material as taught in ECE 4430
- 2.) Insure that the students of ECE 6412 are adequately prepared

#### **Outline**

- Models for Integrated-Circuit Active Devices
- Bipolar, MOS, and BiCMOS IC Technology
- Single-Transistor and Multiple-Transistor Amplifiers
- Transistor Current Sources and Active Loads

## **SINGLE-TRANSISTOR AND MULTIPLE-TRANSISTOR AMPLIFIERS**

### **Characterization of Amplifiers**

Amplifiers will be characterized by the following properties:

- Large-signal voltage transfer characteristics (.DC)
- Large-signal voltage swing limitations (.DC and .TRAN)
- Small-signal, frequency independent performance (.TF)
- Gain (.TF)
- Input resistance (.TF)
- Output resistance (.TF)
- Small-signal, frequency response (.AC)
- Other properties (.TEMP, .FOUR, etc.)
- Noise (.NOISE)
- Power dissipation (.OP)
- Slew rate (.TRAN)
- Etc.

## Types of Single Transistor Amplifiers

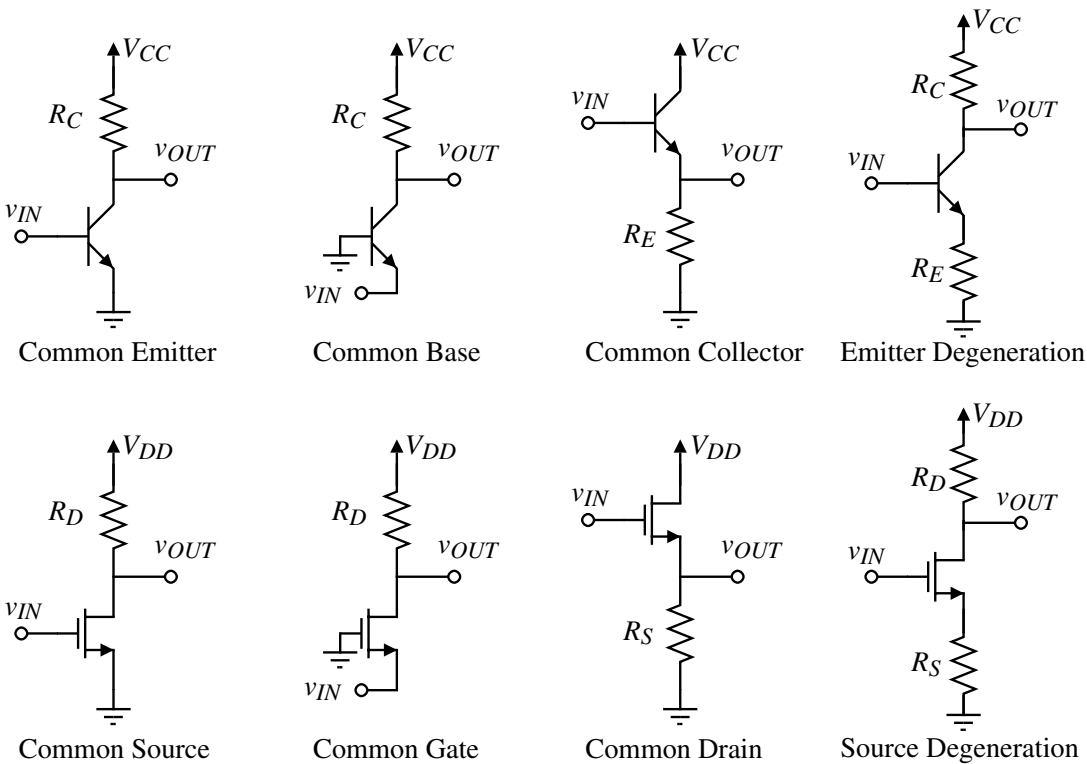


Fig. 030-01

## Signal Flow in Transistors

It is important to recognize that ac signals can only flow into and out of certain transistor terminals.

Illustration:

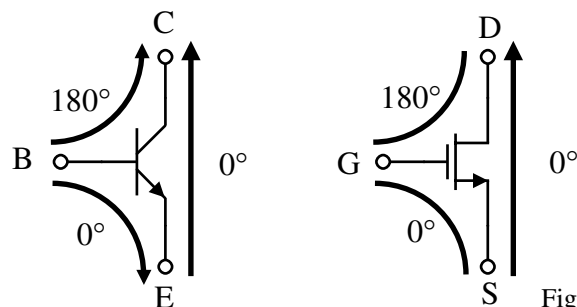


Fig. 030-02

Rules:

The collector or drain can never be an input terminal.

The base or gate can never be an output terminal.

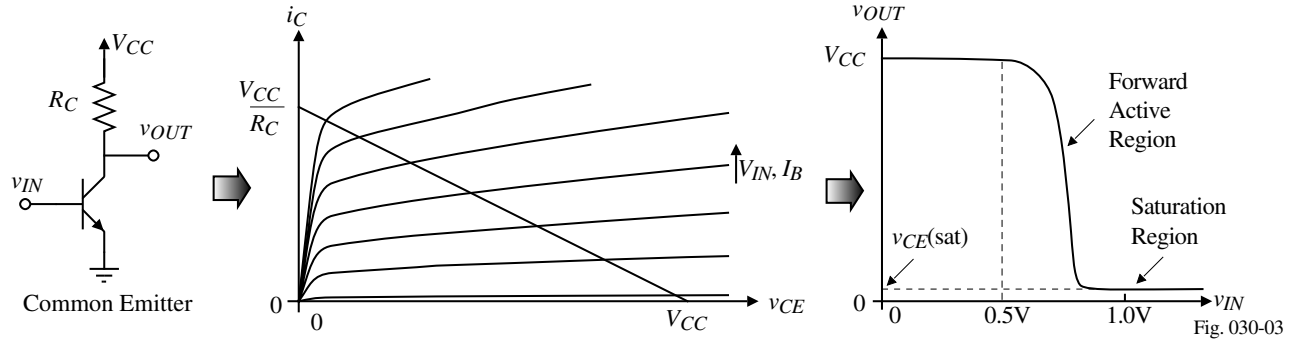
In addition it is important to note polarity reversals on these signal paths.

The base-collector or gate-drain path inverts. All other paths are noninverting.

(This of course assumes that there are no reactive elements causing phase shifts)

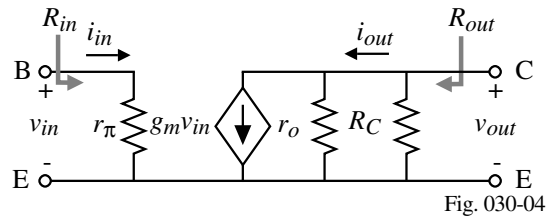
### Common Emitter Amplifier

Large-Signal:



Small-Signal:

$$g_m = \frac{I_C}{V_T} \quad \text{and} \quad r_o = \frac{V_A}{I_C}$$

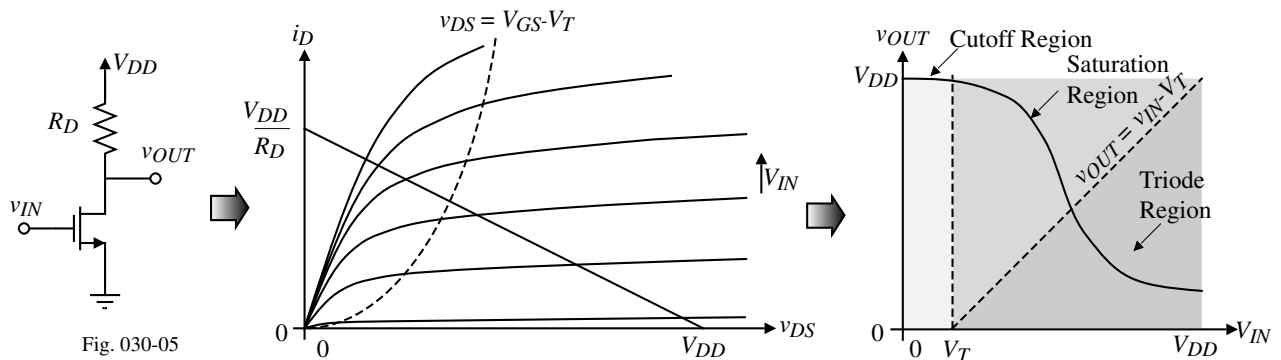


$$R_{in} = r_{\pi} = \frac{\beta_o}{g_m}, \quad R_{out} = \frac{r_o R_C}{r_o + R_C}, \quad \frac{v_{out}}{v_{in}} = \frac{-g_m \cdot r_o \cdot R_C}{r_o + R_C} \quad \text{and} \quad \frac{i_{out}}{i_{in}} = \frac{\beta_o \cdot r_o}{r_o + R_C}$$

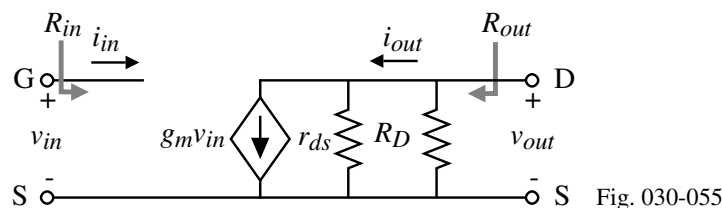
(One should also consider the case of a source resistance,  $R_S$ , in series with the input)

### Common Source Amplifier

Large-Signal:



Small-Signal:



$$R_{in} = \infty, \quad R_{out} = \frac{r_{ds} R_D}{r_{ds} + R_D}, \quad \frac{v_{out}}{v_{in}} = \frac{-g_m \cdot r_{ds} \cdot R_D}{r_{ds} + R_D} \quad \text{and} \quad \frac{i_{out}}{i_{in}} = \infty$$

## Summary of Single BJT Transistor Amplifiers

| Small-Signal Performance | Common Emitter        | Common Base                       | Common Collector                           |
|--------------------------|-----------------------|-----------------------------------|--|
| Input Resistance         | $r_{\pi}$<br>(Medium) | $\frac{r_{\pi}}{1+\beta_o}$ (Low) | $r_{\pi}+(1+\beta_o)R_E$<br>(High)         |
| Output Resistance        | $r_o$<br>(High)       | $r_o(1+\beta_o)$<br>(Very high)   | $\frac{r_{\pi}+R_S}{1+\beta_o}$ (Very low) |
| Voltage Gain             | $-g_m R_L$            | $g_m R_L$                         | 1  |
| Current Gain             | $\beta_o$             | $-\alpha$                         | $-(1+\beta_o)$                             |

## Summary of Single MOSFET Transistor Amplifiers

| Small-Signal Performance | Common Source                        | Common Gate                       | Common Drain            |
|--------------------------|--------------------------------------|-----------------------------------|-------------------------|
| Input Resistance         | $\infty$                             | $\frac{r_{ds}+R_D}{1+g_m r_{ds}}$ | $\infty$                |
| Output Resistance        | $\frac{r_{ds}R_D}{r_{ds}+R_D}$       | $\frac{r_{ds}R_D}{r_{ds}+R_D}$    | $\frac{R_S}{1+g_m R_S}$ |
| Voltage Gain             | $\frac{-g_m r_{ds} R_D}{r_{ds}+R_D}$ | $g_m R_D$                         | 0.8                     |
| Current Gain             | $\infty$                             | -1                                | $\infty$                |

## BJT Cascode Amplifier

Circuit and small-signal model:

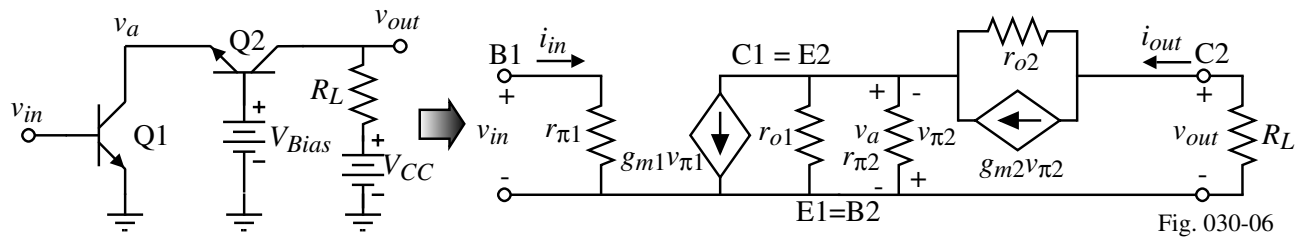


Fig. 030-06

If  $\beta_1 \approx \beta_2$  and  $r_o$  can be neglected, then:

$$R_{in} = r_{\pi 1}$$

$$R_{out} \approx \beta_2 r_{o 2}$$

$$\frac{v_{out}}{v_{in}} = \left( \frac{v_{out}}{v_a} \right) \left( \frac{v_a}{v_{in}} \right) = (g_{m 2} R_L) \left( \frac{r_{\pi 2}}{1 + \beta_{o 2}} \cdot \frac{-\beta_{o 1}}{r_{\pi 1}} \right) \approx (g_{m 2} R_L) (-1) = -g_{m 2} R_L$$

$$\frac{i_{out}}{i_{in}} = \alpha_2 \beta_1$$

The advantage of the cascode is that the gain of Q1 is -1 and therefore the Miller capacitor,  $C_{\mu}$ , is not translated to the base-emitter as a large capacitor.

## MOS Cascode Amplifier

Circuit and small-signal model:

Small-signal performance (assuming a load resistance in the drain of  $R_L$ ):

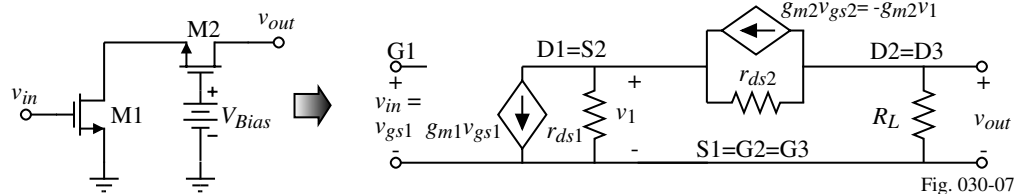


Fig. 030-07

$$R_{in} = \infty$$

Using nodal analysis, we can write,

$$[g_{ds 1} + g_{ds 2} + g_{m 2}]v_1 - g_{ds 2}v_{out} = -g_{m 1}v_{in} \quad \text{and} \quad -[g_{ds 2} + g_{m 2}]v_1 + (g_{ds 2} + G_L)v_{out} = 0$$

Solving for  $v_{out}/v_{in}$  yields,

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m 1}(g_{ds 2} + g_{m 2})}{g_{ds 1}g_{ds 2} + g_{ds 1}G_L + g_{ds 2}G_L + G_Lg_{m 2}} \cong \frac{-g_{m 1}}{G_L} = -g_{m 1}R_L$$

Note that unlike the BJT cascode, the voltage gain,  $v_1/v_{in}$  is greater than -1.

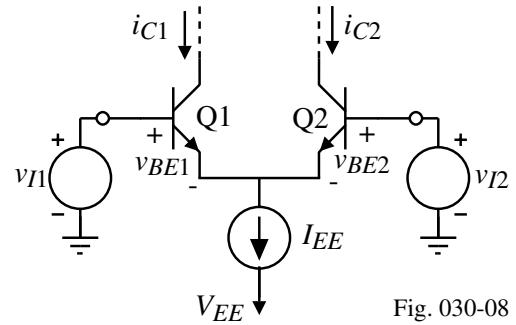
$$\frac{v_1}{v_{in}} = -g_{m 2} \left[ r_{ds 2} \parallel \left( \frac{r_{ds 2} + R_L}{1 + g_{m 2}r_{ds 2}} \right) \right] \approx -\frac{r_{ds 2} + R_L}{r_{ds 2}} = -\left( 1 + \frac{R_L}{r_{ds 2}} \right) \quad (R_L < r_{ds 2} \text{ for the gain to be } -1)$$

The small-signal output resistance is,

$$r_{out} = [r_{ds 1} + r_{ds 2} + g_{m 2}r_{ds 1}r_{ds 2}] \parallel R_L \cong R_L$$

### Transconductance Characteristic of the BJT Differential Amplifier

Consider the following NPN-BJT differential amplifier (sometimes called an emitter-coupled pair):



Large-Signal Analysis:

1.) Input loop eq.:

$$v_{I1} - v_{BE1} + v_{BE2} - v_{I2} = v_{I1} - v_{I2} - v_{BE1} + v_{BE2} = v_{ID} - v_{BE1} + v_{BE2} = 0$$

2.) Forward-active region:

$$v_{BE1} = V_t \ln\left(\frac{i_{C1}}{I_{S1}}\right) \quad \text{and} \quad v_{BE2} = V_t \ln\left(\frac{i_{C2}}{I_{S2}}\right)$$

3.) If  $I_{S1} = I_{S2}$  then  $\frac{i_{C1}}{i_{C2}} = \exp\left(\frac{v_{I1} - v_{I2}}{V_t}\right) = \exp\left(\frac{v_{ID}}{V_t}\right)$

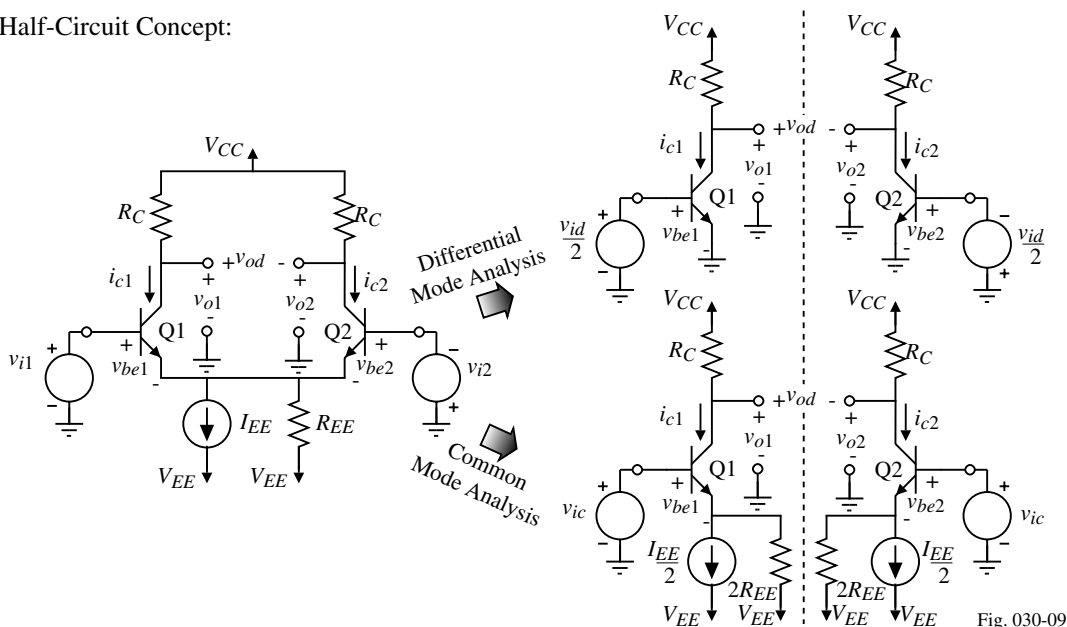
4.) Nodal current equation at the emitters:  $-(i_{E1} + i_{E2}) = I_{EE} = \frac{1}{\alpha_F} (i_{C1} + i_{C2})$

5.) Combining the above equations gives:  $i_{C1} = \frac{\alpha_F I_{EE}}{1 + \exp\left(\frac{-v_{ID}}{V_t}\right)}$  and  $i_{C2} = \frac{\alpha_F I_{EE}}{1 + \exp\left(\frac{v_{ID}}{V_t}\right)}$

### Differential and Common-mode Small-Signal BJT Amplifier Performance

The small-signal performance of a differential amplifier can be separated into a differential mode and common mode analysis. This separation allows us to take advantage of the following simplifications.

Half-Circuit Concept:



Note: The half-circuit concept is valid as long as the resistance seen looking into each emitter is approximately the same.



## Differential and Common-mode Small-Signal Performance

The small-signal performance of a differential amplifier can be separated into a differential mode and common mode analysis. This separation allows us to take advantage of the following simplifications.

Half-Circuit Concept:

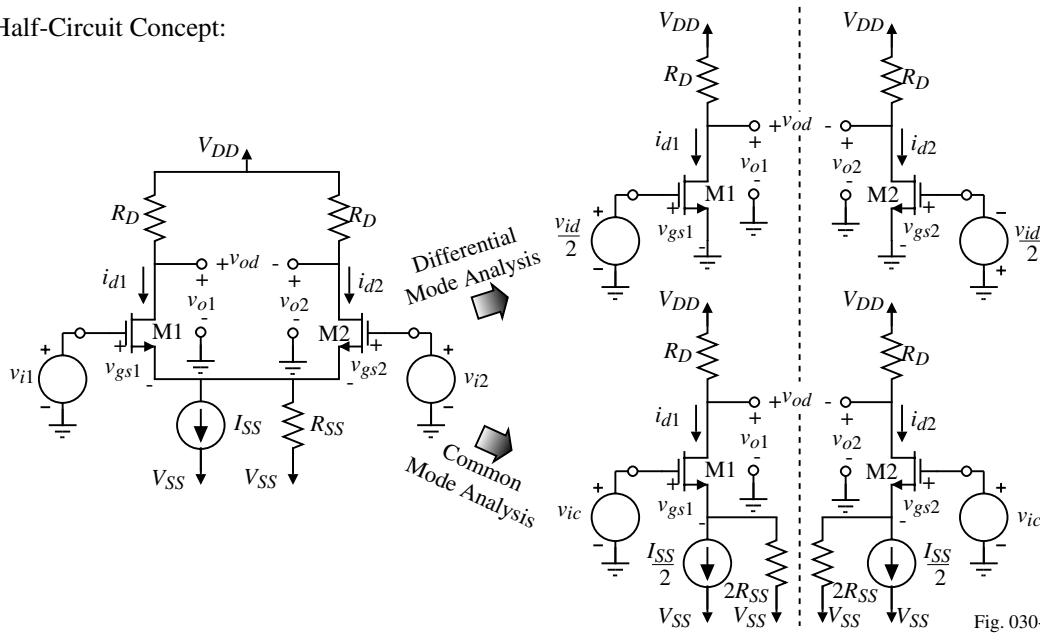


Fig. 030-13

Note: The half-circuit concept is valid as long as the resistance seen looking into each source is approximately the same.

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## Other Characteristics of the Differential Amplifier

- Common-mode rejection ratio
- Input common-mode range
- Slew rate

BJT:

**ICMR:** The maximum and minimum input common mode range is:

$$v_{ic}(\max) = V_{CC} - 0.5I_{EE}R_C - v_{CE1}(\text{sat}) + V_{BE1}$$

$$v_{ic}(\min) = V_{EE} + v_{CE3}(\text{sat}) + V_{BE1}$$

**SR:** The differential amplifier has a slew rate limit of  $I_{EE}/C_{eq}$  where  $C_{eq}$  is the capacitance seen to ground from either collector.

MOSFET:

**ICMR:** The maximum and minimum input common mode range is:

$$v_{ic}(\max) = V_{DD} - 0.5I_{SS}R_D + V_{T1}$$

$$v_{ic}(\min) = V_{SS} + v_{DS3}(\text{sat}) + V_{GS1}$$

**SR:** The differential amplifier has a slew rate limit of  $I_{SS}/C_{eq}$  where  $C_{eq}$  is the equivalent capacitance seen from either of the drains to ground.



## TRANSISTOR CURRENT SOURCES AND ACTIVE LOADS

### Summary of Current Sinks and Sources

| Current Sink/Source                              | $r_{OUT}$  | $V_{MIN}$                  |
|--|--|----------------------------|
| Simple MOS Current Sink                          | $r_{ds} = \frac{1}{\lambda I_D}$                       | $V_{DS(sat)} = V_{ON}$     |
| Simple BJT Current Sink                          | $r_o = \frac{V_A}{I_C}$                                | $V_{CE(sat)} \approx 0.2V$ |
| Cascode MOS                                      | $\approx g_{m2}r_{ds2}r_{ds1}$                         | $V_T + 2V_{ON}$            |
| Cascode BJT                                      | $\approx \beta_F r_o$                                  | $2V_{CE(sat)}$             |
| Minimum $V_{MIN}$ Cascode Current Sink           | $\approx g_{m2}r_{ds2}r_{ds1}$                         | $2V_{ON}$                  |
| Regulated Cascode Current Sink                   | $\approx r_{ds3}g_{m3}r_{ds2}g_{m4}(r_{ds4}  r_{ds5})$ | $\approx V_T + V_{ON}$     |
| Minimum $V_{MIN}$ Regulated Cascode Current Sink | $\approx r_{ds3}g_{m3}r_{ds2}g_{m4}(r_{ds4}  r_{ds5})$ | $\approx V_{ON}$           |

### Summary of MOS Current Mirrors

| Current Mirror            | Accuracy       | Output Resistance | Input Resistance    | Minimum Output Voltage                  | Minimum Input Voltage                 |
|---------------------------|----------------|-------------------|---------------------|---|---------------------------------------|
| Simple                    | Poor           | $r_{ds}$          | $\frac{1}{g_m}$     | $V_{ON}$                                | $V_T + V_{ON}$                        |
| Cascode                   | Excellent      | $g_m r_{ds}^2$    | $\frac{2}{g_m}$     | $V_T + 2V_{ON}$                         | $2(V_T + V_{ON})$                     |
| Wide Output Swing Cascode | Excellent      | $g_m r_{ds}^2$    | $\frac{1}{g_m}$     | $2V_{ON}$                               | $V_T + V_{ON}$                        |
| Self-biased Cascode       | Excellent      | $g_m r_{ds}^2$    | $R + \frac{1}{g_m}$ | $2V_{ON}$                               | $V_T + 2V_{ON}$                       |
| Wilson                    | Poor           | $g_m r_{ds}^2$    | $\frac{2}{g_m}$     | $2(V_T + V_{ON})$                       | $V_T + 2V_{ON}$                       |
| Regulated Cascode         | Good-Excellent | $g_m^2 r_{ds}^3$  | $\frac{1}{g_m}$     | $V_T + 2V_{ON}$<br>(min. is $2V_{ON}$ ) | $V_T + V_{ON}$<br>(min. is $V_{ON}$ ) |

## Summary of BJT Current Mirrors

| Current Mirror            | Accuracy       | Output Resistance | Input Resistance        | Minimum Output Voltage | Minimum Input Voltage  |
|---------------------------|----------------|-------------------|-------------------------|------------------------|------------------------|
| Simple                    | Poor           | $r_o$             | $\frac{1}{g_m}$         | $V_{CE(sat)}$          | $V_{BE}$               |
| Cascode                   | Excellent      | $\beta F r_o$     | $\frac{2}{g_m}$         | $V_{CE(sat)} + V_{BE}$ | $2V_{BE}$              |
| Wide Output Swing Cascode | Excellent      | $\beta F r_o$     | $\frac{1}{g_m}$         | $2V_{CE(sat)}$         | $V_{BE}$               |
| Self-biased Cascode       | Excellent      | $\beta F r_o$     | $R + \frac{1}{g_m}$     | $2V_{CE(sat)}$         | $V_{CE(sat)} + V_{BE}$ |
| Wilson                    | Poor           | $\beta F r_o$     | $\frac{2}{g_m}$         | $V_{CE(sat)} + V_{BE}$ | $V_{CE(sat)} + V_{BE}$ |
| Regulated Cascode         | Good-Excellent | $\beta F r_o$     | $\frac{1}{g_m}$ or less | $V_{CE(sat)}^*$        | $V_{CE(sat)}^*$        |

\* One can design the regulated cascode so that effectively the minimum value of  $V_{MIN}$  (out) is just  $V_{CE(sat)}$ .

## Active Load Amplifiers

What is an active load amplifier?

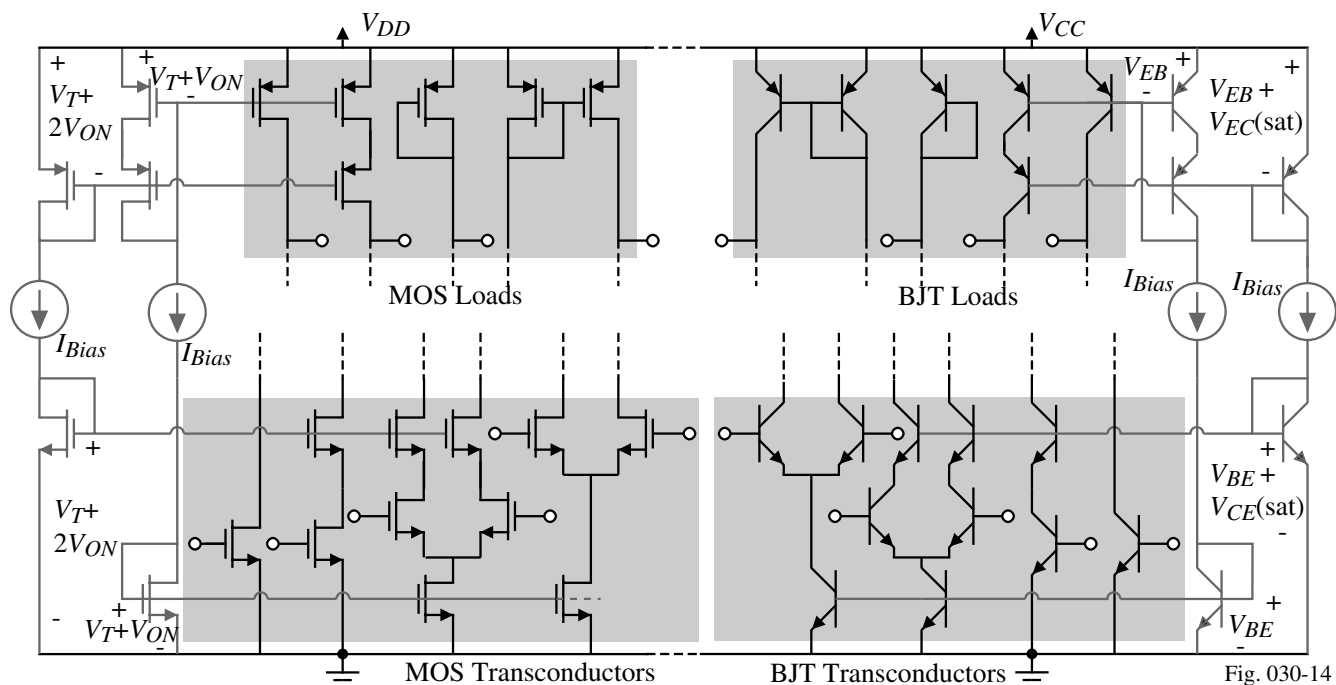


Fig. 030-14

It is a combination of any of the above transconductors and loads to form an amplifier.

(Remember that the above are only *some* of the examples of transconductors and loads.)

## BJT Differential Amplifier with a Current Mirror Load

### Design Considerations:

#### Constraints

Power supply  
Technology  
Temperature

#### Specifications

Small-signal gain  
Frequency response ( $C_L$ )  
ICMR  
Slew rate ( $C_L$ )  
Power dissipation

### Relationships

$$A_v = g_{m1}R_{out}$$

$$\omega_{-3dB} = 1/R_{out}C_L$$

$$v_{IC(max)} = V_{CC} - |V_{BE3}| - V_{CE1(sat)} + V_{BE1} \approx V_{CC} - V_{CE1(sat)}$$

$$v_{IC(min)} = V_{EE} + V_{CE5(sat)} + V_{BE1}$$

$$SR = I_{EE}/C_L$$

$$P_{diss} = (V_{CC} + |V_{EE}|) \cdot \text{All dc currents flowing from } V_{CC} \text{ or to } V_{EE}$$

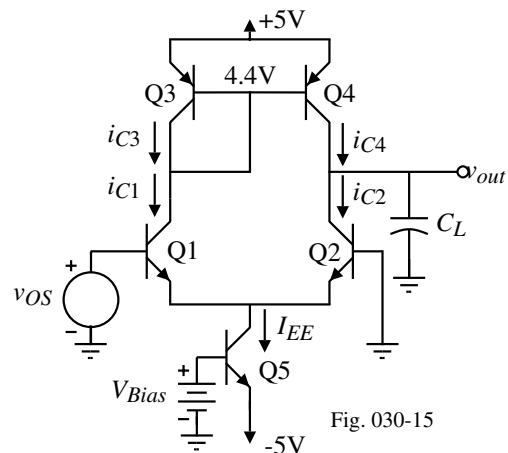


Fig. 030-15

## CMOS Differential Amplifier with a Current Mirror Load

### Design Considerations:

#### Constraints

Power supply  
Technology  
Temperature

#### Specifications

Small-signal gain  
Frequency response ( $C_L$ )  
ICMR  
Slew rate ( $C_L$ )  
Power dissipation

### Relationships

$$A_v = g_{m1}R_{out}$$

$$\omega_{-3dB} = 1/R_{out}C_L$$

$$V_{IC(max)} = V_{DD} - V_{SG3} + V_{TN1}$$

$$V_{IC(min)} = V_{DS5(sat)} + V_{GS1} = V_{DS5(sat)} + V_{GS2}$$

$$SR = I_{SS}/C_L$$

$$P_{diss} = (V_{DD} + |V_{SS}|) \cdot \text{All dc currents flowing from } V_{DD} \text{ or to } V_{SS}$$

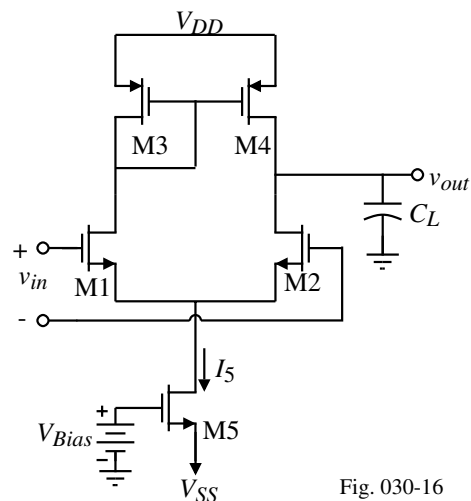


Fig. 030-16

## **Summary of Active Load Amplifiers**

- Active load amplifier consists of a transconductor and a load
  - There are a large number of combinations of loads and transconductors possible. We have not considered the many cascoded possibilities and other configurations.
- The BJT amplifier generally has more gain and wider signal swing than the MOS amplifier
- The voltage gain of the MOS transconductor with a current source or current mirror load is inversely proportional to the square root of the bias current.
- The current mirror load differential amplifier is a widely used input stage
- The frequency response is generally determined by the dominant pole which is found at points in the circuit that are high impedance to ac ground and large capacitance
- The active load amplifier is the primary gain stage in operational amplifiers and other applications and will be a fundamental building block in more complex circuits
- Performance not considered include slew rate and noise

## **SUMMARY**

- Single and Multiple Transistor Amplifiers
  - Characterization
  - BJT: Common emitter, common-base, common-collector, general
  - MOSFET: Common source, common-gate, common-drain, general
- Cascode Amplifiers
- Differential Amplifiers
  - Differential mode analysis (balance requirements)  $\Rightarrow$  Half-circuit concept
  - Common mode analysis  $\Rightarrow$  Half-circuit concept
  - Input common mode range and slew rate
- Transistor Current Sources and Current Mirrors
- Active Load Amplifiers
- Other Material not Included in this Review
  - Voltage and Current References
  - Bandgap Voltage Reference
  - Simple two-stage op amps